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RESEARCH PAPER

0.8–8 GHz 4-bit MMIC phase shifter for T/R modules

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This paper presents the design approach and test results of a full passive, decade bandwidth GaAs MMIC, composed by a phase shifter (PS) with a cascaded absorptive single pole double throw *switch, suitable for transmitter/receiver modules in active electronically scanned array. The proposed PS – fabricated using a UMS GaAs 0.25 PHEMT process – combines all-pass filters with high-pass filters, in order to provide less than 13 dB insertion loss, less than* $\pm 20^{\circ}$ *phase error and less than* ± 2.5 *dB amplitude error in the 0.8–8 GHz bandwidth.*

Keywords: MMIC, Monolithic phase shifters, Broadband, T/R modules

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I. INTRODUCTION

A phase shifter is a key element whose bandwidth commonly represents the bottleneck of T/R modules used in modern antenna phased arrays (APAs) for electronic warfare (EW) applications [1]. Moreover, when an active phased array capable of transmitter/receiver (T/R) function is required, a reciprocal phase shifter (PS) is desirable in order to simplify the T/R architecture, avoiding "common leg" architecture. Many solutions have been investigated in scientific literature to develop PS MMICs as illustrated in Table 1, where the classical topologies are sorted by bandwidth performance. Group "A" topologies, studied in [12] offers reciprocity but they have limited bandwidth, for this reason they are not suitable for wideband applications. The "B" group topologies are reciprocal and able to reach around two octaves bandwidth; nevertheless they are generally based on Lange couplers, which are difficult to integrate when operative frequency falls below 1 GHz. Group "C" topologies are used when the bandwidth becomes ultra large, starting from relative low frequencies, they are suitable for EW applications in the communication bandwidth below 2 GHz; most of them use active components, which imply the need of power supply and offer a non-reciprocal response. Reflection type PS with active circulators is another approach used in wideband MMIC; the active element synthesis allows to overcome the bandwidth limitation of the classical Lange coupler used as reflectometer [8]. Another topology, mostly used in SiGe design, where lumped elements approach is preferred, is to realize a PS using an active vector modulator, composed by poly-phase filters or quadrature all-pass filters (APF), to obtain four orthogonal vectors to be amplitude modulated with variable gain amplifiers and then recombined [9]. Another approach is to cascade several APF in order to obtain an ultra large bandwidth. The drawback of this approach is represented by the high insertion loss. For this reason the PS presented in paper [11] makes use of amplifiers to limit the insertion loss. An interesting variation, demonstrated in hybrid technology, consists of using APF with both low pass filters (LPF) and high pass filters (HPF) [13]. Another approach [14] consists of operating the phase shifting in the optical domain using stimulated Brillouin scattering based phase shifters. To perform such function, it is necessary to properly modulate the radio frequency (RF) signal into optical domain and demodulate it back to RF. The obtained performance is very impressive in terms of bandwidth (1.5–31 GHz) and determines low phase and amplitude errors, unfortunately the technology leads to a non-compact solution if compared with a monolithic microwave integrated circuit (MMIC). The papers [13, 14] have not been inserted in the table because they have not been demonstrated in MMIC

Table 1. MMIC phase shifter topology versus bandwidth.

Group	Bandwidth (Octaves)	Topology	Reciprocal	Reference
A	$B \leq 1$	Loaded transmission lines	Y	[2]
		Switched transmission lines	Y	[3]
		Switched paths HPF and LPF	Y	[4]
B	$1 < B \leq 2$	Reflection type	Y	[5]
		Switched with shorted coupled lines	Y	[6]
		Switched filter circuits	Y	[7]
C	$B > 2$	Reflection type with active circulators	N	[8]
		Active vector modulators	N	[9, 10]
		APF with buffers	N	[11]
		APF with phase equalizer	Y	This work

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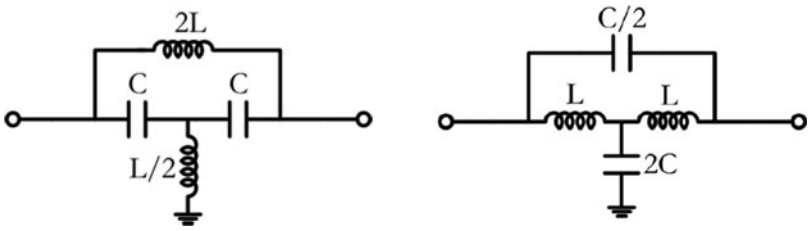

Fig. 1. Common APF topologies.

realization. In this paper, for the first time at the best knowledge of the authors, a full passive and reciprocal MMIC 4-bit PS with 1 decade of bandwidth from 0.8 to 8 GHz is presented and is also demonstrated that LPF is not strictly necessary to achieve broadband performance if compared with [13].

Since this work presents a PS with $B > 2$, the comparison with the "state of art" will be limited to the works listed in group C, Table 1.

The Reflection type with active circulators [8] is a quite attractive architecture in terms of phase error ($\pm 2.1^\circ$ for a 85° phase shift), nevertheless the information provided in the paper is not sufficient for a full comparison for higher phase shifts (337.5°). The most important difference is the active nature of the architecture, which can provide a low insertion loss, unfortunately the non-reciprocity is an important drawback, which make this architecture unusable in the application the PS presented in this paper was designed for.

Active vector modulators architecture [9, 10] is typically used in CMOS and SiGe, where the use of active components is preferred above passive components. This aspect leads to highly integrated, but non-reciprocal phase shifters. Moreover, a vector modulator phase shifter has no digital steps, because it is intrinsically analog, for this reason it needs a digital to analog converter to synthesize a desired phase step. The obtained performance are good in both [9], where a 15° RMS phase error has been presented in the frequency range from 6 to 20 GHz, and [10], where 7° RMS have been demonstrated in the frequency range from 0.5 to 6 GHz.

APF with buffers architecture [11] is quite similar to the one presented in this paper, in fact both PS use two all pass cells to provide the desired phase shift. Nevertheless, in [11] there is no use of high pass compensation (which is discussed in the presented paper); for this reason, phase performance is apparently poor, below 1 GHz. Furthermore, the architecture [11] makes use of active cells, which provides a lower insertion loss; unfortunately, the non-reciprocity, represent an unacceptable drawback for the application mentioned in the presented paper.

After this overview on the traditional design approach, Section II will introduce the novel methodology, while Section III is devoted to the presentation of the design and measured results, confirming the effectiveness of the proposed strategy. In Section IV the conclusions have been presented.

II. NOVEL DESIGN APPROACH

The proposed phase shifter is based on APF networks, which are very suitable since they theoretically have a frequency independent amplitude response.

In Fig. 1, two common APF topologies are depicted. A proper choice of L and C values allows to provide the desired phase shift and maintain the impedance matching at the same time. Both topologies can be designed using (1), where Z_o is the characteristic impedance and ω_o is the "transition frequency" at which a 180° phase shift occurs.

$$\begin{cases} Z_o = \sqrt{\dfrac{L}{C}} \\ \omega_o = \dfrac{1}{\sqrt{LC}} \end{cases}. \tag{1}$$

The desired phase shift, as observed in [15], can be obtained as difference between two APFs phase versus frequency response, tuned at different transition frequencies: ω_{oi} and $\omega_{oi'}$ for APFi and APFi', respectively, as shown in Fig. 2.

An example of a 22.5° ideal PS cell response, composed by a single stage APF, is visible in Fig. 3 where a low phase error – defined as the difference between nominal and actual phase – can be granted on a narrow band centered on the ω_i frequency, according to (2).

$$\Delta\phi_i(\omega) = 2\tan^{-1}\left(\frac{\omega}{\omega_i p_i} - \frac{\omega_i p_i}{\omega}\right) - 2\tan^{-1}\left(\frac{\omega p_i}{\omega_i} - \frac{\omega_i}{\omega p_i}\right), \tag{2}$$

where the transition frequency of each APF is defined according to (3).

$$p_i = \frac{\omega_{oi}}{\omega_i} = \frac{\omega_i}{\omega'_{oI}}. \tag{3}$$

In order to extend the PS bandwidth, assuming a $\pm 10^\circ$ maximum error as goal, it is possible to use two cascaded APFs with a proper frequency shift, as discussed in [15] and shown in Figs 4 and 5.

More than two cascaded cells can be employed to further extend the bandwidth, unfortunately, the higher the number

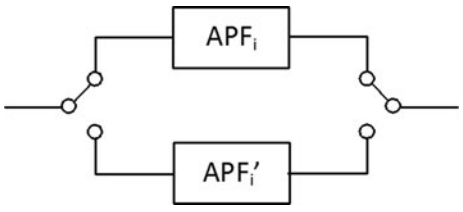

Fig. 2. PS cell with single APF.

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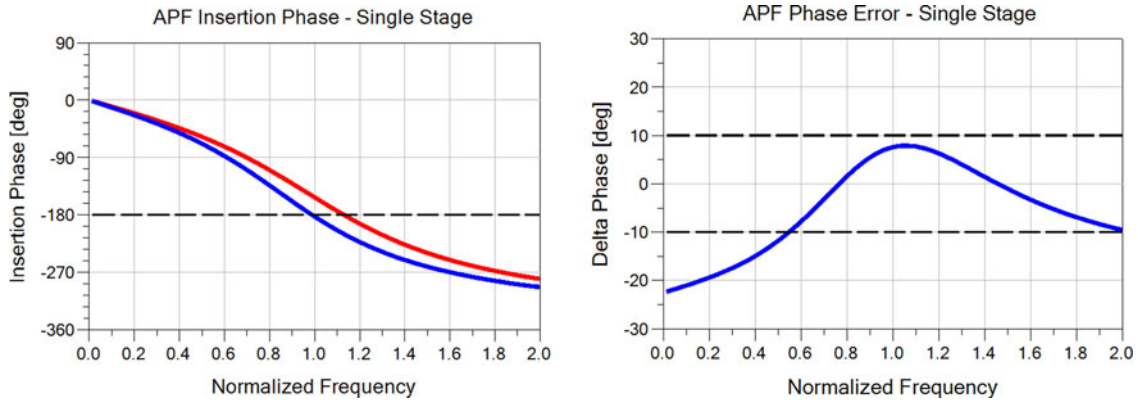

Fig. 3. A 22.5° cell response with single stage APFs. Insertion phase on the left and phase error on the right.

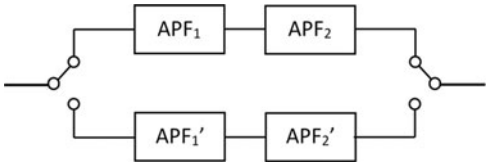

Fig. 4. PS cell with two cascade APFs.

of APFs, the bigger the area occupation and insertion loss. Furthermore, since every APF phase response tends to be zero at low frequency, the corresponding phase difference tends to be zero as well, making the phase shifter unusable in that frequency region; increasing the APFs number, does not effectively solve this problem, as highlighted in Fig. 6.

In order to compensate the low frequency limitation it is possible to insert a HPF, whose cut-off frequency shall be accurately selected to improve the low frequency response, leaving the high frequency behavior unaltered. Such HPF can be placed in the cell as indicated in Fig. 7, where APF_1 represents the reference state. The cut-off frequency selection presents another drawback that must be kept into account: the higher the phase boost, the higher the amplitude drop, due to the filtering action.

As visible in Fig. 8, the HPF solved the low frequency issue with no relevant effect at high frequency.

As final step it is possible to improve the overall performance using a CAD optimization, as shown in Fig. 9.

This solution provides an extension of the phase shifter bandwidth at low frequency, maintaining the number of APFs as little as possible; it can be also extended to realize larger phase steps which would require several APF stages as presented in [11].

III. PHASE SHIFTER DESIGN AND MEASURED RESULTS

A broadband 4-bit phase shifter has been designed, realized, and tested. The PS block diagram is shown in Fig. 10.

There are four cells which provide 22.5°, 45°, 90°, and 180° shift and an absorptive single pole double throw (SPDT) switch. The PS cell controls are: 0 V and −2.5 V. In order to compensate the low frequency limitation, two different types of phase equalizers have been adopted. The 22.5° and 45° cells are based on a single stage APF with the addition of two series capacitor, as depicted in Fig. 11 (top), while the 90° and 180° cells are based on a double stage APF with the addition of a T shape-HPF, as shown Fig. 11 (down).

Both HPF choices have been made taking physical and electrical symmetry into account. Furthermore, in order to keep every PS cell size as little as possible, a planar transformer solution has been adopted for every APF. The transformer is used as substitute of the "uncoupled" pair of inductance, suggested on the right of Fig. 1.

Since mutual coupling should be taken into account, the transformer substitution requires an extension of the design

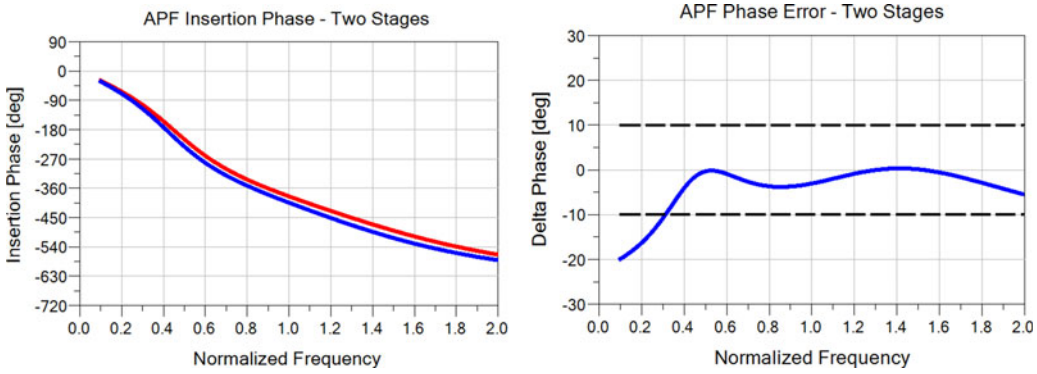

Fig. 5. A 22.5° cell response with double stage APFs. Insertion phase on the left and phase error on the right.

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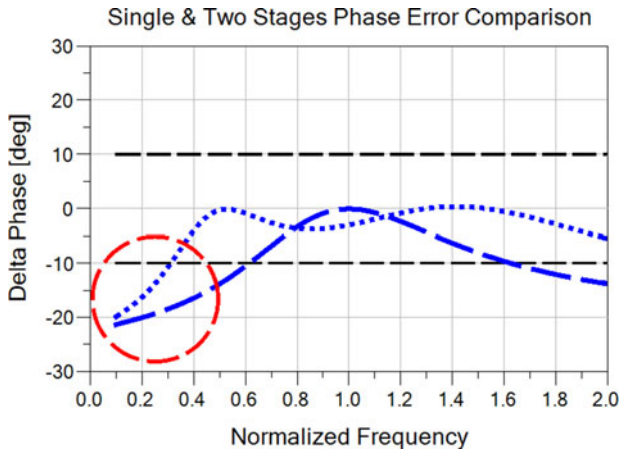

Fig. 6. Low Frequency issue of single and two stages PS cells.

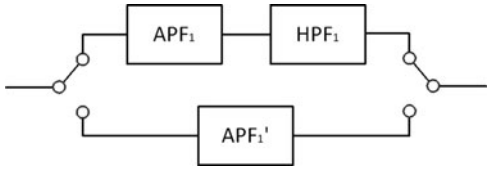

Fig. 7. PS cell with single stage APFs and HPF phase equalizer.

equations [11]. The 22.5° cell is presented as example in Fig. 12 (left), the planar transformer discussed before is clearly visible in both paths, as well as the two series capacitors placed in the upper path.

In Fig. 13, a comparison between electromagnetic (EM)-simulated and measured performance of the single 22.5° cell is depicted in Fig. 12 (left). The results show a good match between the simulation and obtained measurements.

At the end of the phase shifter, there is an high isolation, absorptive SPDT switch, which has been designed and tested in a test cell depicted in Fig. 12 (right). Both switch paths are composed by a series field effect transistor (FET) followed by two FETs in shunt connection. Each path ends with the circuitry shown in Fig. 14, which provides the 50 Ω matching when the series FET is open and the parallel FETs are shunted.

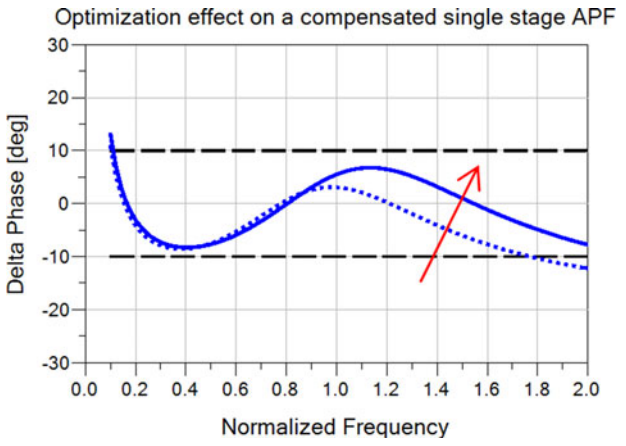

Fig. 9. Phase error of a 22.5° cell with single stage APFs and HPF (dotted line "before", solid line "after" optimization).

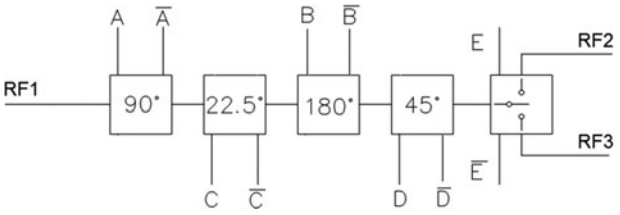

Fig. 10. PS block diagram.

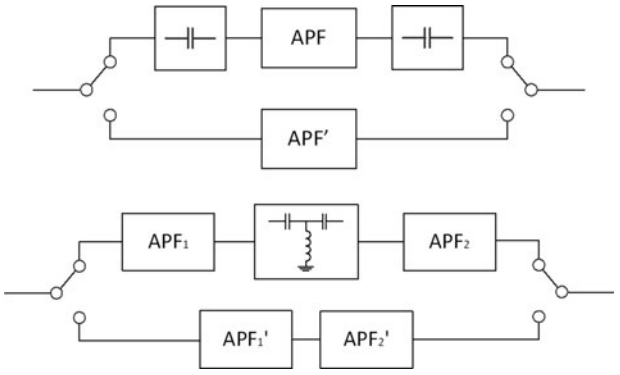

Fig. 11. Phase equalizers used for 22.5° and 45° cells (top) and for 90° and 180° cells (bottom).

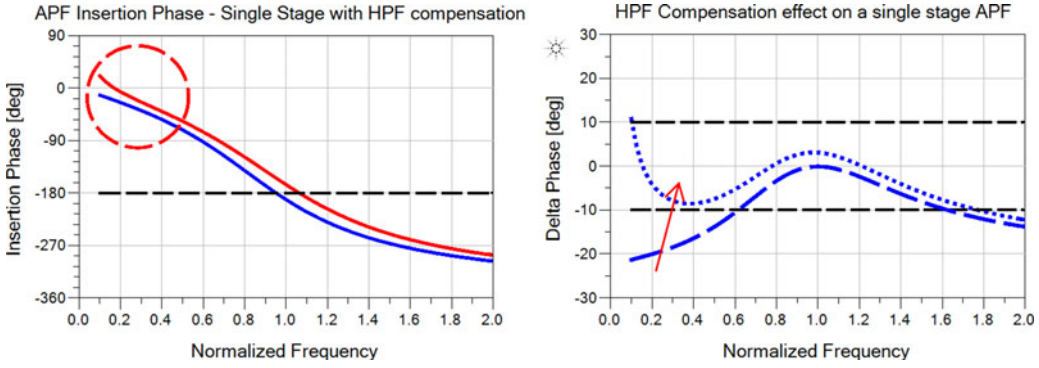

Fig. 8. A 22.5° cell response with single stage APFs and HPF. Insertion phase on the left and phase error on the right (dashed line "before", dotted line "after" compensation).

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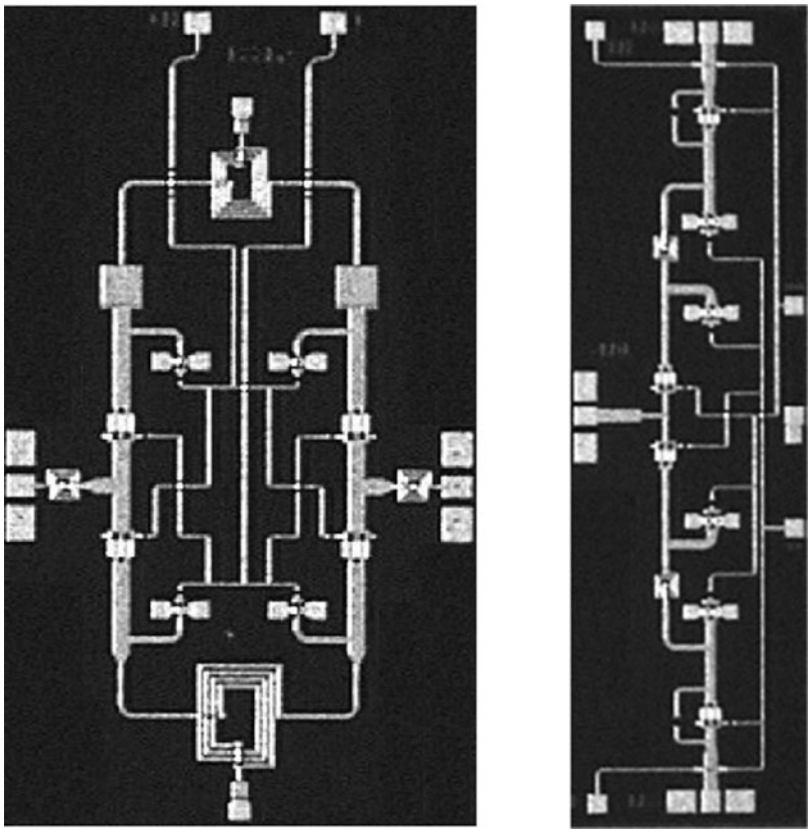

Fig. 12. Microphotograph of the fabricated PS 22.5° test cell (1.6 × 3.7 = 6 mm²) on the left and fabricated absorptive SPDT test cell (4.3 × 1.3 = 5.6 mm²) on the right.

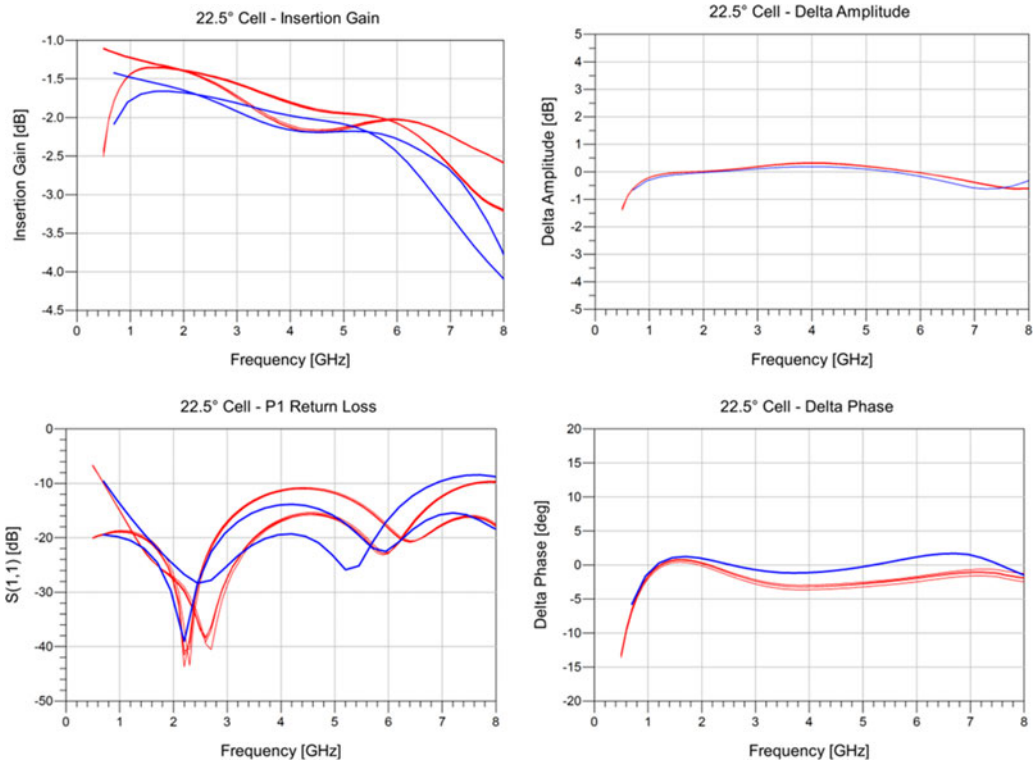

Fig. 13. EM-simulated (blue line) and measured performance (red line) comparison of the single test cell 22.5° step.

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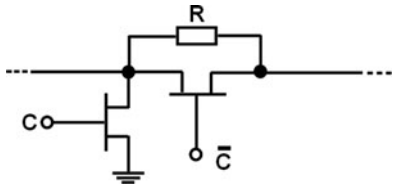

Fig. 14. Last section switch implementation detail.

In Fig. 15, there is a comparison between EM-simulated and measured performance of the single SPDT absorptive switch test cell, depicted in Fig. 12 (right). The results show a good match between the simulation and obtained measurements.

Since the switch is designed to be absorptive, it is important to note the good return loss all over the operating bandwidth, in both on and off states.

When cascaded, each cell is loaded by the adjacent ones, exhibiting different input/output impedance; in this condition the single cell behavior will be different from the expected behavior on 50 Ω terminations, causing undesired phase errors.

A common way to overcome this problem consists in trying to re-center the chain performance by using optimization or tuning tools provided by any microwave CAD environment. The above mentioned approach however is not always viable, due to the overall design complexity and the resulting resource demand in terms of simulation time. In this case the cell sequence (Fig. 10) has been determined using the algorithm proposed in [16].

In Fig. 16 the insertion gain and amplitude error over all phase shifter steps is presented. The insertion gain contains the contribution of the SPDT switch insertion loss (Fig. 15).

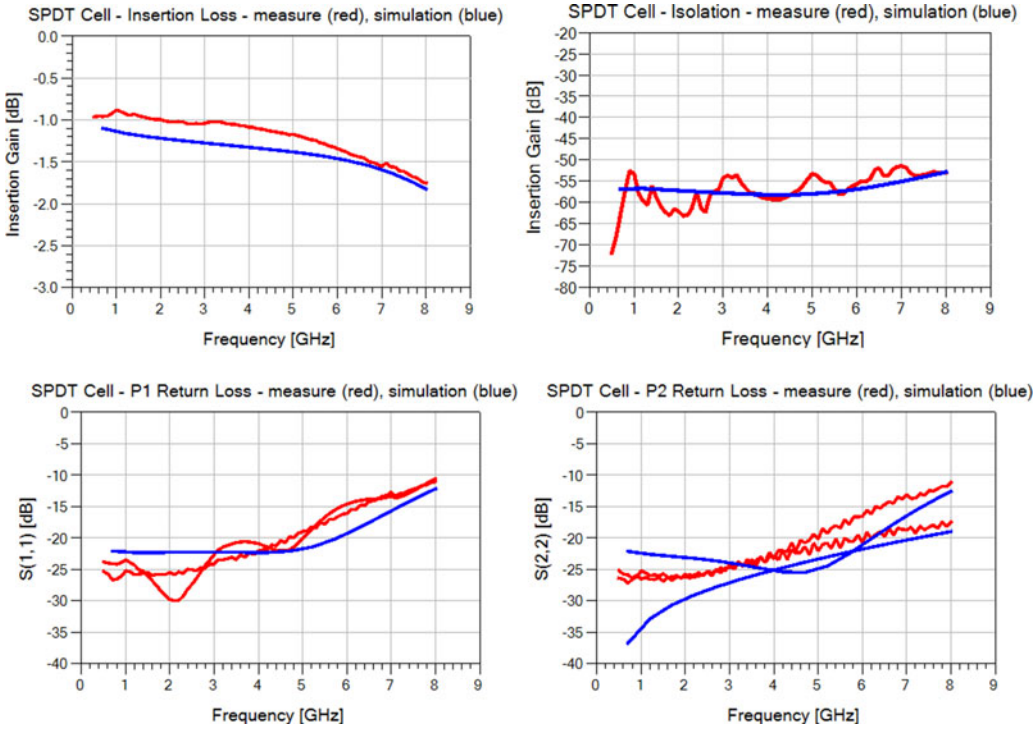

Fig. 15. EM-simulated (blue line) and measured performance (red line) comparison of the absorptive SPDT test cell.

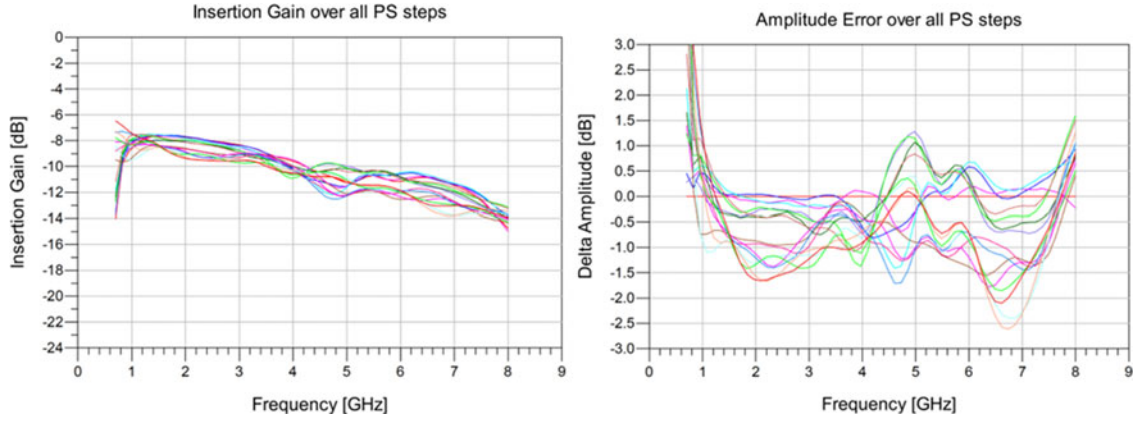

Fig. 16. Measured insertion gain (left) and amplitude error (right) over all the phase states.

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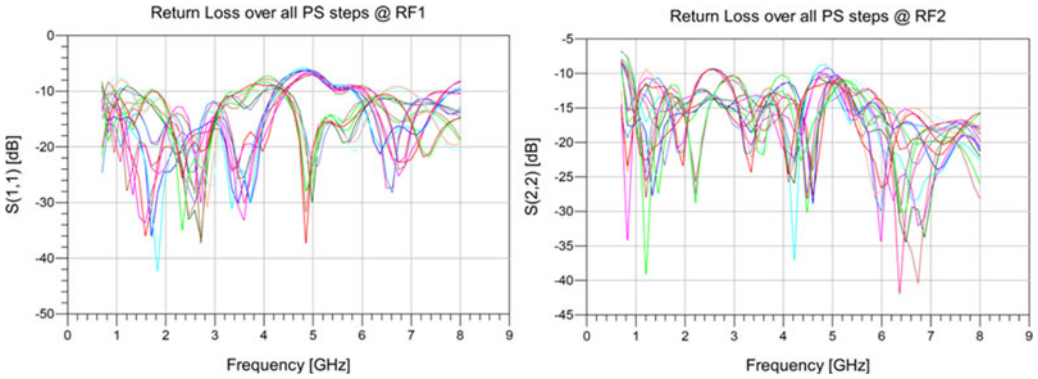

Fig. 17. Measured $S(1,1)$ and $S(2,2)$ [dB] over all the phase states.

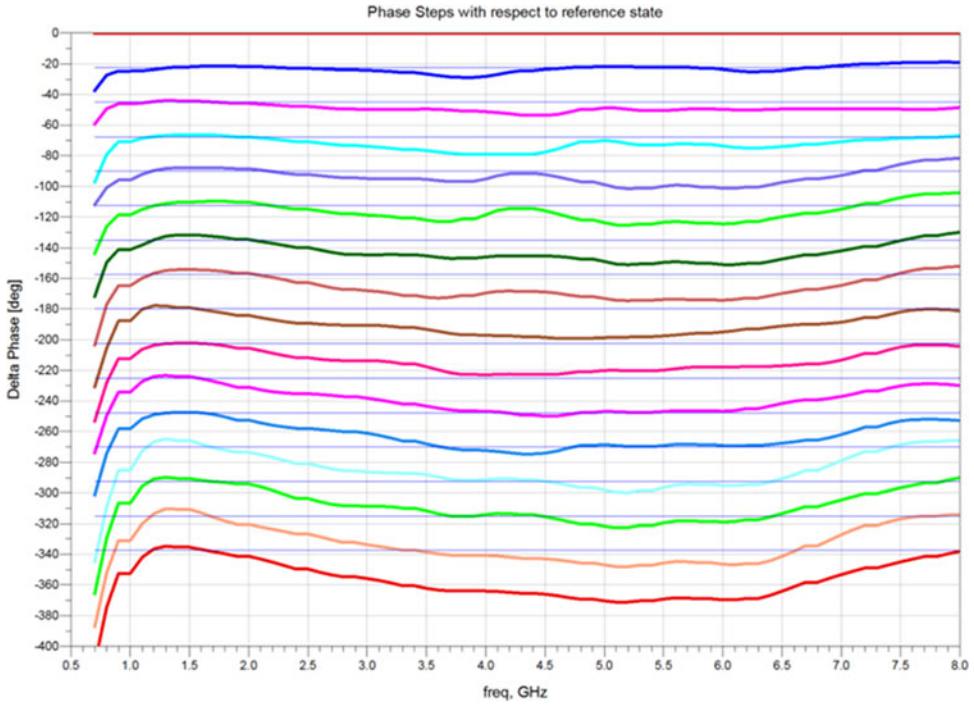

Fig. 18. Measured Delta Phase steps with respect to o° (reference step).

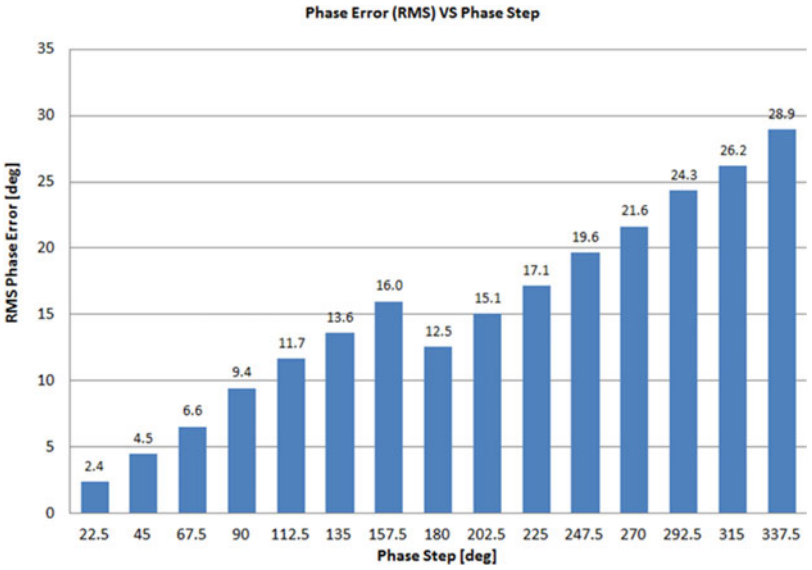

Fig. 19. Measured RMS Phase Error with respect to the phase step.

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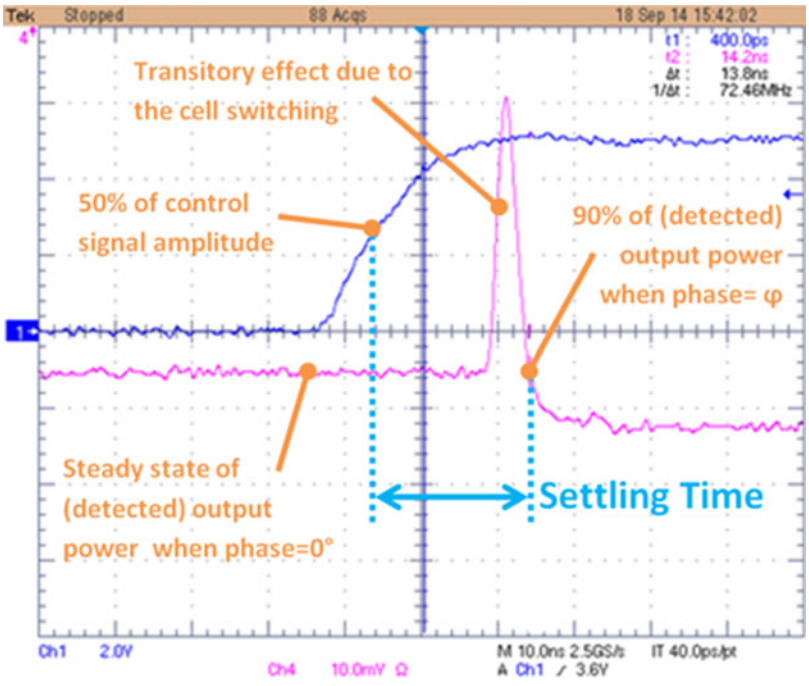

Fig. 20. Settling time measurement criteria for $o^{\circ} \rightarrow \phi'^{\circ}$ transition.

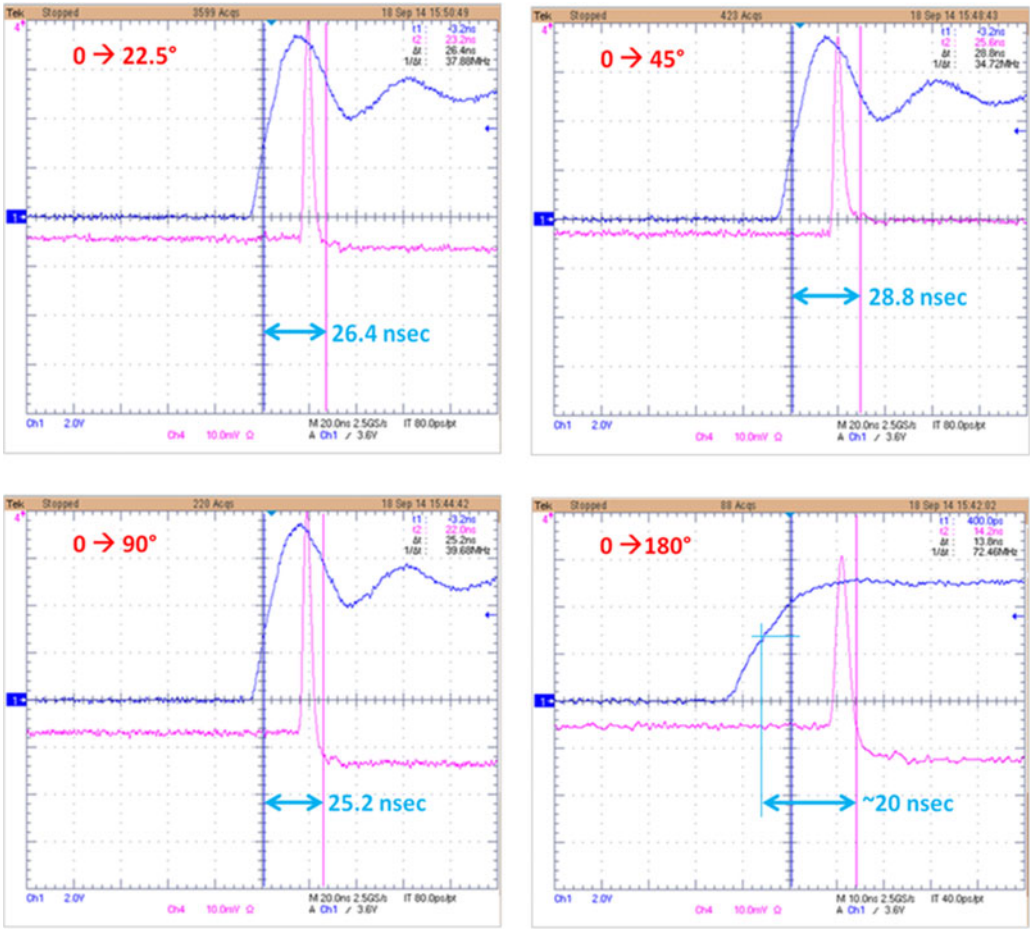

Fig. 21. Settling time measurement for the fundamental steps transitions.

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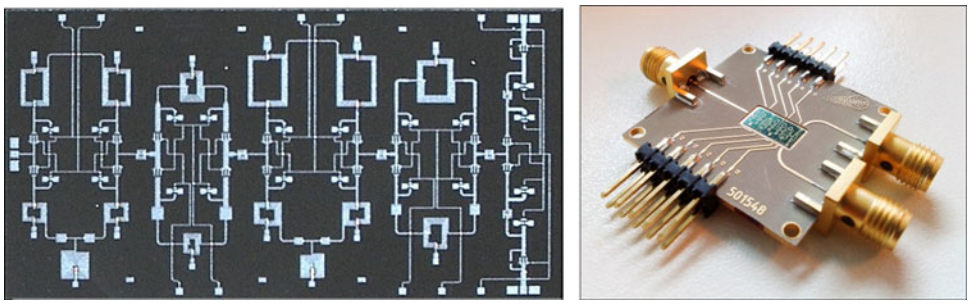

Fig. 22. Photograph of the fabricated PS (4.4 × 8.5 = 37 mm²) on the left and the test fixture used to validate the PS design provided by UMS on the right.

The insertion loss of the switch is around 1.8 dB at 8 GHz, due to the absorptive topology that requires an additional switch element at the end of each leg of the switch. The phase shifter insertion loss without the switch is around 12 dB at 8 GHz.

As visible in Fig. 16, at low frequency there is an amplitude cut-off introduced by the HPF. The PS return loss at RF1 and RF2 port is shown in Fig. 17.

The phase performance is presented in Fig. 18.

The RMS Phase error, with respect to the nominal phase step, is shown in Fig. 19

The measured phase performance – in terms of peak to peak (Fig. 18) error – is less than $\pm 20^\circ$ in the full operating bandwidth, considering 180° step as reference. In the worst case (all cells activated), the measured performance in terms of RMS error (Fig. 19) is slightly less than 29°. On the contrary, the elementary phase steps are below 12.5° RMS phase error.

The PS should be characterized in terms of phase settling time (defined from the 50% of the control signal voltage to the 90% of output required phase). For practical purpose the measure has been performed analyzing the amplitude response, assuming that either of the phases and amplitude of output signal take the same time to settle at 90% of their steady state value. Figure 20 shows the way the measurement should be read: the settling time has been measured using a two channels oscilloscope, where CH1 is dedicated to the control signal (trigger on the rising edge) while CH2 is connected to a negative voltage power detector.

The test fixture in Fig. 22 has been driven by an interface board, which adds an additional 10 ns delay, which should be subtracted from the results showed in Fig. 21. Compared with the expected use of the presented phase shifter, the settling time is fully compliant with the application requirement: in fact, in a T/R module used for a EW application, it is necessary to keep the amplitude settling time below 60 ns; such time is typically determined by the final power stages of the transmission chain. Same considerations apply to the phase settling time anyway – its strict relation with the amplitude response – guarantees that the phase performance is stable within 60 ns.

A photograph of the fabricated PS is shown in Fig. 22. As first prototype, particular attention was paid to limit EM coupling between cells as much as possible, this inevitably led to a bigger size; since there is room for improvement, there is a concrete possibility to reduce the chip area on a second design, to be used in production.

In [11], the MMIC phase shifter has been divided into two parts, this solution guarantees yield improvements but does not reduce the large area occupation.

IV. CONCLUSION

A broadband PS based on APF and HPF filters has been designed, using a reduced number of APFs and avoiding the use of LPFs, in order to decrease the insertion loss and keep MMIC size as little as possible. Due to the reciprocity requirement, no amplifiers have been used. The PS has been fabricated using a GaAs 0.25 PHEMT process in order to provide less than 13 dB insertion loss, less than $\pm 20^\circ$ phase error (considering 180° step as reference) and less than ± 2.5 dB amplitude error in the 0.8–8 GHz bandwidth. The phase shifter settling time is below 20 ns. Provided results show a very good agreement between simulation and measurement, such achievement fully satisfies the T/R module broadband requirements for EW applications.

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