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A new nonlinear HEMT model for AlGaN/GaN switch applications

GUILLAUME CALLET[1,2], JAD FARAJ[1], OLIVIER JARDEL[2], CHRISTOPHE CHARBONNIAUD[3], JEAN-CLAUDE JACQUET[2], TIBAULT REVEYRAND[1], ERWAN MORVAN[1], STÉPHANE PIOTROWICZ[2], JEAN-PIERRE TEYSSIER[1] AND R. QUÉRÉ[2]

We present here a new set of equations for modeling the I–V characteristics of Field Effects Transistors (FETs), particularly optimized for AlGaN/GaN HEMTs. These equations describe the whole characteristics from negative to positive breakdown loci, and reproduce the current saturation at high level. Using this model enables to decrease the modeling process duration when a same transistor topology is used for several applications in a T/R module. It can even be used for switches design, which is the most demanding application in terms of I–V swing. Moreover, particular care was taken to accurately model the first third orders of the current derivatives, which is important for multione applications. We also focused on an accurate definition of the nonlinear elements such as capacitances for power applications. There are 18 parameters for the main current source (and six for both diodes I_{gs} and I_{gd}). This can be compared to Tajima's equations-based model (13 parameters) or to the Angelov model (14 parameters), which only fit the I–V characteristics for positive values of V_{ds}. We will detail here the model formulation, and show some measurements/modeling comparisons on both I–V, [S]-parameters and temporal load-pull obtained for a 8×75 μm GaN HEMT, with 0.25 μm gate length.

Keywords: Switch, SPST, SPDT, GaN, Model

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I. INTRODUCTION

AlGaN/GaN HEMT are a promising technology, especially for T/R modules including several elements as power amplifiers, LNA, or power switches. For both these elements, distinct models already exist, such as [1–4] for power amplifiers applications, or [5] in-switch mode amplifiers applications. The new trend to improve the performances, the cost, and the size of these modules is to design all these functions in the same technology and on the same chips. Thus, the same transistor topologies can be used in different functions. Designing each of these functions implies having models with different degrees of accuracies, and it is very challenging to obtain a valid description of the nonlinear elements for several applications with the same model, and improve the definition of drain current source for both positive and negative drain voltage. However, in order to reduce the modeling process duration, it is very interesting to reuse, as far as possible, some parts of a model to design a new one for another application. The *I–V* model we will describe here was designed in this context.

There are different needs concerning the *I–V* model:

- For the design of power amplifiers, the model has to be capable of predicting very accurately the *I–V* curves at positive drain–source voltages, the partial derivatives g_m and g_d, the knee voltage, and the decrease of the transconductance at high current (to fit the power saturation and the maximum of Power Added Efficiency (PAE)).
- For the design of power switches, the model has to be capable of predicting the *I–V* curves at both positive and negative drain–source voltages, and particularly the partial derivatives for the "ON" command voltage, for which the transistor works in the linear region most of the time. Special care has to be taken with regard to the continuity of the current and its derivatives in the proximity of $V_{ds} = 0$ V. Most of the time, the designers use splined *I–V* models for these kinds of designs, but their possible number of derivations is limited to the degree of the interpolation polynomial, and their high sensitivity to measurement imprecisions in the vicinity of $V_{ds} = 0$ V can induce some important errors on the partial derivatives. Moreover, it is important that the model reproduces the breakdown, as it sets the power injection limits of the switches.
- For multitone application, predicting the third-order intermodulation requires to accurately model the third- and higher-order derivatives of I_{ds} with respect to V_{gs} [6].

We will present here the equations of a new model. The model in this case is extracted from pulsed *I–V* measurements at room temperature in order to reduce the thermal effects; due to its cold quiescent bias and low dissipated power, we can disregard the self-heating effects with good approximation [7, 8]. The measured devices can also reveal sensitive to trapping effects. Thermal and/or trapping subcircuits can then be added in the same manner as in [9].

[1]XLIM-UMR CNRS 6172-Université de Limoges, 7, rue Jules Vallès, 19100 Brive-la-Gaillarde, France.
[2]Alcatel-Thales 3-5lab, Route de Nozay, 91640 Marcoussis, France.
[3]AMCAD Engineering, ESTER Technopole, 87069 Limoges, France.
Corresponding author:
G. Callet
Email: guillaume.callet@xlim.fr

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II. EQUATIONS OF THE MODEL

A) Equations of the main current source

The main current source is described by the following equations:

$$Id = I_{dss}\, dhyp[Vdsn + A\, Vdsn^3] \cdot Vgsn \tag{1}$$

with

$$Vgsn = Vgs_{lin}\left[1 + \frac{Vp_0}{vp}\right]^N, \tag{2}$$

$$vp = Vp_0 + H_{asympt}(-Vds(1 - Vpdec),\, 1 \times 10^{-4},\, 0) + P\, V_{ds}, \tag{3}$$

$$Vdsn = \frac{V_{ds}}{Vknee\,[1 + W\,(Vgsn - 1)]}, \tag{4}$$

$$Vgs_{lin} = H_{asympt} \times \left[\frac{V_{satp} + vp}{H_{asympt}\left(V_{satp} + vp + Vp_0,\, 1 \times 10^{-4}, \frac{-vp}{vp_0}\right)}, s_{vp}, 0\right], \tag{5}$$

$$V_{satp} = L_{asympt}\left[\frac{Vgs}{2}, S_{sat1p}, V_{sat1p}\right] + L_{asympt}\left[\frac{Vgs}{2}, S_{sat2p}, V_{sat2p} - V_{sat1p}\right], \tag{6}$$

$$s_{vp} = H_{asympt}\left[L_{asympt}\left(\frac{-V_{ds}}{Sneg}, S_{satn}, V_{satn}\right), 1 \times 10^{-4}, gmvp\right], \tag{7}$$

with

$$A = cval(Apos,\, Aneg,\, V_{ds},\, \alpha_{trval}), \tag{8}$$

$$W = cval(Wpos,\, Wneg,\, (V_{gs} + vp0),\, \alpha_{trval}). \tag{9}$$

Four functions are used in these equations. The function *dhyp* allows reconstructing the current envelope and is quite similar to a tanh function:

$$dhyp(x) = \frac{x}{\sqrt{1 + x^2}}. \tag{10}$$

The *cval* function allows changing the value of a parameter, x from x_{neg} to x_{pos}, when its third parameter reaches the value 0, with a softness determined by the parameter α_{trval},

$$cval(x_{pos}, x_{neg}, V, \alpha_{trval}) = \frac{x_{pos} - x_{neg}}{2}\tanh(\alpha_{trval}\, V) + \frac{x_{pos} + x_{neg}}{2}. \tag{11}$$

In order to obtain smooth transitions from one domain to another, three functions named $genp(x)$, $H_{asympt}(x)$, and $L_{asympt}(x)$ were used. These functions are C_∞ and allow us to separate the definition domain in upper and lower regions in a smooth way. "a" is the smoothing parameter that acts as illustrated in Fig. 1. The behavior of these three functions is also shown in Fig. 1:

$$genp(x) = \begin{cases} \dfrac{1}{2(-x + \sqrt{1 + x^2})}, & x > -1, \\ \dfrac{-1}{2 \cdot x(1 + \sqrt{1 + (1/x^2)})}, & x \le -1, \end{cases} \tag{12}$$

$$H_{asympt}(x, a, x_H) = \begin{cases} x + a\, genp\left(\dfrac{-(x + x_H)}{a}\right), & x > -x_H, \\ x_H - a\, genp\left(\dfrac{x + x_H}{a}\right), & x \le -x_H, \end{cases} \tag{13}$$

$$L_{asympt}(x, a, x_L) = \begin{cases} x_L - a\, genp\left(\dfrac{x_L - x}{a}\right), & x > x_L, \\ -x_L + a\, genp\left(\dfrac{x - x_L}{a}\right), & x \le x_L. \end{cases} \tag{14}$$

B) Equations of the gate–drain and gate–source diodes

The classical diode equation used for modeling the gate source current Igs (reference equation 15) is no suitable here for describing the gate current Igd. Hence, a different formulation is proposed in equation 16:

$$I_{gs} = I_{sgs}\left[e^{\frac{q\, V_{gs}}{N_{gs}\, k\, T}} - 1\right], \tag{15}$$

$$I_{gd} = I_{sgd}\left[e^{\frac{q\, V_{gd} - \alpha_{gs}\,(V_{gs} - V_{tgd})}{N_{gs}\, k\, T}} - 1\right]. \tag{16}$$

Moreover, a resistance R_{leak} can be added parallel to the gate–drain diode in order to take into account the gate leakage current sometimes measured.

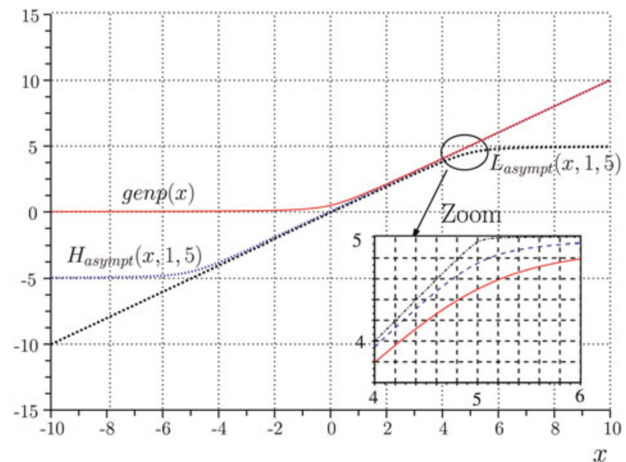

Fig. 1. Behavior of functions $genp(x)$ in the solid line, $H_{asympt}(x, 1, 5)$ in gray dots and $L_{asympt}(x, 1, 5)$ in black dots; inset function $L_{asympt}(x, 1, 5)$ for various values of $x = 0.1$ in the black plot, $x = 0.5$ in the gray plot, and $x = 1$ in the black solid line.

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C) Equations of the nonlinear capacitances for power amplifiers and switch applications

For the sake of accuracy of the model, we chose to create a one-dimensional (1D) nonlinear model capacitance and took particular care in conserving as much as possible the equations for the two modes of applications:

– For power amplifier applications, gate source capacitance (C_{gs}) and gate drain capacitance (C_{gd}) had already been defined by nonlinear 1D equations in [9], and are presented in (17).

$$Cgx = C_{gxo} + \frac{C_{gx1} - C_{gxo}}{2} \times [1 + \tanh(a_{gx}(Vm_{gx} + Vgx))] - \frac{C_{gx2}}{2} \cdot [1 + \tanh(b_{gx}(Vp_{gx} + Vgx))], \quad (17)$$

where "x" stands for "d" or "s."

– For switch applications, C_{gs} and C_{gd} are defined on a larger range of terminal voltages. Values of V_{gs} are far below V_p in the OFF-mode (typically −20 V), and are set to 0 or +1 V in the ON-mode, and V_{gd} takes positives values. We keep the equations defined in (17) and will validate the results later. In power amplifier applications, drain source capacitance (C_{ds}) is considered constant [9]. However, this approximation can no longer be made in the enlarged domain of definition corresponding to the switch applications. That is why we define it with a 1D equation that makes C_{ds} drop to a lower value (0 pF) for small or negative V_{ds}, parameterized in the DC bias V_{gs} (18).

We extract drain-source capacitance (C_{gs}), gate–drain capacitance (C_{gd}) and drain-source capacitance (C_{ds}) from multibias [S]-parameters measurements; the values and model of capacitances are plotted in Fig. 2 and the value of each parameter is presented in Table 1. In the choice of capacitance values, we took particular care in accurate fit in the two mains areas defined by ON- and OFF-mode regimes:

$$C_{ds} = \frac{C_{ds1} - C_{dso}}{2}[1 + \tanh(a_{ds}(V_{cor_{ds}} + V_{ds} - V_{gs}))]. \quad (18)$$

We notice that for power amplifiers application, we can keep a fixed value of the drain source capacitance.

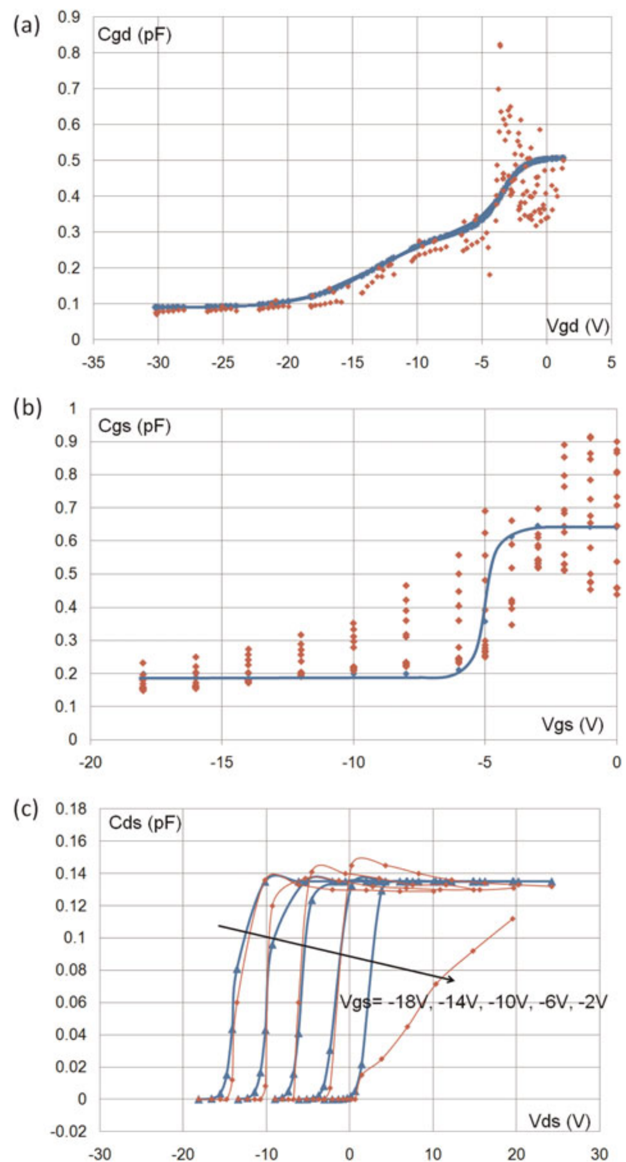

Fig. 2. (a) Gate–drain capacitance versus gate–drain voltage, plots: extracted values of C_{gd}, solid line: model values; (b) gate–source capacitance versus gate source voltage, plots: extracted values of C_{gs}, solid line: model values; (c) drain–source capacitance versus drain–source voltage, diamonds: extracted values of C_{gd} for $V_{gs} = -18$ V to $V_{gs} = -2$ V, thick line and triangles: model values.

III. VERIFICATION OF THE PROPOSED MODEL FOR SWITCH APPLICATIONS

In order to validate the model, several measurements have been done on FET transistors. The first validation is done by comparing PIV measurements (with 400ns pulse width) of 8 × 75 × 0.25 mm GaN HEMT processed at Alcatel-Thales 3-5lab and its modeled IV characteristic. (cf. fig. 3). The quiescent bias-point chosen here is $V_{gso} = 0$ V and $V_{dso} = 0$ V; then the traps states are set by the instantaneous voltage levels (the I–V curves obtained with this measurement configuration are hence the ones to be modeled if trapping subcircuit are added). Fig. 4 shows a good correlation obtained by using the proposed formulation. The values of the parameters are given in Tables 2 and 3.

The partial derivatives of the current are also shown (here defined as $g_m = \partial I_{ds}/\partial V_{gs}$ and $g_d = \partial I_{ds}/\partial V_{ds}$ whatever the sign

Table 1. Values of the parameters of equations of C_{gs}, C_{ds}, I_{gd} for the 8 × 75 μm GaN HEMT.

Capacitances parameters values					
C_{gdo}(pF)	C_{gd1}(pF)	C_{gd2}(pF)	a_{gd}	b_{gd}	Vm_{gd}(V)
0.09	0.28	−0.23	0.6	0.18	3.5
Vp_{gd}(V)	C_{gso}(pF)	C_{gs1}(pF)	C_{gs2}(pF)	a_{gs}	b_{gs}
13	0.2	0.65	0.01	1.5	0.6
Vm_{gs}(V)	V_{pgs}(V)	C_{dgso}(pF)	C_{ds1}(pF)	a_{ds}	$Vcor$(V)
4.8	2	0	0.135	1	−4.2

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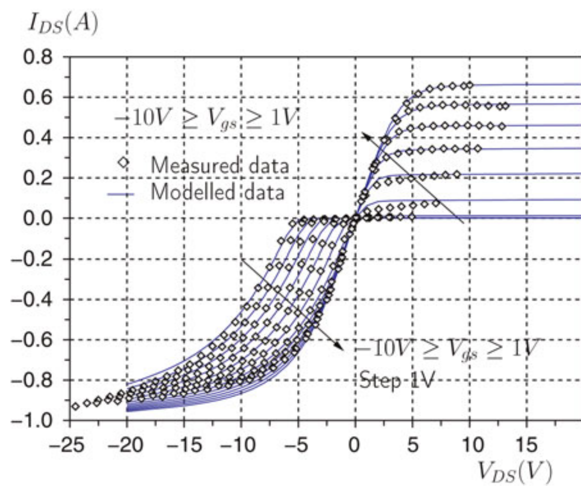

Fig. 3. Comparison between the measured/modeled pulsed $I_{gs}(V_{ds})$ of a 8 × 75 μm GaN HEMT, V_{gs} is stepped from −1 to +1.5 V (squares: measurements, black solid lines: model, black dashed lines: best fit with classical equations).

of V_{ds}): Fig. 6 shows the output conductance for $V_{qs} = -10$, −7, −1 and 1 V, and Fig. 7 the transconductance, its first- and second-order derivatives, for different values of V_{ds} (−1, 1, and 10 V). We took particular care in accurately modeling the transconductance close to the pinch-off, which is important to fit the low-level gain in class B amplifiers for example.

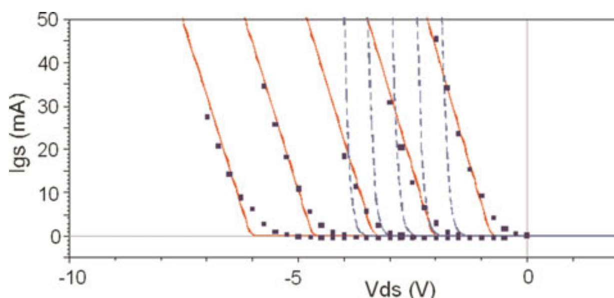

Fig. 4. Comparison between the measured/modeled pulsed $I_{gs}(V_{ds})$ of a 8 × 75 μm GaN HEMT, V_{gs} is stepped from −1 to +1.5 V (squares: measurements, black solid lines: model, black dashed lines: best fit with classical equations).

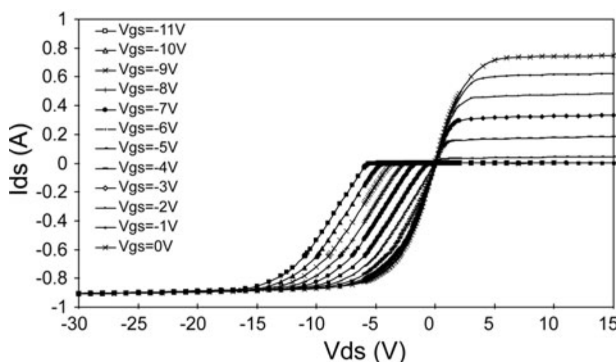

Fig. 5. Physical simulation realized; thanks to Atlas Silvaco show the current saturation for highly negative values of V_{ds}, which is hard to measure without degrading the device.

Table 2. Values of the parameters of equations of the diodes for the 8 × 75 μm GaN HEMT.

Main current source parameters					
I_{dss}	Vp_0	P	W_{neg}	W_{pos}	A_{neg}
0.98	5.07	0.002	0	0.91	0.01
A_{pos}	V_{knee}	S_{neg}	$gmvp$	S_{satn}	V_{satn}
0.22	3.98	53	0.1	0.33	0.49
S_{sat1p}	V_{sat2p}	V_{sat2p}	V_{sat2p}	α_{trval}	N
1.09	−2.1	0.3	2	1	1.2

Table 3. Values of the parameters of equations of the diodes for the 8 × 75 μm GaN HEMT.

Diodes parameters					
I_{sgd}	N_{gd}	α_{gs}	V_{tgd}	I_{sgs}	N_{gs}
2×10^{-29}	2.67	−2.14	0.77	1.3×10^{-27}	1.39

IV. BREAKDOWN MODEL

The breakdown is modeled for both positive and negative values of V_{ds}. However, measuring it on GaN HEMTs is a quite difficult task, as it often leads to its destruction. We used here the drain current injection method proposed in [10] to determine the breakdown voltages in this case, and approximately obtained $BV_{ds} = -65$ and +95 V. The derived breakdown model is simple, but useful to know the maximum power the transistor can sustain in the OFF regime, for which power injection leads to a large voltage swing.

For the positive breakdown, a current source I_{avdg} is plugged between the gate and the drain, with a current value having an exponential form

$$I_{avdg} = I_{savdg}\, e^{\alpha_{dg} \cdot V_{ds}}. \qquad (19)$$

For the negative breakdown, a current source I_{avgs} is plugged between the gate and the source:

$$I_{avgs} = I_{savgs}\, e^{\alpha_{gs} \cdot (-V_{ds})}. \qquad (20)$$

The parameters of these models are given in the Table 4.

The impact of the breakdown models on the $I_{ds}(V_{ds})$ curves is presented deeper in detail in [11]. We note that for negative values of V_{ds}, the current saturates before the breakdown (this saturation is set by the parameters S_{satn} and V_{satn}. This saturation is difficult to measure as it leads, in most of the cases, to the destruction of devices, but physical simulations performed

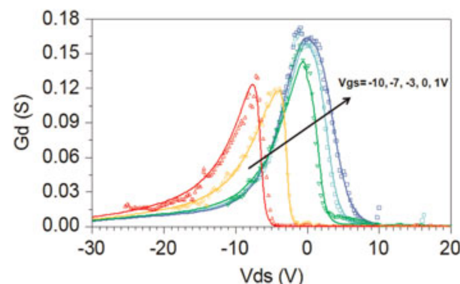

Fig. 6. Fit of the pulsed g_d versus V_{ds} measured curves of a 8 × 75 μm GaN HEMT, $V_{gs} = -10$, −7, −3, 0 and +1 V (symbols: measurements, solid lines: model).

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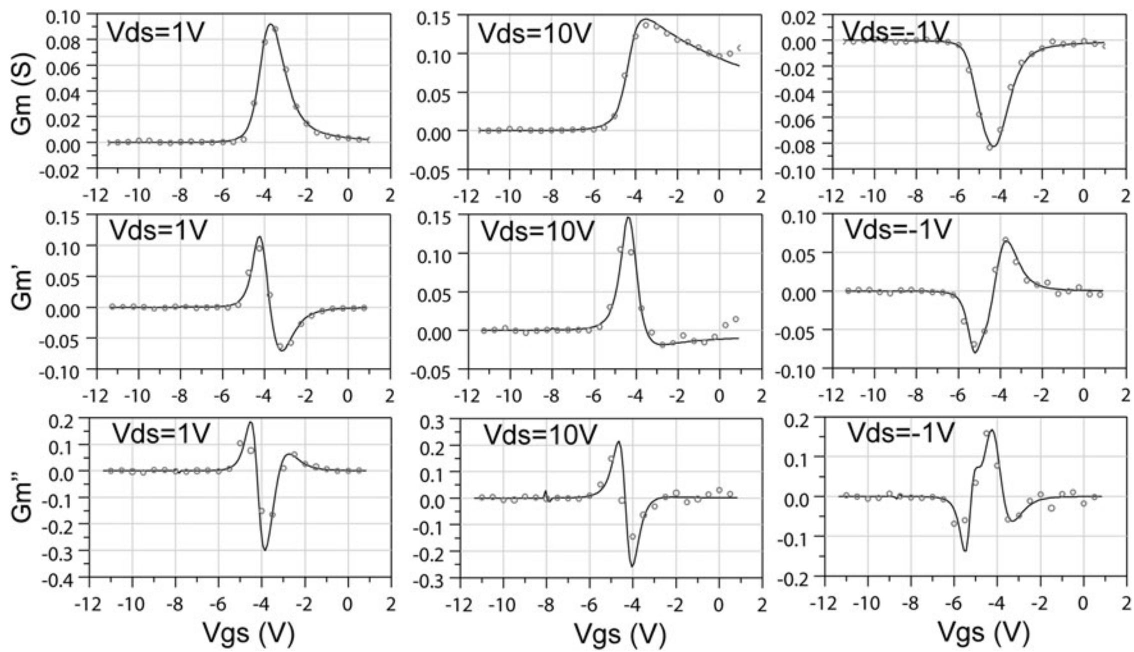

Fig. 7. Fit of the pulsed g_m versus V_{gs} measured curves of a 8 × 75 μm GaN HEMT, for different V_{ds}: −1, 1 and 10 V (symbols: measurements, solid lines: model).

with Atlas Silvaco highlight this phenomenon well in Fig. 5 (the modeled device had a slightly different epitaxy and technology as the measured one).

V. VALIDATION ON [S]-PARAMETERS

The accuracy of the model in the RF frequency range was checked through [S]-parameters measurements in the various working regimes of the transistor. Its small signal model was derived from the previous nonlinear *I–V* model, and extrinsic RF parameters were extracted and then kept constant over the whole set of bias points. Comparisons between modeled and measured [S]-parameters are provided in Fig. 8(a) and 8(b). These points correspond to the nonlinear working limits of the transistor in the OFF and ON regimes. It has to be noted that the model is able to accurately represent the [S]-parameters variations versus the bias values and then will be very useful for the design of RF switch applications.

VI. VALIDATION ON LARGE SIGNAL RF DRIVE AND TIME DOMAIN WAVEFORMS MEASUREMENTS

A) Bench presentation

To validate the model in switch applications we used a large signal time domain bench, including a large signal network

Table 4. Values of the parameters of the equations of the positive and negative breakdown for the 8 × 75 μ m GaN HEMT.

Breakdown generators			
I_{savdg}	α_{dg}	I_{savgs}	α_{gs}
3×10^{-6}	0.12	3×10^{-6}	0.17

analyzer (LSNA) as described in Fig. 9. The bench allows a reconstruction of temporal waveforms; thanks to the acquisition of harmonics and their phase relation, which is made possible due to measurement coupling probes located as close as possible to the measurement terminal [12].

The LSNA subsampling process of CW large signals acts in the same way as that of a stroboscope. It allows us, in a one-shot measurement, to acquire both the fundamental and harmonic frequencies data for all the incident and reflected waves [13]; thanks to the rigorous calibration algorithms, the time domain current, and voltages slopes versus time or the load cycles can be drawn at the reference planes.

B) Setup and measurement results

The load line cycle form, for the switch, depends on the ON- or OFF-state of the device. To see the time domain waveforms of this phenomenon, the experiment consists in injecting the RF power by the Drain access of the device with a quiescent bias of 0 V for all the measurements. Several measurements were performed for gate voltages ranging from $V_{gs} = -15$ V to 0 V and the results obtained for two cases, respectively, ON-switch state and OFF-switch state, are presented here. The fundamental RF frequency is set at 4 GHz. Although the configuration of the bench allows to set-up the impedances at the harmonics 2 and 3, we chose to focus mainly on the fundamental and then applied a complex load; thanks to the tuner on the gate access whose value is $Z_{gate} = 50 - j70$. It must be noted that the terminal impedance at the gate terminal plays an important role in the behavior of the switch. Due to the mounting of the transistors in common source, only parallel configuration of the switch was investigated in this experiment. However, the developed model can be used in a three-terminal configuration. The load line cycle in the ON-state switch ($V_{gs} = 0$ V) is plotted in Fig. 10 in linear working regime, this measurement is plotted with results

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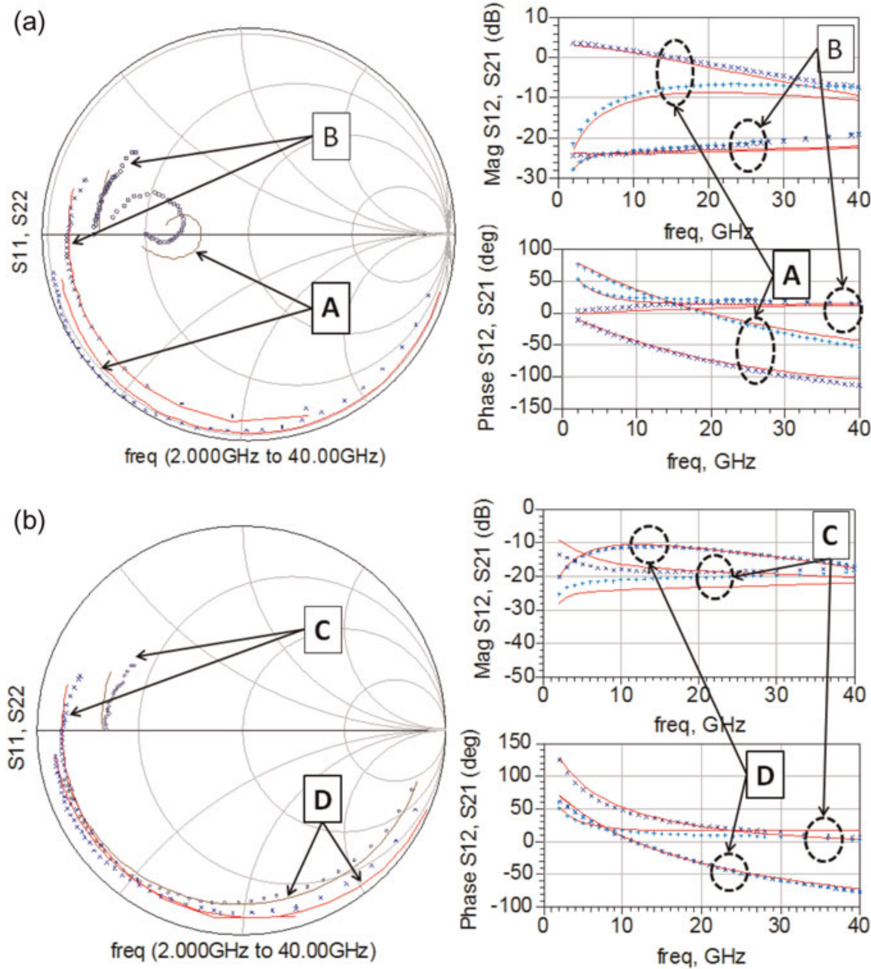

Fig. 8. Comparison between measured (symbols) and modeled (lines) of [S]-parameters for a 8 × 75 μm GaN HEMT, at different biases points: (a) For negative V_{ds} bias A: $V_{gs} = -18$ V, $V_{ds} = -14$ V; bias B: $V_{gs} = 0$ V, $V_{ds} = -2$ V. (b) For positive V_{ds} biases C: $V_{gs} = -18$ V, $V_{ds} = 16$ V; bias D: $V_{gs} = 0$ V, $V_{ds} = 3$ V.

given by the simulation at the same input power level than measured in the DUT plane ($P_{avs} = 34.2$ dBm), showing good accuracy of the model.

The load line cycle in the OFF-state of the switch ($V_{gs} = -13$ V) was measured for two regimes: one linear corresponding to an available power $P_{avs} = 23.8$ dBm on drain access, and the other in a nonlinear regime corresponding to $P_{avs} = 34.9$ dBm. The measured load cycles were compared to the simulated ones. The comparison was performed in the reference plane corresponding to the extrinsic access of the switch. The comparison is shown in Fig. 11 and time domain waveforms of current and voltage are given in Fig. 12.

The good behavior of the model for nonlinear power applications was demonstrated here. We notice that in the nonlinear OFF regime the load line does not follow the I–V characteristic, i.e. no negative current appears. This is due to a nonlinear shift of the quiescent drain voltage which is very sensitive to the impedance at the gate terminal. Having assessed the nonlinear model in the ON and OFF states, an evaluation of the insertion losses and isolation due to the device versus the injected RF

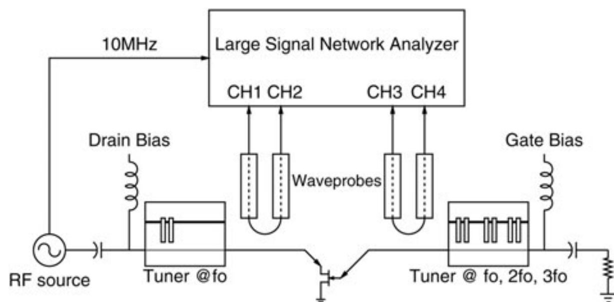

Fig. 9. Scheme of time domain load-pull bench in measurement condition with drain access excitation.

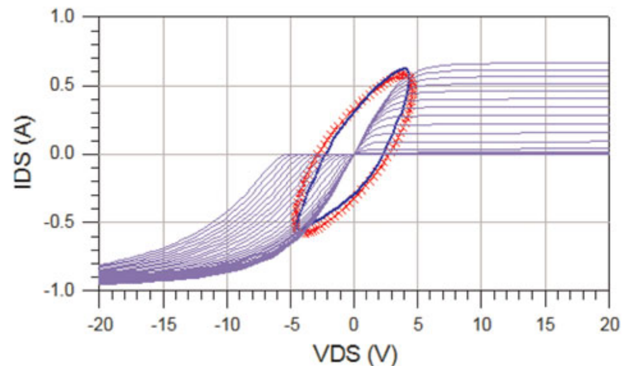

Fig. 10. Extrinsic load line for $V_{gs} = 0$ V for an available power 34.2 dBm, measurement crosses, simulation curves.

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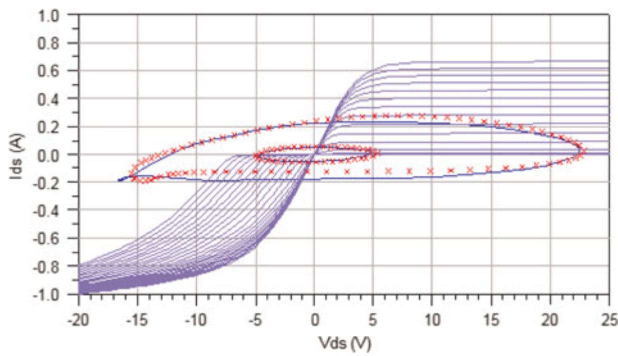

Fig. 11. Extrinsic load lines for $V_{gs} = -13$ V for an available power $P_{avs} =$ 23.8 dBm and an available power $P_{avs} = 34.9$ dBm, measurements are plotted in crosses, simulations appear in solid line.

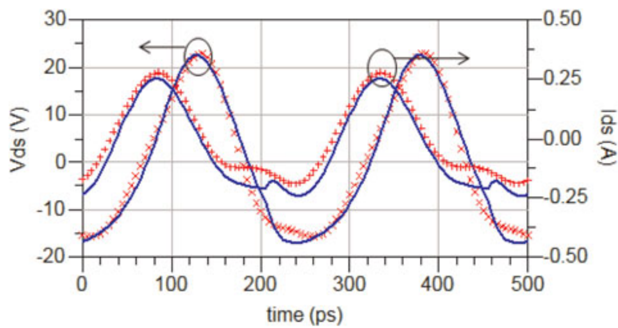

Fig. 12. Drain source voltage and current waveforms for $V_{gs} = -13$ V for an available power 34.9 dBm, measurements are plotted in crosses, simulations appear in solid lines.

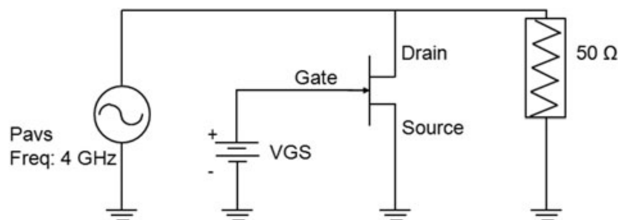

Fig. 13. Simulation of the performances of the parallel switch in the ON and OFF regimes. Insertion loss is defined as $P_{out}-P_{in}$ when the transistor is switched OFF while the isolation is defined as $P_{out}-P_{in}$ when the transistor is switched ON.

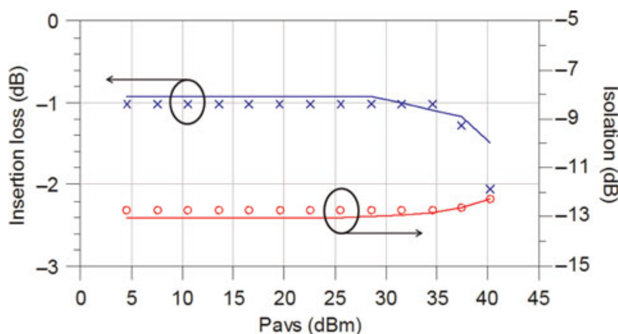

Fig. 14. Comparisons of isolation (transistor ON) between simulation in red and measurements in circles for $V_{gs} = 0$ V, and insertion losses (transistor OFF) between the simulation blue solid line and measurements in crosses for $V_{gs} = -15$ V in blue versus the available power.

power can be foreseen. Thus, the simulations were performed at 4 GHz with the transistor mounted as shown in Fig. 13. Here the switch is in a shunt configuration and the transistor is switched ON for measuring the isolation while it is switched OFF to estimate the insertion losses. This configuration is often encountered in applications such as single pole double throw (SPDT) structure in transmission/reception modules. These simulation results are plotted in Fig. 14 and they are compared to measurement results obtained for two DC gate-source voltages, $V_{gs} = -15$ and 0 V.

VII. CONCLUSIONS

The model proposed allows reproducing the *I–V* characteristics of FETs for positive and negative values of the drain voltage, and then, by adding the breakdown effects, allow reproducing the whole *I–V* characteristics. The formulation for the main part is based on smoothed asymptotic functions. It needs a reduced number of parameters, it is well suited for convergence, and has continuous high-order derivatives. This formulation can be used for modeling transistors aimed at different applications, reducing then the modeling process duration when the same topology of transistor is used in these applications.

A nonlinear model for switch applications was developed, using the *I–V* formulation, and adding nonlinear capacitances extracted from multibias [S]-parameters. We showed a good correlation between measured and modeled [S]-parameters over several bias points, corresponding approximately to the limits of the RF swings in its both working regimes. We also complete the study with time domain load-pull measurements which allowed us to conclude with a good agreement and a good CAD behavior on both linear and nonlinear functioning. This shows the interest of the *I–V* model, and subcircuit modeling, for designing such RF functions.

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Guillaume Callet was born in Arles, France 1983. He obtained an engineering degree from ENSEA (Ecole Nationale Suprieure d' Electronique et de ses Applications) in 2008 and is currently working toward a Ph.D. degree from Limoges University, in the common laboratory between Xlim and Alcatel-Thales III–V Lab, MITIC. He works on the development of AlInN/GaN technology, particularly on the modeling of power devices.

Jad Faraj was born in Lebanon in 1983. He received a Master Research degree in 2007 from the University of Limoges, France. He is presently a Ph.D. student at the (Xlim) laboratory, with the Non Linear Electronic Circuits and Sub-Systems team, University of Limoges. His research topic is pulsed time domain load-pull characterization of microwave power transistors and the developing of RF instrumentations for large signal measurements.

Olivier Jardel was born in Poitiers, France, in November 1981. He received an engineering degree from Aix-Marseille I University, in 2004, and the Ph.D. degree from Limoges University in April 2008, in the common laboratory MITIC between XLIM and Alcatel-Thales 3–5 lab. He is currently a research Engineer at Alcatel-Thales 3–5 lab, and is working on the development of the new AlInN/GaN HEMT technology, on transistor modeling, and on the design of high-power amplifiers.

Christophe Charbonniaud was born in Limoges, France, in 1972. He received a Master Research degree from Universit de Limoges, France, in 2001, and Ph.D. degree from the Research Institute on Microwave and Optical Communications XLIM, Université de Limoges, in 2005. He is a co-founder of AMCAD Engineering, France, where he serves as the modeling team manager of amplifiers.

Jean-Claude Jacquet received the Engineer degree from the Ecole Supérieure d'Optique, Orsay, France, in 1990. He subsequently joined the Central Research Laboratory of Thales, as a Research Staff Member, where he was involved with spintronic devices. He focused his efforts on the giant magnetoresistive effect and found a new physical effect called the magnetorefractive effect. Since 1999, he has been involved with GaInP HBT and GaN HEMT microwave power devices. He is currently in charge of thermal management and of the physical modeling aspects on GaN HEMT with the Alcatel/Thales III–V Laboratory.

Tibault Reveyrand was born in Paris, France. He received a Ph.D. degree from Université de Limoges, Limoges, France, in 2002. From 2002 to 2004, he was Post-Doctoral Scientist with the Centre National d'Etudes Spatiales (CNES) (French Space Agency). In 2005, he became a Contractual Engineer with the Centre National de la Recherche Scientifique (CNRS), XLIM, Limoges, France. His main research interests include the characterization and modeling of RF and microwave nonlinear components.

Erwan Morvan graduated in material physics and semiconductor devices at National Institute for Applied Science (INSA) in Lyon (France). He was a Ph.D. student at National Center for Microelectronics in Barcelona (CNM) from 1995 to 1999. He worked in the field of device and technology simulation. He developed an ion implantation simulator for Silicon Carbide (SiC) crystal. He obtained the Ph.D. degree in electronics from INSA Lyon in 1999. In 2000, he joined the Corporate Laboratory of Thomson CSF (LCR), now called Thales Research and Technology (TRT). He was involved in SiC MESFET design, technology and characterization as a research engineer from 2000 to

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2003. He is now involved in AlGaN/GaN and InAlN/GaN device technology research and development.

Stéphane Piotrowicz was born in France 1971. He received a Ph.D. degree in Electronics from the University of Lille in 1999. He Joined the Thales Research Center and worked on the design of Hybrid and MMIC power amplifiers on the InGaP/GaAs HBT technology for Radar and Space Applications. He currently works on the development of AlGaN/GaN technology at Alcatel-Thales III–V Lab. He is in-charge of hybrid and MMIC demonstrators for T/R modules as power switches, power amplifiers and low noise amplifiers.

Jean-Pierre Teyssier was born in 1963 in Brive, France. Since 1990, he works at the IRCOM/XLIM lab of the University of Limoges, France, in the group of Pr Raymond Quéré. He has presented his Ph.D. Thesis in 1994, the subject was about pulsed $I(V)$ and pulsed S-Parameters for the nonlinear characterization of microwave active devices. Till now, he is involved in the design of measurement systems and instrumentation for microwave nonlinear investigations, with an emphasis on time domain pulsed large signal characterization of transistors. Since many years, Jean-Pierre Teyssier and his students are frequent contributors of ARFTG papers, he is now a member of ARFTG ExCom, responsible for workshop organization.

R. Quéré (Fellow IEEE) received the electrical engineering degree from ENSEEIHT Toulouse, France in 1976 and the French agrégation in applied physics in 1978. After a teaching period of 8 years for undergraduate students, he prepared and earned a Ph.D. degree (with honors) from University of Limoges in 1989. In 1992, he was appointed as full professor at the University of Limoges. Since 1998, he leads the nonlinear high-frequency devices, circuits and systems research department at XLIM-CNRS laboratory. This department gathers 70 permanent and non-permanent researchers and is involved in high-frequency devices circuits and systems design. His main field of interest is in the area of nonlinear device and circuit modeling with a particular emphasis on nonlinear phenomena such as stability in power amplifiers. He advises more than 30 Ph.D. students and he authors or co-authors more than 100 journal articles or communications in international conferences such as IMS/MTT, EuMW. He was the co-author of the book "Nonlinear Stability of Nonlinear Microwave Circuits". Moreover, he is involved in a number of technical program committees and serves as a reviewer for several journals such as Electronic Letters, IEEE transactions on MTT. In 2005, he was appointed as the general Chairman of the European Microwave Week in Paris.

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