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RESEARCH PAPER

Large-signal characterization of DDR silicon IMPATTs operating up to 0.5 THz

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Large-signal (L-S) characterization of double-drift region (DDR) impact avalanche transit time (IMPATT) devices based on silicon designed to operate at different millimeter-wave (mm-wave) and terahertz (THz) frequencies up to 0.5 THz is carried out in this paper using an L-S simulation method developed by the authors based on non-sinusoidal voltage excitation (NSVE) model. L-S simulation results show that the device is capable of delivering peak RF power of 657.64 mW with 8.25% conversion efficiency at 94 GHz for 50% voltage modulation; whereas RF power output and efficiency reduce to 89.61 mW and 2.22% respectively at 0.5 THz for same voltage modulation. Effect of parasitic series resistance on the L-S properties of DDR Si IMPATTs is also investigated, which shows that the decrease in RF power output and conversion efficiency of the device due to series resistance is more pronounced at higher frequencies especially at the THz regime. The NSVE L-S simulation results are compared with well established double-iterative field maximum (DEFM) small-signal (S-S) simulation results and finally both are compared with the experimental results. The comparative study shows that the proposed NSVE L-S simulation results are in closer agreement with experimental results as compared to those of DEFM S-S simulation.

Keywords: Avalanche response time, DDR silicon IMPATTs, Large-signal simulation, Millimeter-wave, Thermal design, Terahertz regime

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I. INTRODUCTION

Impact avalanche transit time (IMPATT) devices have already emerged as high power, high efficiency solid-state sources for both microwave (3–30 GHz) and millimeter-wave (mm-wave) (30–300 GHz) frequency bands [1–3]. Several small-signal (S-S) analysis and simulation methodologies of IMPATT devices have already provided a considerable insight into the IMPATT operation [4–6]. Several authors [7–12] investigated the mm-wave performance of double-drift region (DDR) Si IMPATT devices operating at different mm-wave atmospheric window frequencies following an S-S simulation technique based on Gummel–Blue approach [13]. However, several important properties of IMPATT oscillators such as dependence of RF power output, DC to RF conversion efficiency, and frequency tuning of the oscillators on diode parameters, bias current, and RF circuitry cannot be precisely obtained from S-S analysis. Thus, large-signal (L-S) analysis of IMPATT devices is necessary to acquire the above-mentioned properties. Evans and Haddad [14] presented an L-S model of IMPATT oscillator and RF power output, efficiency of the oscillator was obtained from a closed-form solution of nonlinear equations describing a Read-type (p–n–v–n) IMPATT device in 1968. They assumed much shorter transit time of the charge carriers through the drift region as compared to the period of RF oscillation to obtain the closed-form solution. Pioneering work on L-S analysis of Read-type silicon IMPATT oscillator is carried out by Scharfetter and Gummel [15]. They obtained a self-consistent numerical solution for equations describing carrier transport, carrier generation, and space-charge balance and presented the theoretical calculations of L-S admittance and efficiency achievable in a silicon Read-type IMPATT diode. Gupta and Lomax [16] followed a current-excited L-S analysis along with circuit implementation in 1973. They assumed a sinusoidal current flowing through the device and obtained corresponding voltage response to calculate device impedance.

In the present paper, the authors have made an attempt to obtain the upper cut-off frequency limit of DDR Si IMPATTs through an avalanche response time based simulation approach [17–20]. An L-S simulation technique based on non-sinusoidal voltage excitation (NSVE) model [21–23] is developed and simulation is carried out to study L-S characteristics of DDR IMPATTs based on Si designed to operate at different mm-wave and terahertz (THz) frequencies up to the limiting frequency of IMPATT operation for DDR Si IMPATTs obtained from avalanche response time based simulation, i.e. up to 0.5 THz. The effect of parasitic series resistance on L-S properties of DDR Si IMPATTs is also

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investigated, which shows that the decrease in RF power output and conversion efficiency of the device due to series resistance is more prominent at higher frequencies. The NSVE L-S simulation results are compared with well-established double-iterative field maximum (DEFM) S-S simulation results and finally both are compared with the experimental results to cross check the validity of the proposed method.

II. L-S SIMULATION TECHNIQUE

One-dimensional model of a reverse biased n^+–n–p–p^+ structure shown in Fig. 1 is used for the L-S simulation of DDR IMPATT device because of the physical phenomena taking place in the semiconductor bulk along the symmetry axis of the mesa structure of IMPATT devices. The fundamental time- and space-dependent device equations, such as Poisson's equation (equation (1)), continuity equations (equations (2) and (3)) and current density equations (equations (4) and (5)) involving mobile space charge in depletion layer are simultaneously solved under L-S conditions with appropriate boundary conditions by using a DEFM simulation method [21–23]. The fundamental device equations are given by

$$\frac{d\xi(x,t)}{dx} = \frac{q}{\varepsilon_s}(N_D - N_A + p(x,t) - n(x,t)), \tag{1}$$

$$q\frac{\partial p(x,t)}{\partial t} = -\frac{\partial J_p(x,t)}{\partial x} + (\alpha_n(x,t)J_n(x,t) + \alpha_p(x,t)J_p(x,t)), \tag{2}$$

$$q\frac{\partial n(x,t)}{\partial t} = \frac{\partial J_n(x,t)}{\partial x} + (\alpha_n(x,t)J_n(x,t) + \alpha_p(x,t)J_p(x,t)), \tag{3}$$

$$J_p(x,t) = qp(x,t)v_p(x,t) - qD_P\left(\frac{\partial p(x,t)}{\partial x}\right), \tag{4}$$

$$J_n(x,t) = qn(x,t)v_n(x,t) + qD_n\left(\frac{\partial n(x,t)}{\partial x}\right), \tag{5}$$

where N_D and N_A are the donor and acceptor concentrations, $\alpha_n(x,t)$ and $\alpha_p(x,t)$ are the electron and hole ionization rates at the space point x at the instant t, $v_n(x,t)$ and $v_p(x,t)$ are the electron and hole drift velocities at x at the instant t, D_n and D_p are the electron and hole diffusion coefficients, $p(x,t)$ and $n(x,t)$ are respectively the electron and hole concentrations at x at the instant t, $\xi(x,t)$ is the electric field at x at the instant t, $J_n(x,t)$ and $J_p(x,t)$ are respectively the electron and hole components of bias current density ($J_o(t) = J_n(x,t) + J_p(x,t)$) at x at the instant t, q is the electric charge of an electron ($q = 1.6 \times 10^{-19}$ C), and ε_s is the permittivity of the semiconductor material. Boundary conditions are imposed at the contacts (i.e. n^+–n and p^+–p interfaces) by setting up appropriate restrictions in equations (1)–(5). The boundary conditions for the time varying electric field at depletion layer edges are given by [21–23]

$$\xi(-x_1,t) = 0 \quad \text{and} \quad \xi(+x_2,t) = 0. \tag{6}$$

Similarly, the boundary conditions for time varying normalized current density $P(x,t) = (J_p(x,t) - J_n(x,t))/J_o(t)$ at depletion layer edges, i.e. at $x = -x_1$ and $x = x_2$ are given by [21–23]

$$P(-x_1,t) = \left(\frac{2}{M_p(-x_1,t)} - 1\right) \quad \text{and}$$
$$P(+x_2,t) = \left(1 - \frac{2}{M_n(+x_2,t)}\right), \tag{7}$$

where $M_n(x_2,t)$ and $M_p(-x_1,t)$ are the electron and hole multiplication factors at depletion layer edges at instant t are given by

$$M_p(-x_1,t) = \frac{J_o(t)}{J_p(-x_1,t)} \quad \text{and}$$
$$M_n(+x_2,t) = \frac{J_o(t)}{J_n(+x_2,t)}. \tag{8}$$

The total diode voltage ($V_B(t)$) and avalanche zone voltage drop ($V_A(t)$) at a particular instant of time t are obtained from numerical integration of the field profile over the depletion layer and avalanche layer widths respectively as follows:

$$V_B(t) = \int_{-x_1}^{x_2} \xi(x,t)dx \quad \text{and} \quad V_A(t) = \int_{-x_{A1}}^{x_{A2}} \xi(x,t)dx. \tag{9}$$

DC values of peak electric field (ξ_p), breakdown voltage (V_B), and avalanche zone voltage (V_A) drop can be evaluated by taking the time averages of time varying peak electric field ($\xi_p(t)$), total diode voltage ($V_B(t)$), and avalanche zone voltage drop ($V_A(t)$) over a complete time period of steady-state oscillation ($T = 1/f$; where f is the fundamental frequency of steady-state oscillation). Thus, the DC values of the peak electric field (ξ_p), breakdown voltage (V_B), and avalanche zone voltage (V_A) are given by

$$\xi_p = \frac{1}{T}\int_o^T \xi_p(t)dt, \quad V_B = \frac{1}{T}\int_o^T V_B(t)dt \quad \text{and}$$
$$V_A = \frac{1}{T}\int_o^T V_A(t)dt. \tag{10}$$

The L-S simulation is carried out by considering the IMPATT device as a non-sinusoidal voltage driven source,

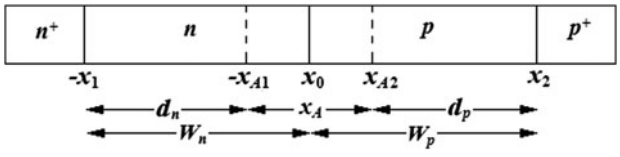

Fig. 1. One-dimensional model of DDR IMPATT device.

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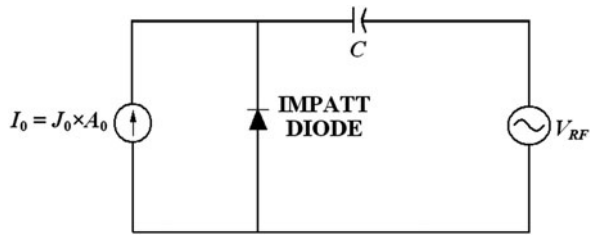

Fig. 2. Voltage driven IMPATT diode oscillator and associated circuit.

shown in Fig. 2. The input AC voltage is given as

$$V_{RF}(t) = V_B \sum_{p=1}^{n} m_x^p \sin(p\omega t). \tag{11}$$

The bias voltage is applied across the device through a coupling capacitor (C) to study the performance of the device at a given fundamental frequency ($f = \omega/2\pi$) with its n harmonics. The snapshots of electric field and current density profiles in the depletion layer of the IMPATT device are obtained from simultaneous numerical solutions of the basic device equations (equations (1)–(5)) subject to appropriate boundary conditions (equations (6) and (7)). The L-S simulation is carried out by taking 500 space steps and 100–150 time steps with sufficient accuracy.

The L-S program is run until the limit of one complete cycle (i.e. $0 \le \omega t \le 2\pi$) is reached. A current source provides the necessary bias current density. The RF voltage amplitude is V_{RF} and operating frequency is f. The waveforms associated with terminal current and voltage during a complete cycle of oscillation are Fourier analyzed to study the high-frequency characteristics of the device at various instants of time ($\omega t = 0$, $\pi/2$, π, $3\pi/2$, and 2π). The simulation is repeated at consecutive cycles to confirm the stability of oscillation. The simulated values of L-S negative conductance ($G(\omega)$), susceptance ($B(\omega)$), negative resistance ($Z_R(\omega)$), reactance ($Z_X(\omega)$), and Q-factor ($Q_p = -B_p/G_p$), where G_p and B_p are L-S peak negative conductance and susceptance at optimum frequency (f_p)) respectively are obtained from this study. The L-S values of negative conductance ($G(\omega)$) and susceptance ($B(\omega)$) (both are normalized by device junction area A_0: considering circular cross-sectional area of the device, $A_0 = \pi(D_0/2)^2$; where D_0 is the device effective junction diameter) are their effective values at the fundamental frequency of the voltage source, obtained by detailed Fourier analysis of the terminal current and voltage waveforms. The L-S device admittance is $Y_D(\omega) = [G(\omega) + jB(\omega)]A_0$. The L-S device impedance is given by

$$Z_D(\omega) = \frac{1}{Y_D(\omega)} = \frac{1}{[G(\omega) + jB(\omega)]A_0} = Z_R(\omega) + jZ_X(\omega). \tag{12}$$

The L-S negative resistance ($Z_R(\omega)$) and reactance ($Z_X(\omega)$) of the device are given by

$$Z_R(\omega) = \frac{G(\omega)}{[G(\omega)^2 + B(\omega)^2]A_0} \quad \text{and} \quad Z_X(\omega) = \frac{-B(\omega)}{[G(\omega)^2 + B(\omega)^2]A_0}. \tag{13}$$

If R_S is the series resistance associated with the device then the effective device impedance is modified to

$$Z_{D_{eff}}(\omega) = (Z_R(\omega) + R_S) + jZ_X(\omega). \tag{14}$$

The effective admittance of the device is now modified to

$$Y_{D_{eff}}(\omega) = \frac{1}{Z_{D_{eff}}(\omega)} = \left[G_{eff}(\omega) + jB_{eff}(\omega)\right]A_0. \tag{15}$$

Now, the effective L-S RF power output (P_{RF}) may be calculated as

$$P_{RF} = \frac{1}{2} V_{RF}^2 \left|\left(G_{eff}\right)_p\right| A_0, \tag{16}$$

where V_{RF} is the RF voltage, $|(G_{eff})_p|$ is the magnitude of L-S peak effective negative conductance normalized with respect to effective junction area (A_0). The effective L-S DC to RF conversion efficiency (η_L) of the device is obtained from the equation

$$\eta_L = \frac{P_{RF}}{P_{DC}}, \tag{17}$$

where $P_{DC} = J_0 V_B A_0$ is the input DC power and J_0 is the bias current density.

III. CALCULATION OF AVALANCHE RESPONSE TIME

The avalanche response time of DDR IMPATTs can be calculated from the knowledge of static spatial distribution of electron and hole ionization rates ($\alpha_n(x)$ versus x and $\alpha_p(x)$ versus x) obtained from DC simulation, saturated drift velocities of charge carriers (v_{sn} and v_{sp}). If τ_{An} and τ_{Ap} are avalanche response times initiated by electrons and holes, respectively, then these are expressed as [17–20]

$$\tau_{An} = \frac{1}{(v_{sn} + v_{sp})} \int_{-x_{A_1}}^{x_{A_2}} \exp\left[-\int_{-x_{A_1}}^{x} \left(\alpha_n(x) - \alpha_p(x)\right)dx'\right]dx, \tag{18}$$

$$\tau_{Ap} = \tau_{An} \exp\left[\int_{-x_{A_1}}^{x_{A_2}} \left(\alpha_n(x) - \alpha_p(x)\right)dx\right]. \tag{19}$$

When avalanche process is initiated by a mixture of electrons and holes then the corresponding response time τ_A is given by [17–20]

$$\tau_A = \tau_{An}\left\{(1-k) + k \cdot \exp\left[-\int_{-x_{A_1}}^{x_{A_2}} \left(\alpha_n(x) - \alpha_p(x)\right)dx\right]\right\}^{-1}, \tag{20}$$

where the parameter $k = J_{ps}/J_s$ and $(1-k) = J_{ns}/J_s$; $J_s = J_{ps} + J_{ns}$ is the total reverse saturation current of the device under dark condition. The expressions for thermally generated electron and hole reverse saturation currents (J_{ns}, J_{ps})

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are given by

$$J_{ns} = \left(\frac{qD_n n_i^2}{L_n N_A}\right) \quad \text{and} \quad J_{ps} = \left(\frac{qD_p n_i^2}{L_p N_D}\right), \tag{21}$$

where D_n and D_p are the diffusion coefficients of electrons and holes, respectively, L_n and L_p are the diffusion lengths of electrons and holes, respectively, n_i is the intrinsic carrier concentration, N_D and N_A are the donor and acceptor concentrations, respectively. Static spatial distribution of electron and hole ionization rates ($\alpha_n(x)$ and $\alpha_p(x)$) are obtained from the static or DC simulation of DDR IMPATTs. DC simulation is conducted by solving the basic device equations (equations (1)–(5)) simultaneously subject to proper boundary conditions (equations (6) and (7)) in static mode (time independent), i.e. by keeping the voltage modulation factor, $m_x = 0$.

IV. RESULTS AND DISCUSSION

A) Design of structural, doping, and other parameters

The active layer widths (W_n, W_p) and background doping concentrations (N_D, N_A) of DDR IMPATTs based on Si are initially chosen by using the transit time formula of Sze and Ryder [24]. The structural and doping parameters of the devices are designed for optimum performance at different mm-wave and THz frequencies (i.e. at design frequency, f_d) by using the method described in earlier papers [21–23]. The doping concentrations of n^+- and p^+-layers (N_{n+} and N_{p+}) are taken much higher, in the order of ~10^{25}/m^3 in the simulation. Structural and doping parameters of the designed Si-based DDR IMPATT devices are given in Table 1. The realistic field dependence of ionization rates (α_n, α_p) and drift velocities (v_n, v_p) of charge carriers and other material parameters such as bandgap (E_g), intrinsic carrier concentration (n_i), effective density of states of conduction and valance bands (N_c, N_v), diffusion coefficients (D_n, D_p), mobilities (μ_n, μ_p), and diffusion lengths (L_n, L_p) of Si (at realistic junction temperature of 500 K) are taken from the recently published experimental reports [25–28].

B) Static characteristics

Important static or DC parameters such as peak electric field (ξ_p), breakdown voltage (V_B), avalanche zone voltage (V_A), ratio of drift zone voltage drop to breakdown voltage (V_D/V_B), avalanche layer width (x_A), and ratio of avalanche zone width to total depletion layer width (x_A/W) of the designed DDR Si IMPATTs are obtained from the static simulation as mentioned earlier and are given in Table 2. Variations of ξ_p, V_B, and V_A with operating frequency of Si-based DDR IMPATTs are shown in Fig. 3. Table 2 shows that peak electric field (ξ_p) increases, while the breakdown voltage (V_B), avalanche zone voltage (V_A), and avalanche layer width (x_A) decrease in DDR IMPATTs based as the operating frequency increases. Peak electric field (ξ_p) increases from 6.03700 × 10^7–12.3120 × 10^7 V/m in Si IMPATTs as the operating frequency increases from 94 GHz to 0.5 THz. From the knowledge of avalanche zone voltage (V_A) and breakdown voltage (V_B), the drift zone voltage ($V_D = V_B - V_A$) of the device can be calculated. The ratio of drift zone voltage to breakdown voltage (V_D/V_B) decreases in the devices under consideration as the operating frequency increases. At higher frequencies the ratio V_D/V_B decreases sharply in Si DDRs ($V_D/V_B = 0.3346$ at 94 GHz; whereas $V_D/V_B = 0.1615$ at 0.5 THz). According to the semi-quantitative formula of DC to RF conversion efficiency ($\eta_L = (1/\pi) \times (V_D/V_B)$) [15] the DC to RF conversion efficiency (η_L) of IMPATT devices is directly proportional to the ratio V_D/V_B. Thus, the DC to RF conversion efficiency of Si IMPATTs is expected to decrease sharply with the increase of operating frequency.

The ratio of avalanche zone width to total drift layer width (x_A/W) in Si IMPATTs increases sharply at higher operating frequencies. Higher x_A/W indicates wider avalanche zone, which leads to higher avalanche voltage (V_A) and lower drift zone voltage (V_D). Lower V_D/V_B, lower is the conversion efficiency. Thus, the rapid widening of the avalanche region at higher operating frequencies is the primary cause of sharp decrease of conversion efficiency at higher operating frequencies in Si IMPATTs. In the case of Si DDRs, x_A/W is 44.62% at 94 GHz but it rises to 63.03% at 0.5 THz which causes sharp decrease of conversion efficiency at 0.5 THz frequency.

C) Thermal design

It is well known that the RF power output of IMPATT devices increases with the increase of junction temperature [1, 21]. Thus, the junction temperature of the device must be kept fixed well above the room temperature ($T_j > T_o = 300$ K) but below the burnout temperature (T_B) of the base material (here, T_B of the base material silicon is 575 K) by proper thermal design and appropriate heat sinking arrangement to avoid the thermal runway phenomenon and consequent device burnout. Generally, the junction temperatures of IMPATTs based on silicon are kept near 500 K for steady-state CW operation by using suitable heat sinks made of either metal (copper or silver) or type-IIA diamond [1, 29, 30]. However, a significant thermal advantage can be obtained by using a type-IIA diamond as heat sink material [1] due to its high thermal conductivity ($k_{dm} = 1200$ W/m/K [28] at 500 K). A simple method of designing heat sink has been proposed by Acharyya *et al.* [29] in 2011, where they

Table 1. Structural and doping parameters.

Base material	Serial number	f_d (GHz)	W_n (μm)	W_p (μm)	N_D (×10^{23} m^{-3})	N_A (×10^{23} m^{-3})	N_{n+}, N_{p+} (×10^{25} m^{-3})
Si	1	94	0.400	0.380	1.200	1.250	5.000
	2	140	0.280	0.245	1.800	2.100	5.000
	3	220	0.180	0.160	3.950	4.590	5.000
	4	300	0.132	0.112	6.000	7.300	5.000
	5	500	0.072	0.072	15.000	16.200	5.000

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Table 2. Static parameters.

Base material	Serial number	f_d (GHz)	J_o ($\times 10^8$ A/m^2)	ξ_p ($\times 10^7$ V/m)	V_B (V)	V_A (V)	V_D/V_B (%)	x_A (μm)	x_A/W (%)
Si	1	94	3.40	6.03700	24.36	16.21	33.46	0.348	44.62
	2	140	5.80	6.68700	19.02	13.64	28.66	0.270	51.42
	3	220	14.5	8.18700	13.99	10.40	25.66	0.172	49.86
	4	300	24.5	9.33700	11.71	9.25	21.01	0.136	55.74
	5	500	55.0	12.31200	9.35	7.84	16.15	0.089	63.03

have modeled the heat transfer in ordinary mesa structured DDR IMPATT diode on semi-infinite heat sink by using a lumped analytical representation of heat flow in both upper and bottom sides of the p–n junction. They showed that heat transfer mainly occurred from the p–n junction through the bottom side of the n^+–n–p–p^+ mesa structure (i.e. p-layer → p^+-layer → metal contacts (Ti, Au) → heat sink) during CW steady-state operation due to much smaller thermal resistance of the bottom side as compared to that of the upper side. Thus, the total effective thermal resistance of the device on the semi-infinite heat sink (θ_T) can be written as

$$\theta_T = (\theta_p + \theta_{p^+} + \theta_{Ti} + \theta_{Au}) + \theta_{HS}, \tag{22}$$

where θ_p, θ_{p+}, θ_{Ti}, θ_{Au} are the thermal resistances of p-, p^+-layers of the device, Ti, Au contact layers respectively, and θ_{HS} is the thermal resistance of the semi-infinite heal sink. The thermal resistance of p-epitaxial layer and Ti, Au contact layers can be written as

$$\theta_p = \left(\frac{4W_p}{\pi D_o{}^2 k_{Si}}\right), \quad \theta_{Ti} = \left(\frac{4W_{Ti}}{\pi D_{S-1}{}^2 k_{Ti}}\right) \quad \text{and}$$
$$\theta_{Au} = \left(\frac{4W_{Au}}{\pi D_{S-1}{}^2 k_{Au}}\right), \tag{23}$$

respectively, where W_p, W_{Ti}, and W_{Au} are the thicknesses of p-epitaxial layer and Ti, Au contact layers respectively, D_o is the junction diameter, D_{S-1} is the diameter of the device–heat sink interface (diameters of Ti, Au contact layers) and

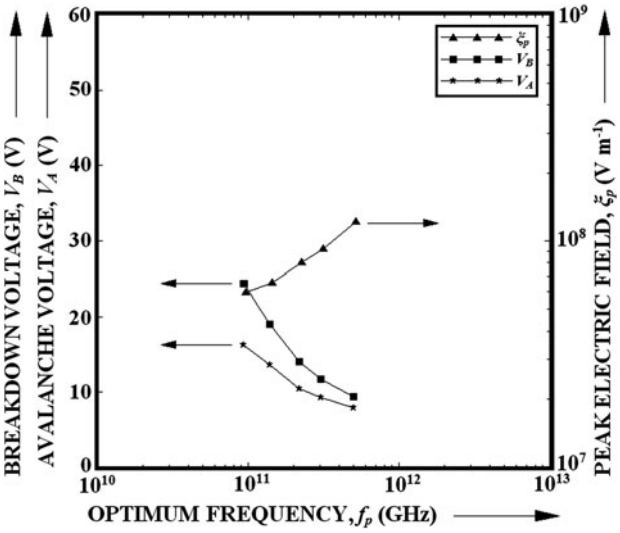

Fig. 3. Variations of breakdown voltage, avalanche voltage, and peak electric field with optimum frequency of DDR Si IMPATTs.

k_{Si}, k_{Ti}, and k_{Au} are the thermal conductivities of Si, Ti, and Au respectively ($k_{Si} = 150.00$ W/m/K, $k_{Ti} = 21.90$ W/m/K, $k_{Au} = 320.00$ W/m/K [31]). The mesa etched p^+-layer is considered to consist of a number of concentric cylindrical layers one below the other each having the same thickness (W_{p+}/S; where S is the number of cylinders) with increasing diameter from D_o to D_{S-1} as shown in Fig. 4. The expression of thermal resistance due to p^+-layer can be written as

$$\theta_{p+} = \left(\frac{4}{\pi k_{Si}}\right) \sum_{m=o}^{S-1} \left(\frac{W_{p+}}{S D_m^2}\right). \tag{24}$$

In the present calculation, the number of concentric cylindrical layers S is taken as 100 to achieve approximate tapered conical-shaped structure of p^+-layer with sufficient accuracy which is near approximation of mesa etched p^+-layer. Thickness of different layers (p-, p^+-layers of the device, Ti, and Au contact layers) and device–heat sink interface diameters (D_{S-1}) of DDR Si IMPATT operating at different mm-wave and THz frequencies are given in Table 3.

The thermal resistance of the heat sink having thickness L_H and diameter D_H can be written as

$$\theta_{HS} = \left(\frac{4L_H}{\pi D_H^2 k_{dm}}\right), \tag{25}$$

where k_{dm} is the thermal conductivity of heat sink material (type-IIA diamond). The junction temperature of the device in CW steady-state operation can be obtained from the following relation:

$$T_j = T_o + \left(\frac{\pi}{4}\right)(1 - \eta_L) J_o V_B D_o{}^2 \theta_T \tag{26}$$

where T_o is the ambient temperature ($T_o = 300$ K). The values of V_B and J_o are obtained from the DC simulation of DDR Si IMPATT device designed to operate at a particular frequency. The DC to RF conversion efficiency (η_L) of the device at that frequency is initially estimated from the NSVE L-S simulation presented in this paper (later in this paper). Now, if θ_T is known, then the junction temperature can be calculated from equation (26). However, in the present problem, T_j has to be kept near 500 K to get maximum RF power from the device avoiding the device burnout. Thus, the device junction diameter (D_o) and heat sink dimensions (L_H and D_H) have to be chosen appropriately keeping all other dimensions of the device fixed such that T_j remains nearly 500 K.

The flowchart of the method of obtaining D_o, L_H, and D_H is shown in Fig. 5. At first, the junction temperature (T_j) of the device design to operate at a particular frequency (f_d) is

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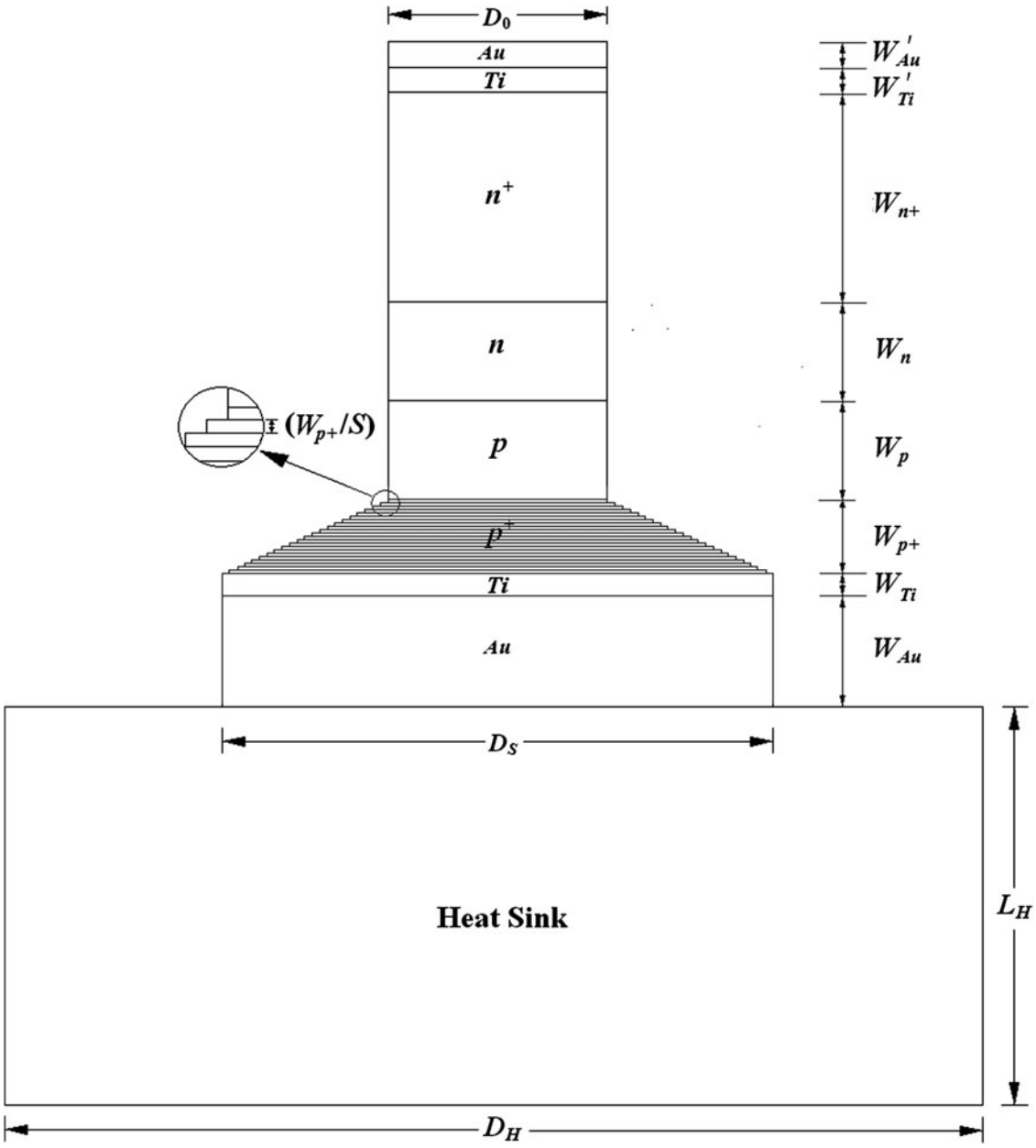

Fig. 4. Mesa structure of DDR IMPATT device on semi-infinite heat sink; the mesa etched p^+-layer is considered to consist of a number of concentric cylindrical layers one below the other each having the same thickness (W_{p+}/S; where S is the number of cylinders) with increasing diameter from D_o to D_{S-1}.

calculated from equation (26) by using the corresponding bias current density (J_o), breakdown voltage (V_B) obtained from DC simulation, initially estimated DC to RF conversion efficiency (η_L) from the NSVE L-S simulation, initially chosen junction diameter (D_o), and heat sink dimensions (L_H and D_H; where $D_H \gg D_o$, otherwise device-heat sink bonding is difficult to achieve). If the calculated T_j remains within the range of 480–520 K, then the D_o, L_H, and D_H values are accepted provided that $D_H \gg D_o$, otherwise D_o, L_H, and D_H values are modified accordingly (keeping $D_H \gg D_o$) and again T_j is calculated from equation (26). The process is repeated until appropriated D_o, L_H, and D_H values are obtained for which $480 \leq T_j \leq 520$. The finally estimated D_o, L_H, and D_H values, corresponding thermal resistance of the device ($\theta_D = \theta_p + \theta_{p+} + \theta_{Ti} + \theta_{Au}$), and total effective thermal resistance of the device on semi-infinite heat sinks ($\theta_T = \theta_D + \theta_{HS}$) designed to operate at different mm-wave and THz frequencies and corresponding junction temperatures (T_j) are given in Table 4.

D) Avalanche response times

Avalanche response times (τ_A) of DDR IMPATTs based on Si are calculated by equation (20). Spatial variations of ionization rates of electrons (α_n) and holes (α_p) for each device are obtained from the output of the static program and used to solve equations (18) and (20). Transit times (τ_T) associated with the DDR IMPATT devices based on Si operating at different mm-wave and THz frequencies are obtained from transit time formula of Sze and Ryder [24]. Figure 6 shows the variations of τ_A and τ_T with operating frequency in Si-based DDRs. DDR IMPATTs based on a particular semiconductor

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Table 3. Thickness of different layers and device–heat sink interface diameters.

Base material	Serial number	f_d (GHz)	W_p (μm)	W_{p+} (μm)	W_{Ti} (μm)	W_{Au} (μm)	D_{S-1} (μm)
Si	1	94	0.380	0.200	0.500	4.000	300.00
	2	140	0.245	0.150	0.300	3.000	200.00
	3	220	0.160	0.120	0.250	2.000	150.00
	4	300	0.112	0.100	0.150	1.500	100.00
	5	500	0.072	0.050	0.100	1.000	80.00

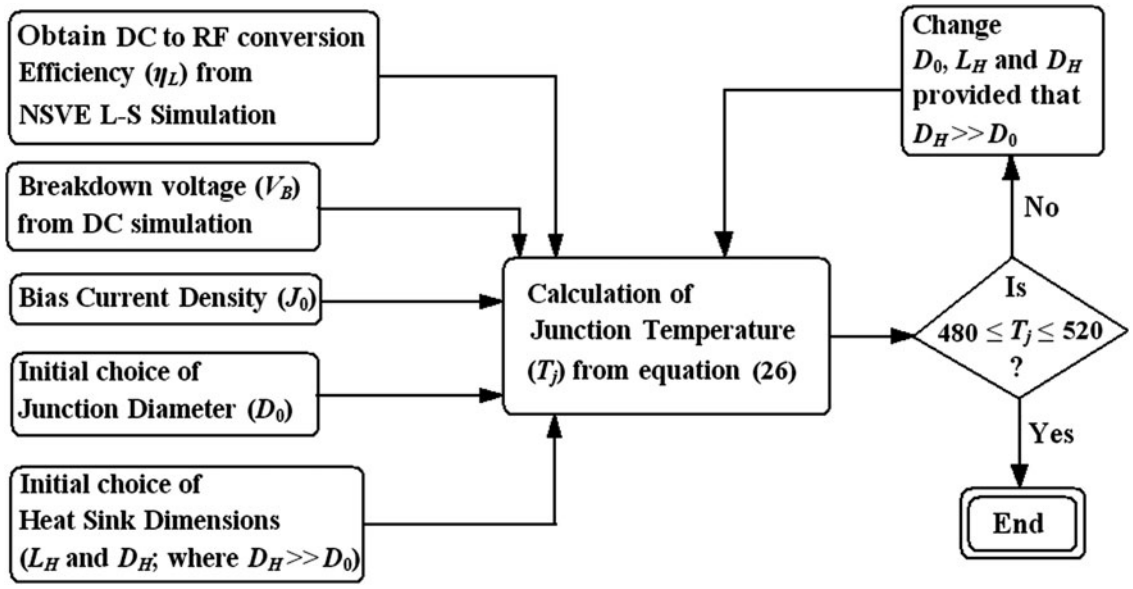

Fig. 5. Flowchart showing the method of obtaining D_o, L_H, and D_H.

can be operated at higher frequencies provided the avalanche response time (τ_A) is much lower than the transit time (τ_T) of carriers at the higher frequencies [17–20]. Avalanche response time (τ_A) of the device depends on saturated drift velocities and ionization rates of electron and holes (v_{sn}, v_{sp} and α_n, α_p, respectively) of the base semiconductor. Thus, the type of the base material determines the value of τ_A at a particular frequency. Figure 6 shows that the avalanche response time (τ_A) of Si DDRs becomes almost comparable to transit time (τ_T) as the operating frequency increases to 0.5 THz, which implies that above 0.5 THz, it is difficult to achieve IMPATT action in Si-based DDR IMPATTs. Thus, the highest operating frequency of Si DDRs is limited to 0.5 THz.

E) L-S characteristics

The important L-S parameters of Si-based DDR IMPATTs designed to operate at different mm-wave and THz frequencies such as peak optimum frequency (f_p), avalanche resonance frequency (f_a), peak negative conductance (G_p), corresponding susceptance (B_p), quality factor or Q-factor ($Q_p = -B_p/G_p$), negative resistance (Z_R), RF power output (P_{RF}), and L-S DC to RF conversion efficiency (η_L) for 50% voltage modulation are obtained from the L-S simulation assuming series resistance, $R_S = 0$ and those are listed in Table 5. The voltage modulation factor is taken as 50%, since it was earlier studied that the 94 GHz DDR Si IMPATT delivers maximum RF power when the voltage modulation factor is kept in the range of 50–60% [21–23]; which is also verified and confirmed for DDR Si IMPATTs operating at higher frequencies in the present study. Admittance characteristics or conductance–susceptance plots for 94, 140, 220, and 300 GHz Si DDR IMPATTs for 50% voltage modulation are shown in Fig. 7 while the same plots for 0.5 THz Si IMPATT are shown in Fig. 8. It is observed from Table 5, Figs 7, and 8 that the magnitudes of G_p and B_p increase with the increase of operating frequency in those devices. Avalanche resonance frequency (f_a) of the IMPATT device is the frequency at which the conductance of the

Table 4. Junction diameters, heat sink dimensions, thermal resistances, and junction temperatures of DDR Si IMPATTs designed to operate at different mm-wave and THz frequencies.

Base material	Serial number	f_d (GHz)	D_o (μm)	L_H (μm)	D_H (μm)	θ_D (K/W)	θ_T (K/W)	T_j (K)
Si	1	94	35.00	4000.00	400.00	0.5908	27.1166	498.25
	2	140	25.00	2700.00	286.00	0.8740	35.8976	482.38
	3	220	20.00	2300.00	262.00	1.1760	36.7272	523.15
	4	300	15.00	1800.00	218.00	1.7685	41.9558	505.46
	5	500	10.00	650.00	116.00	1.8018	53.0556	509.53

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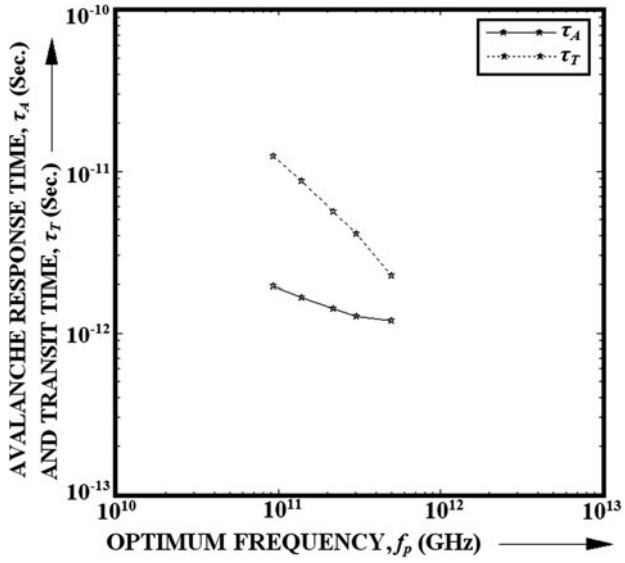

Fig. 6. Variations of avalanche response time and transit time with optimum frequency of DDR Si IMPATTs.

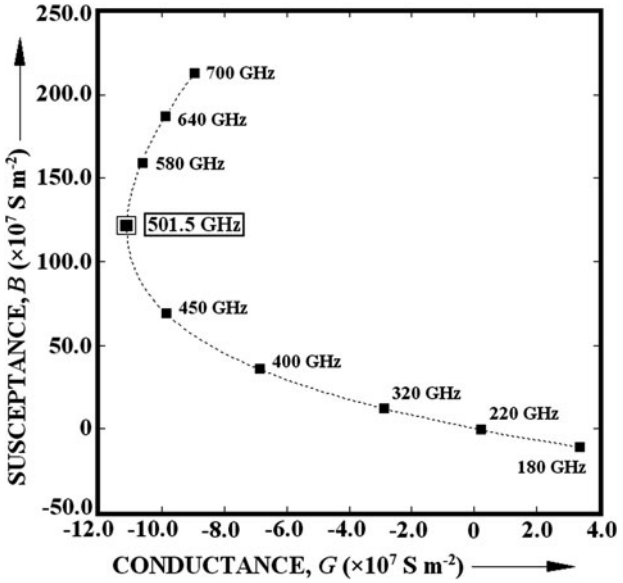

Fig. 8. Admittance characteristics of 0.5 THz DDR Si IMPATT.

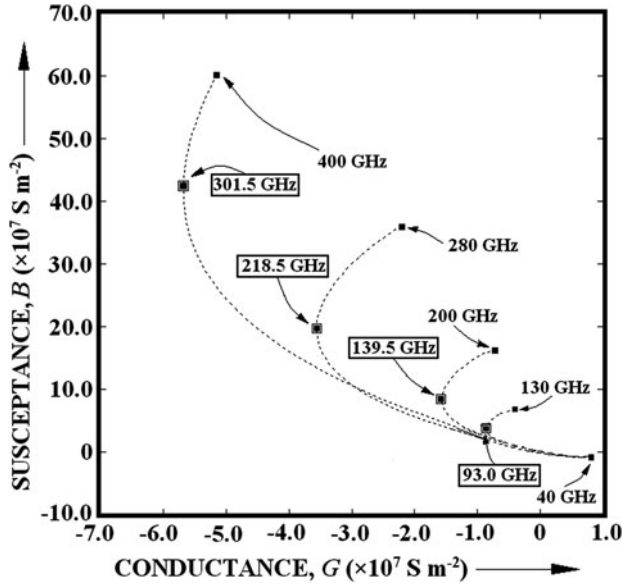

Fig. 7. Admittance characteristics of 94, 140, 220, and 300 GHz DDR Si IMPATTs.

device changes its sign from positive to negative. It can be observed from Table 5 that f_a increases sharply from 52.0 GHz to 196.7 GHz as the operating frequency increases from 94 GHz to 0.5 THz. Q-factor ($Q_p = -B_p/G_p$) of the device determines the growth rate of IMPATT oscillation. Lower Q-factor closer to one (i.e. $Q_p \approx 1$) suggests a higher oscillation growth rate. It is observed from Table 5 that the Q-factor of Si-based DDR IMPATTs increases from 4.17 to 11.62 as the operating frequency increases from 94 GHz to 0.5 THz. Thus, the oscillation growth rate degrades as the frequency of operation increases. It is also worth noting from Table 5 that the magnitude of negative resistance (Z_R) of Si IMPATTs decreases sharply with the operating frequency, which is the primary cause of sharp decrement of RF power output at higher operating frequencies.

F) Effect of parasitic series resistance

In an IMPATT oscillator the RF power should be efficiently transferred from the active region of the device to the external load. This can be ensured by matching the real part of device impedance to the real part of load impedance by using a matching network with low loss at the resonant frequency at which total reactance of the device–circuit combination is zero [32]. However, the power loss taking place in the inactive region of the device cannot be compensated for by the external circuitry. This loss should be minimized; otherwise it can severely degrade overall performance of the oscillator. The undepleted portion of the device contributes to positive series resistance and RF power is dissipated there as heat. The parasitic series resistance originates from the un-swept epitaxial layer, substrate layer, and contact layers of the

Table 5. L-S parameters ($R_S = 0$).

Base material	Serial number	f_p (GHz)	f_a (GHz)	G_p (× 10^7 S/m^2)	B_p (× 10^7 S/m^2)	$Q_p = -(B_p/G_p)$	Z_R/A_j (× 10^{-10} Ω/m^2)	P_{RF} (mW)	η_L (%)
Si	1	93.0	52.0	−0.9215	3.6758	3.99	−64.1683	657.64	8.25
	2	139.5	70.9	−1.5069	8.5124	5.65	−20.1643	334.49	6.18
	3	218.5	111.5	−3.8668	19.5416	5.05	−9.7443	297.20	4.66
	4	301.5	141.3	−5.7154	40.5807	7.10	−3.4031	173.12	3.41
	5	501.5	196.7	−10.4471	121.2923	11.62	−0.7045	89.61	2.22

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Table 6. RF power outputs, DC to RF conversion efficiencies, and junction temperatures for different values of R_S.

Serial number	f_d (GHz)	$R_S = 0\ \Omega$			$R_S = 0.2\ \Omega$			$R_S = 0.5\ \Omega$			$R_S = 0.8\ \Omega$		
		P_{RF} (mW)	η_L (%)	T_j (K)	P_{RF} (mW)	η_L (%)	T_j (K)	P_{RF} (mW)	η_L (%)	T_j (K)	P_{RF} (mW)	η_L (%)	T_j (K)
1	94	657.64	8.25	498.25	640.15	8.03	498.73	613.57	7.69	499.46	586.58	7.36	500.18
2	140	334.49	6.18	482.38	319.13	5.89	482.94	295.58	5.46	483.78	272.26	5.03	484.61
3	220	297.20	4.66	523.15	279.35	4.38	523.81	252.11	3.96	524.79	224.34	3.52	525.82
4	300	173.12	3.41	505.46	155.74	3.07	506.18	129.31	2.55	507.29	102.51	2.02	508.41
5	500	89.61	2.22	509.53	69.89	1.73	510.58	39.95	0.99	512.17	9.81	0.24	513.77

device. Since the negative resistance of mm-wave IMPATTs is in the range of a few ohms, positive series resistance is to be kept to a minimum possible value by appropriate design of the structural, doping, and bias current parameters of the device to obtain maximum RF power output from the device.

The RF power out, DC to RF conversion efficiency, and junction temperature of DDR Si IMPATTs designed to operate at 94, 140, 220, 300, and 500 GHz are calculated for different values of series resistance (R_S) and given in Table 6. It is interesting to observe from Table 6 that both the RF power output and conversion efficiency of the device operating at a particular frequency decreases with the increase of the value of series resistance. The effective magnitude of the device negative resistance (i.e. $|Z_R + R_S|$; where the sign of Z_R is negative) decreases as R_S increases; consequently, the RF power output and hence the conversion efficiency decreases. Owing to reduction in DC to RF conversion efficiency (η_L) as a consequence of increase in R_S, more power is dissipated as heat ($P_{DISP} = (1 - \eta_L) \times P_{DC}$) within the device, which leads to increase in junction temperature of the device. The percentages of decrease in RF power output due to parasitic series resistance (i.e. $|\Delta P_{RF}|/P_{RFo}$ (%); where $\Delta P_{RF} = |(P_{RF} - P_{RFo})|$, P_{RF} is the RF power output of the device for $R_S > 0$ and P_{RFo} is the RF power output of the device when $R_S = 0$) of DDR Si IMPATTs at different operating frequencies are shown as bar graphs in Fig. 9. It is worth noting from Table 6 and Fig. 9 that, the effect of series resistance is more prominent in devices operating at higher frequencies, especially in the device operating at the THz regime (i.e. 0.3 and 0.5 THz). This is mainly due to the magnitude of negative resistance (Z_R) of the device which is very small at higher frequency (THz) devices as shown in Table 5. Thus, at higher frequencies, the value of series resistance must be kept very small to get RF power output from those devices, otherwise real part of equation (14) may no longer remain negative, causing no RF power output from the device.

G) Validation of the simulation results

Figure 10 shows the variations of RF power output of DDR Si IMPATTs obtained from NSVE L-S simulation presented in this paper for different R_S values, well-established DEFM S-S simulation for $R_S = 0$ [17] and experimental measurements [1, 33, 34] with optimum frequency. Luy *et al.* [33], fabricated DDR IMPATTs based on Si designed to operate at 94 GHz. They obtained peak RF power of 600 mW at 94 GHz with 6.7% DC to RF conversion efficiency from their molecular beam epitaxy (MBE) grown p^+–p–n–n^+ structured IMPATT diode. The NSVE L-S simulation of DDR Si IMPATT device at 94 GHz shows the device is capable of delivering 657.54 mW peak RF power output with 8.25% conversion efficiency for a hypothetically assumed 0.0 Ω series resistance at a voltage modulation of 50%. The RF power

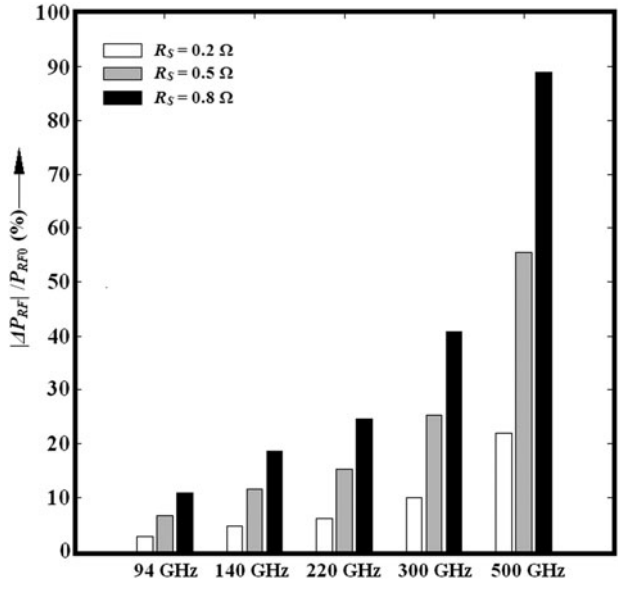

Fig. 9. Bar graphs representing the percentages of decrease in RF power output of DDR Si IMPATTs due to parasitic series resistance.

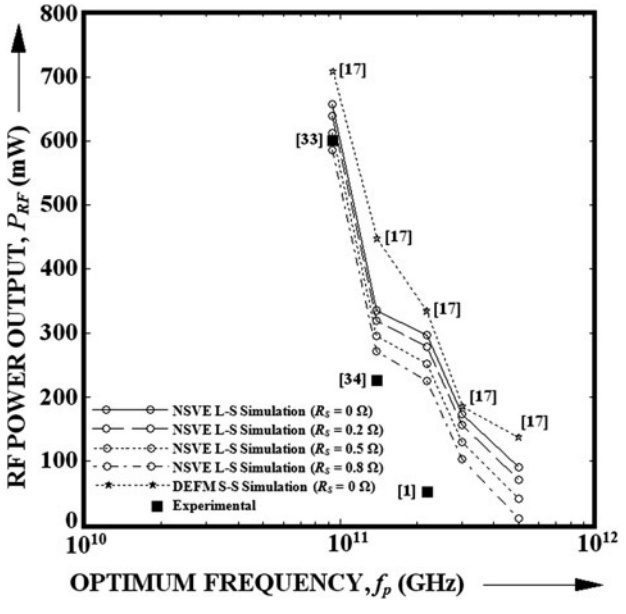

Fig. 10. Variations of RF power output with optimum frequency of DDR Si IMPATTs.

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and efficiency reduced to 640.15 mW and 8.03%, respectively, for the same voltage modulation if the series resistance of the device is 0.2 Ω, which is the experimentally obtained series resistance of 94 GHz DDR Si IMPATT under practical operating conditions [33]. However, DEFM S-S simulation predicts that the same device can deliver 708.43 mW of peak RF power with 10.58% conversion efficiency at 94 GHz for 30% voltage modulation [17]. The deviation of NSVE L-S and DEFM S-S simulation results with respect to experimental results are 6.7–9.6% and 18.1%, respectively, in terms of RF power output and 19.9–23.1% and 57.9% in terms of DC to RF conversion efficiency. Wollitzer *et al.* [34], obtained 225 mW peak RF power output from a 140 GHz DDR Si IMPATT oscillator, while the RF power outputs of DDR Si IMPATTs obtained from NSVE L-S and DEFM S-S simulations at 140 GHz are 334.49 and 446 mW, respectively. Thus, it is clear from the above comparison that the NSVE L-S simulation results are in closer agreement with the experimental results as compared to those of DEFM S-S simulation results. This fact can be explained a follows. Practically, IMPATT diodes operate in L-S mode, where voltage modulation remains within 50–60%. DEFM S-S simulation which is valid for up to 30% voltage modulation due to the S-S approach is not sufficient to predict RF power output and efficiency of the device accurately and the practical situation demands L-S simulation. Midford and Bernick [1], obtained 50 mW RF power output from 220 GHz, DDR Si IMPATT diode. However, NSVE L-S and DEFM S-S simulation predicts that the device can deliver 297.20 and 334.23 mW of peak RF power, respectively, at 220 mW. This discrepancy between the simulated and experimental results at 220 GHz may be due to the un-optimized device structure, different biasing conditions, inappropriate experimental arrangements, etc. adopted by the experimentalists in [1]. However, NSVE L-S simulation is expected to predict more accurate RF power output as compared to DEFM S-S simulation. As far as authors knowledge is concerned, no experimental report is available in the published literature till date on DDR Si IMPATTs operating at THz frequencies (0.3 and 0.5 THz). Thus, the simulation results of 0.3 and 0.5 THz DDR Si IMPATTs could not be compared with the experimental results. However, better prediction of RF power output from DDR Si IMPATTs at 94, 140, and 220 GHz by NSVE L-S simulation which is closer to the experimental results as compared to conventional DEFM S-S simulation, provides much greater assurance in the proposed approach even at the THz regime.

V. CONCLUSION

The L-S characterization of DDR IMPATT devices based on Si designed to operate at different mm-wave and THz frequencies up to 0.5 THz is carried out in this paper. The upper cut-off frequency limit of DDR Si IMPATTs is obtained as 0.5 THz from the avalanche response time based study. The effect of parasitic series resistance on the L-S properties of DDR Si IMPATTs is also investigated, which shows that the decrease in RF power output and conversion efficiency of the device due to series resistance is more pronounced at higher frequencies especially at the THz regime. The NSVE L-S simulation results are compared with well established DEFM S-S simulation results and finally both are compared with the experimental results. The comparative study shows that the proposed NSVE L-S simulation results are in closer agreement with experimental results as compared to those of DEFM S-S simulation. The present study strongly validates the NSVE L-S simulation scheme developed by the authors and simulation study explores the potentiality of DDR Si IMPATTs as powerful terahertz solid-state sources. The design considerations and L-S results presented in this paper will be worthwhile for future experimentalists and encourage them to fabricate DDR Si IMPATTs operating at the THz regime for several possible THz applications such as THz imaging, spectroscopy, bio-sensing, quality inspection in various industrial branches, medical and pharmaceutical applications, THz astronomy, etc.

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