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RESEARCH PAPER

Power performance of 65 nm CMOS integrated LDMOS transistors at WLAN and X-band frequencies

SARA LOTFI[1], OLOF BENGTSSON[2] AND JÖRGEN OLSSON[1]

Laterally diffused metal oxide semiconductor (LDMOS) transistors with 10 V breakdown voltage have been implemented in a 65 nm Complementary metal oxide semiconductor (CMOS) process without extra masks or process steps. Radio frequency (RF) performance for Wireless local area network (WLAN) frequencies and in X-band at 8 GHz is investigated by load-pull measurements in class AB operation for both 3.3 and 5 V supply voltage. Results at 2.45 GHz showed 290 mW/mm output power density with 17 dB linear gain and over 45% power added efficiency (PAE) at 4 dB compression at a supply voltage of 5 V. Furthermore, results in X-band at 8 GHz show 8 dB linear gain, 320 mW/mm output power density and over 22% PAE at 4 dB compression. Third-order intermodulation measurements at 8 GHz revealed OIP3 of 18.9 and 21.9 dBm at 3.3 and 5 V, respectively. The transistors were also tested for reliability which showed no drift in quiescent current after 26 h of DC stress while high-power RF stress showed only small extrapolated drift at 10 years in output power density. This is to the authors' knowledge the first time high output power density in X-band is demonstrated for integrated LDMOS transistors manufactured in a 65 nm CMOS process without extra process steps.

Keywords: LDMOS, CMOS, Power amplifier, WLAN, X-band

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I. INTRODUCTION

Implementing low voltage RF-LDMOS in CMOS processes decreases cost and increases flexibility in various RF power applications [1], especially if the power amplifier (PA) can be integrated onto one single CMOS chip. Low voltage LDMOS transistors can be added to a CMOS process with only few extra process steps and masks [2–4] which enables optimal transistor performance. However, avoiding extra masks or process steps is attractive to foundries since any extra costs or changes to existing device parameters are preferably avoided. This has, for example, been performed in 0.18 μm CMOS [5] and in 65 nm CMOS [6, 7].

At high frequencies, silicon-based technologies are continuing to be improved, but it is still a challenging task for silicon CMOS to cover power applications at X-band (8–12 GHz) such as radar and communication. In [8], it is reported on an LDMOS transistor integrated into a 0.13 μm CMOS process operating at X-band (11 GHz) with a saturated output power (P_{OUT}) of 0.25 W/mm, 11 dB gain and 22% power added efficiency (PAE). In another study, LDMOS transistors integrated in a 0.25 μm BiCMOS process for RF power applications at 1.8 GHz are presented [9], although adding extra masks and process steps as in [8].

Advanced standard CMOS technologies at the 65 nm node, lack "high-voltage" RF devices with the good linearity needed in on-chip PAs. In this study, an LDMOS transistor, intended for WLAN PA on single-ship solutions, was designed and fabricated in a 65 nm CMOS process at foundry without extra process steps or additional masks. The advantages using the 65 nm CMOS process would be a faster, more cost-effective, and more energy-efficient system, compared to, e.g. the 0.13 μm CMOS process used in [8]. However, with these adapted transistor designs, reaching optimal performance can be challenging. Initial evaluation of one of the device designs was performed in [7], with focus on DC and RF performance and power characterization at the WLAN frequencies 2.45 and 5.8 GHz, and showed successful results. Moreover, the LDMOS was implemented as a WLAN PA on a test board in [7] together with matching circuits to demonstrate the feasibility. The LDMOS transistors were designed for a supply voltage of $V_{dd} = 3.3$ V but also showed to be able to operate at $V_{dd} = 5$ V due to the breakdown voltage of 10 V. The results in [7] indicated that this LDMOS could even be pushed into X-band. Here, the authors report more in-depth power performance and analysis at 2.45 and 5.8 GHz. Moreover, this paper is, to the authors knowledge, the first report on X-band RF power performance for a 65 nm CMOS integrated LDMOS. An output power density of 320 mW/mm and PAE of 22% at 8 GHz at a supply voltage of 5 V is demonstrated. With the high breakdown voltage, a high f_T and good power performance demonstrated, this technology

[1]The Ångström Laboratory, Solid State Electronics, Uppsala University, P.O. Box 534, SE-75121 Uppsala, Sweden. Phone: +46-18-471-3035
[2]Ferdinand-Braun-Institut (FBH), Leibniz-Institut für Höchstfrequenztechnik, Gustav-Kirchhoff-Strasse 4, D-12489 Berlin, Germany
Corresponding author:
J. Olsson
Email: jorgen.olsson@angstrom.uu.se

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is also expected to be useful as an integrated driver for GaN-based switch mode PAs [6].

The thin gate oxide together with the high electric fields may make the transistor vulnerable to hot carrier effects and gate tunneling. The reliability and stress mechanisms at various DC bias points of the LDMOS were investigated in [10]. This work also includes long-term DC and large-signal stress at the quiescent point equivalent to class-AB operation. The amount of self-heating in a quiescent bias point is also evaluated with pulsed IV-sweeps compared to static IV.

II. DEVICE DESIGN AND FABRICATION

A test chip, see Fig. 1, with several sizes of LDMOS transistors (different number of fingers), was fabricated in a 65 nm CMOS process. A schematic cross-section of the LDMOS is shown in Fig. 2. The 65 nm process for I/O modules with a 50 Å gate oxide thickness was chosen for the transistors and no halo doping was used. The fabrication process used at foundry did not allow for changing process parameters or adding masks. Hence, the design was optimized without adding masks or other process steps. The maximum drain voltage of 10 V (at gate voltage $V_g = 0$ V), is set by the nwell–pwell junction. To achieve the 10 V breakdown voltage of the LDMOS transistor, the length of the drain drift region was optimized. Simultaneously, a low R_{ON} of 2.4 Ωmm was achieved with the extended drain region. The drift region was protected with the "silicide block"-mask, available in the 65 nm CMOS process preventing silicidation of the optimized drift region.

The transistor layout has paired fingers where each pair has its own substrate ring, shown in Fig. 3. The substrate ring provides effective grounding of the pwell thus preventing premature breakdown due to snap-back caused by generated minority carriers (holes) in the drift region. The width and channel length is $W/L = 200/0.35$ µm and the total gate length (channel length + overlap) is 0.57 µm. The gate overlap at the source-side is ~0.1 µm and accordingly, the drift region underneath the gate is ~0.12 µm (L_{ov} in Fig. 2). The drift region from gate-edge to drain (L_{drift} in Fig. 2) is 0.5 µm.

III. RESULTS AND DISCUSSION

The following sections present DC and small-signal measurements at room temperature followed by on-wafer power characterization using a load-pull measurement setup and RF-probes. Degradation effects are investigated with DC- and RF-stress measurements and finally self-heating is investigated as well.

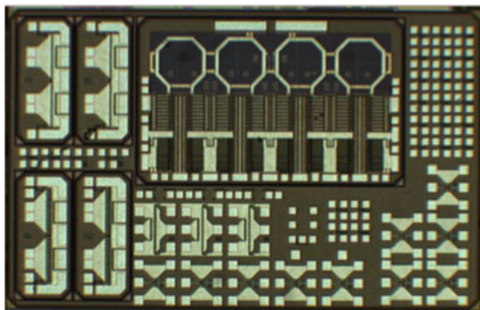

Fig. 1. Fabricated test chip in 65 nm CMOS with transistors of various sizes. Chip size is 2.5 mm × 4 mm.

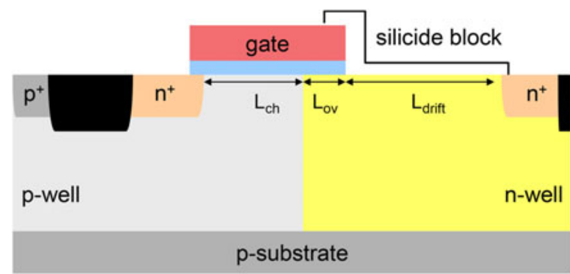

Fig. 2. Schematic cross-section of the fabricated LDMOS. The extended drain region to support the high drain voltage is formed by a silicide block. Channel length – $L_{ch} = 0.35$ µm, overlap region – $L_{ov} = 0.12$ µm, and drift region length – $L_{drift} = 0.5$ µm.

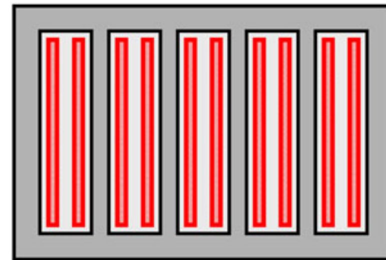

Fig. 3. Schematic layout showing five pairs of fingers where each pair is surrounded by a p+ substrate ring. Only gate fingers and p+ ring are shown for simplicity.

A) DC and RF characterization

Output characteristics were measured and are shown in Fig. 4. The threshold voltage and R_{ON} was extracted to ~0.6 V and 2.4 Ωmm, respectively. Maximum transconductance at drain voltage $V_d = 5$ V is 260 mS/mm. The effect of device self-heating is clearly evident in the output characteristics in Fig. 4, showing the characteristic negative output conductance.

Small-signal S-parameter measurements were performed with a network vector analyzer. The obtained maximum available/stable power gain MSGMAG and small-signal current

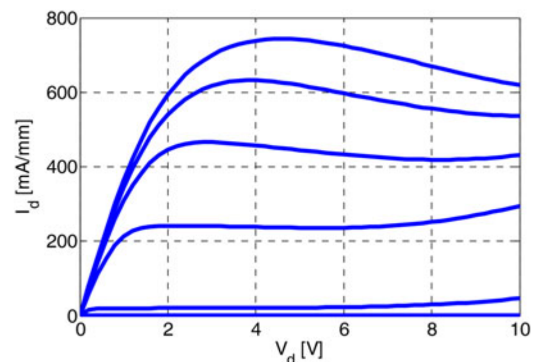

Fig. 4. Output characteristics for the LDMOS transistor with $W/L = 200/0.35$ µm. $V_g = 0, 1, 2, 3, 4, 5$ V.

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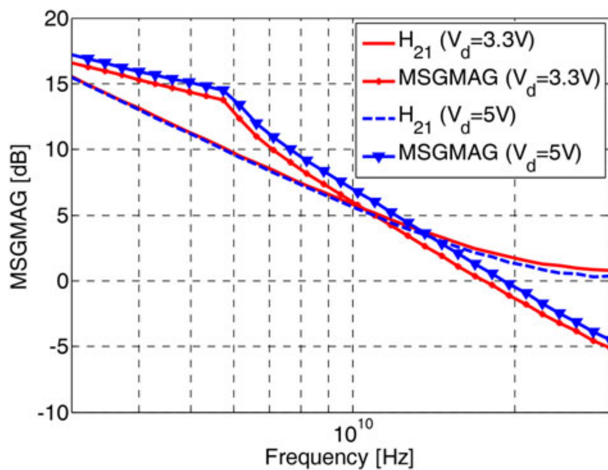

Fig. 5. Maximum available gain MSGMAG and small-signal current gain H_{21} versus frequency ($W = 0.2$ mm) at $V_d = 3.3$ V and $V_d = 5$ V with $V_g = 1.5$ V.

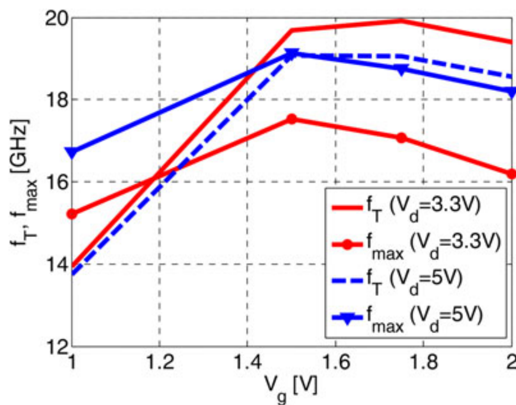

Fig. 6. Extracted f_T and f_{max} versus gate voltage ($W = 0.2$ mm) at $V_d = 3.3$ V and $V_d = 5$ V.

gain H_{21} are plotted in Fig. 5. From the H_{21} and MSGMAG curves, f_T/f_{max} were extracted to 20/17.5 and 19/19 GHz at $V_d = 3.3$ and $V_d = 5$ V, respectively. Figure 6 shows f_T/f_{max} versus gate voltage at $V_d = 3.3$ and $V_d = 5$ V. The maximum of f_T and f_{max} occurs at the same V_g as the maximum of the transconductance, g_m, and the roll-off behavior in f_T/f_{max} is also seen in g_m. The increase in f_{max} with V_d is mainly due to reduced output conductance (real(Y_{22})). The decrease in f_T with V_d is due to a reduction of g_m.

B) Large-signal RF measurements

Power characterization was performed on-wafer for WLAN frequencies at 2.45 and 5.8 GHz at $V_{dd} = 3.3$ V and $V_{dd} = 5$ V. Furthermore, power characterization was also performed in X-band at 8 GHz at both $V_{dd} = 3.3$ and $V_{dd} = 5$ V. The power characterization was conducted in a load-pull system, see Fig. 7. In the system mechanical tuners are used to find and present the optimum impedances (Γ_S and Γ_L) at the reference planes of the transistor, thereby emulating the conditions in a PA. DC supply is provided through bias-tees. Input power (P_{IN}) and output power (P_{OUT}) are measured at the reference planes together with the DC parameters. Based on this information, power parameters such as gain and PAE of the transistor can be fully characterized. The samples were mounted on a metal flange with silver epoxy and the chuck was cooled to $T = 17$ °C. A low class AB bias-point was chosen with the quiescent drain current $I_{dQ} \approx 10\%$ of I_{dmax} (maximum current at $V_g = 5$ V) equivalent to $V_g = 1.2$ V. All measurements were performed in a single-ended configuration. The transistors were matched at high input power for optimum output power. Since a high output power was targeted in the application, a compression point at -4 dB is chosen for comparison. Table 1 summarizes all power characterization results for different operating conditions.

1) Load-pull at 2.45 and 5.8 GHz

A transistor size of $14 \times W/L = 200/0.35$ µm (equal to 2.8 mm gate width) was chosen for WLAN band characterization at 2.45 and 5.8 GHz.

In Figs 8(a) and 8(b), P_{OUT}, gain, and PAE versus input power are presented for 2.45 GHz at $V_{dd} = 3.3$ and $V_{dd} = 5$ V, respectively. Linear gain is ~17 dB at both supply voltages. At $V_{dd} = 3.3$ V, output power reaches ~27 dBm and 36% PAE at 4 dB compression. However, when increasing the supply voltage to 5 V, P_{OUT} reaches over 29 dBm with above 43% PAE.

In Figs 9(a) and 9(b), power characterization is presented at 5.8 GHz at $V_{dd} = 3$ V and $V_{dd} = 5$ V, respectively. A

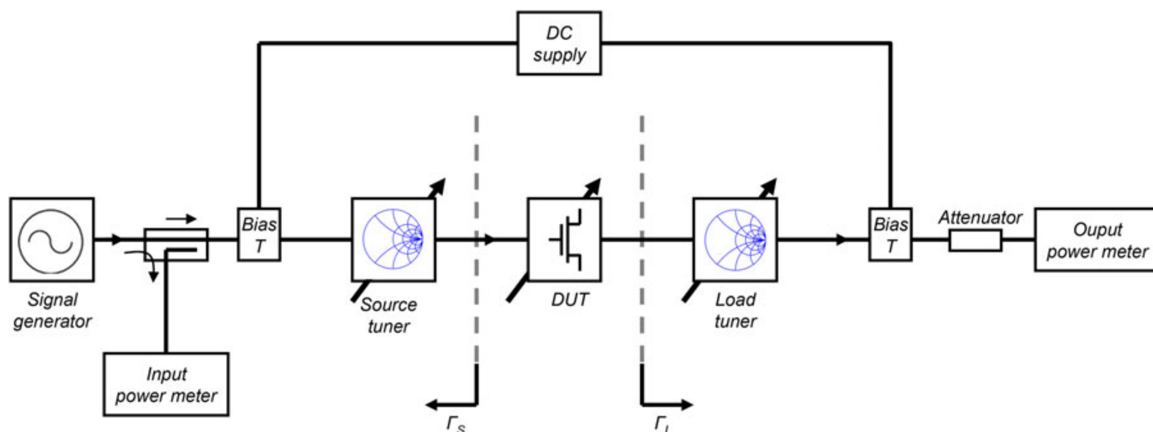

Fig. 7. Schematic picture showing the measurement setup for power characterization of the transistors using the load-pull technique. Γ_S and Γ_L are the reflection coefficients representing the source and load impedance at the input and output ports of the DUT, respectively. Tuner settings are changed to the optimal impedance for high output power and P_{IN} and P_{OUT} are measured with power meters.

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Table 1. Power characterization results for different operating conditions.

Frequency	2.45 GHz		5.8 GHz		8 GHz	
V_{dd} (V)	3.3	5	3.3	5	3.3	5
Compression point (dB)	4	4	4	3	4	4
Width (mm)	2.8	2.8	2.8	2.8	0.2	0.2
Linear gain (dB)	17	17	9	10	7	8
P_{OUT} (dBm)	26.6	29.1	25.5	27.7	14.4	18.1
P_{OUT} (mW/mm)	163	290	127	210	138	323
PAE (%)	36.0	43.5	29.0	33.6	17.8	22.1
OIP3 (dBm)	–	–	–	–	18.9	21.9
Γ_S	$0.79/166^\circ$	$0.76/168^\circ$	$0.83/-179^\circ$	$0.83/180^\circ$	$0.45/117^\circ$	$0.46/112^\circ$
Γ_L	$0.91/172^\circ$	$0.82/169^\circ$	$0.86/170^\circ$	$0.86/167^\circ$	$0.50/103^\circ$	$0.51/90.5^\circ$

noticeable decrease in gain is observed compared to the results at 2.45 GHz due to the higher frequency. At, 5.8 GHz, output power at $V_{dd} = 3.3$ V is ~26 dBm, 1 dB lower compared to at 2.45 GHz. Also, PAE is reduced at the higher frequency. At $V_{dd} = 5$ V, the device could not be driven to full saturation due to limited amount of input power, as seen in Fig. 9(b). The output power is still close to the values at 2.45 GHz, e.g. at $V_{dd} = 5$ V, P_{OUT} reaches ~28 dBm, and PAE is ~34%.

A larger transistor with 2×14 unit cells with $W/L = 200/0.35$ μm with a total gate width of 5.6 mm was mounted on a testboard and was evaluated on-chip and compared to a reference using a PA cascode design with two conventional transistors. The LDMOS delivered 32.8 dBm in the 2.45 GHz band, 1 dB higher compared to the cascode reference, and is the highest reported value to the authors' knowledge for this type of transistor. The LDMOS also passed a frequency mask test for a typical WLAN signal [7].

2) Load-pull at 8 GHz

A smaller transistor size, $W/L = 200/0.35$ μm was used for power characterization in X-band at 8 GHz. At higher frequencies and with large transistor sizes, the real part of the impedance appears closer to the edge in a Smith-chart and accordingly, impedance matching with the tuners was difficult to achieve with the larger transistor size, as used at the WLAN frequencies. Figures 10(a) and 10(b) shows P_{OUT}, gain and PAE versus input power at $V_{dd} = 5$ V and $V_{dd} = 3.3$ V, respectively. Linear gain has only decreased 2 dB compared to 5.8 GHz data. At $V_{dd} = 3.3$ V, output power is ~14 dBm and PAE is ~18%. When increasing the supply voltage to 5 V, P_{OUT} and PAE reaches over 18 dBm and 22%, respectively.

If the P_{OUT} values are compared in mW/mm it is seen that the LDMOS can deliver as much power in X-band as at, i.e. 2.45 GHz (320 mW/mm at 8 GHz versus 290 mW/mm at

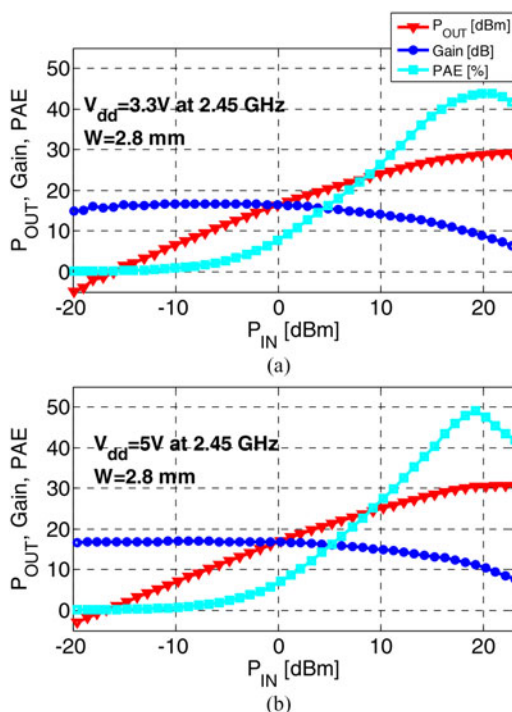

Fig. 8. Power sweep at 2.45 GHz. (a) $V_{dd} = 3.3$ V. Linear gain is ~17 dB. At 4 dB compression: $P_{OUT} = 26.6$ dBm and PAE = 36.0%. (b) $V_{dd} = 5$ V. Linear gain is ~17 dB. At 4 dB compression: $P_{OUT} = 29.1$ dBm and PAE = 43.5%.

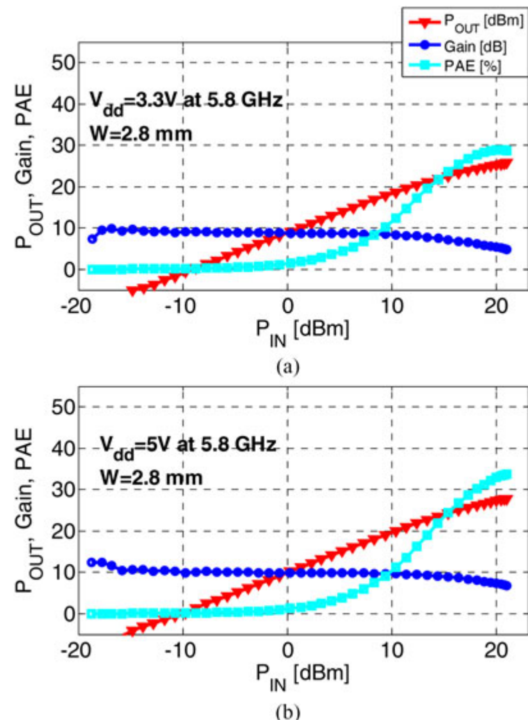

Fig. 9. Power sweep at 5.8 GHz. (a) $V_{dd} = 3.3$ V. Linear gain is ~9 dB. At 4 dB compression: $P_{OUT} = 25.5$ dBm and PAE = 29.0%. (b) $V_{dd} = 5$ V. Linear gain is ~10 dB. At 3 dB compression: $P_{OUT} = 27.7$ dBm and PAE = 33.6%.

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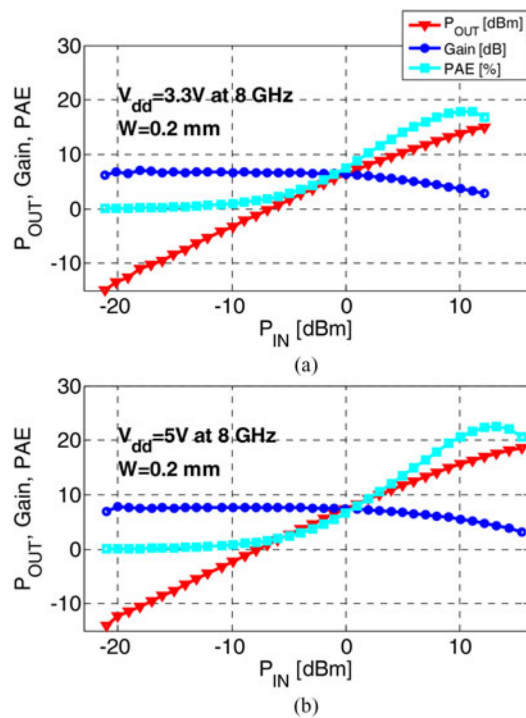

Fig. 10. Power sweep at 8 GHz. (a) $V_{dd} = 3.3$ V. Linear gain is ~7 dB. At 4 dB compression: $P_{OUT} = 14.4$ dBm and PAE = 17.8%. (b) $V_{dd} = 5$ V. Linear gain is ~8 dB. At 4 dB compression: $P_{OUT} = 18.1$ dBm and PAE = 22.1%.

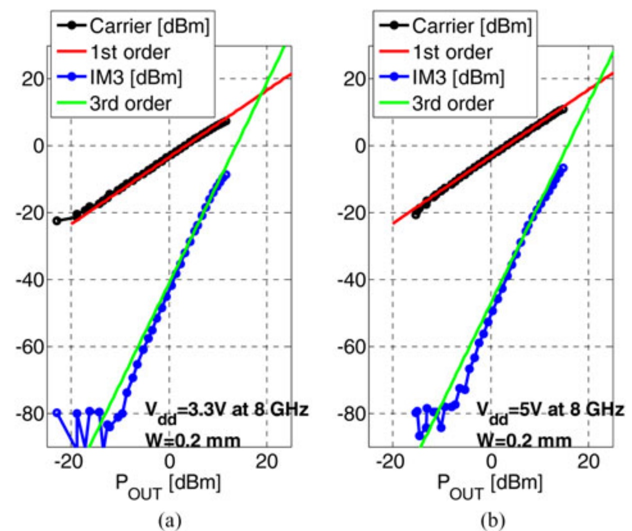

Fig. 11. Worst case third-order intermodulation, IM3, products at 8 GHz and at (a) $V_{dd} = 3.3$ V and at (b) $V_{dd} = 5$ V, respectively.

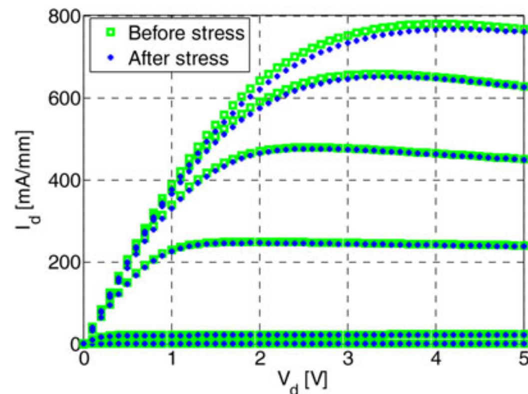

Fig. 12. Output characteristics before and after 26 h DC-stress ($W = 0.2$ mm) at $V_g = 1.2$ V and $V_d = 5$ V.

2.45 GHz), however, with significantly lower gain and lower PAE. This is to the authors' knowledge the first time high output power density is demonstrated in X-band for a 65 nm CMOS integrated LDMOS without additional process steps.

For a PA application, the third-order non-linearities are the most important since they generate spectral components close to the channel that are hard to filter out. The output third-order intercept point (OIP3) was extrapolated from 8 GHz two-tone measurements in the load-pull setup using a two-tone signal with 1 mHz tone-spacing generated in a vector signal analyzer and linearized to −80 dBc at the input of the transistor. The third-order components were measured with a spectrum analyzer on the output. The devices were matched in class-AB for optimum output power as before. The worst case third-order intermodulation products, IM3, are shown in Fig. 11 and the extrapolated OIP3 is found in Table 1. The OIP3 is about 10–15 dB above P1 dB indicating a well-behaved component with regard to non-linearities.

C) Degradation effects

Transistors with $W = 0.2$ mm were subjected to DC-stress for 26 h at room temperature in class-AB quiescent bias points at $V_g = 1.2$ V and both $V_d = 5$ and $V_d = 3.3$ V. No burn-in was performed; IV characteristics were measured on a virgin device and subsequently after stress for calculation of drift in transistor parameters. At $V_g = 1.2$ V and $V_d = 3.3$ V, no major degradation was observed after 26 h as evident in the very low gate current in the order of fA [10]. At $V_g = 1.2$ V and $V_d = 5$ V, hot carrier injection is expected [10] as observed in the increase of gate current. The LDMOS showed a R_{ON} drift of 2.8% after 26 h while the quiescent current and threshold voltage were unaffected, see output characteristics in Fig. 12. This is consistent with the results in [10] where hot carrier injection is located in the overlap region causing R_{ON} to drift.

Long term large-signal stress at 4 dB compression was also performed in the load-pull setup, at $V_{dd} = 3.3$ V and $V_{dd} = 5$ V. P_{OUT} versus time is plotted in Fig. 13 showing no drift at $V_{dd} = 3.3$ V after 72 h. Although the transistor is driven very hard at $V_{dd} = 5$ V, close to breakdown and at high compression, only a small drift in P_{OUT} is observed. The drift was extrapolated to 10 years resulting in a −1.3% drift of P_{OUT} in dBm, which equals to a −5.2% drift in mW/mm. However, operation at 5 V introduces high electric fields in the transistor structure which may cause other degradation effects to occur, and consequently reduce the transistor life time. At 3.3 V, the electric fields are lower and the results both from this paper and [10] indicate no significant drift of any transistor parameter, therefore a lifetime longer than 10 years is expected.

Output characteristics were measured by applying the voltage with a pulse length of 0.2 μs in order to reveal the current without self-heating effects. The results are compared

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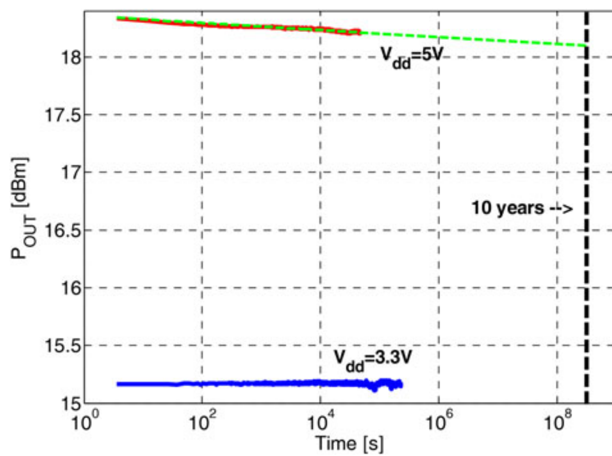

Fig. 13. Large-signal stress showing P_{OUT} versus time at 4 dB compression and at $V_{dd} = 3.3$ V and $V_{dd} = 5$ V.

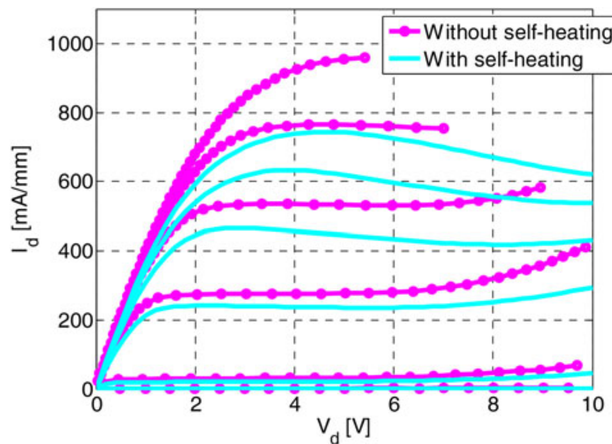

Fig. 14. Output characteristics with and without self-heating effects for the transistor ($W = 0.2$ mm), $V_g = 0, 1, 2, 3, 4, 5$ V. Dotted lines represent dynamic sweep with a pulse length of 0.2 µs.

to a regular IV-sweep in Fig. 14. It is evident from the graph that the temperature in the transistor is high, estimated to over 100°C using the thermal resistivity of silicon and considering the transistor as a point source [11].

IV. CONCLUSION

This paper demonstrates LDMOS transistors, integrated, and fabricated in a 65 nm CMOS process without extra masks or process steps. The transistors show good power performance for WLAN at 2.45 and 5.8 GHz. For example, power performance at 2.45 GHz showed 290 mW/mm output power density and over 43 % PAE at 4 dB of compression. Furthermore, this type of transistor has for the first time been demonstrated in X-band at 8 GHz and showed a maximum output power density of over 300 mW/mm with a PAE of 22% at 4 dB of compression. The combination of very good RF performance and possibility of integration in 65 nm CMOS show the benefits of this type of LDMOS, for e.g. switching applications without linearity requirements. DC-stress measurements show no drift in quiescent current, while slight R_{ON} drift due to hot carrier injection in the drift region underneath the gate is observed. Large-signal stress shows small extrapolated drift in P_{OUT} after 10 years.

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S. Lotfi received a degree in Engineering Physics with specialization in Electrical Engineering from Uppsala University in 2008 and received her Ph.D. degree in Engineering Sciences with specialization in Electronics in February 2014. She is now a researcher at the Department of Solid-State Electronics at the Ångström Laboratory, Uppsala University.

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O. Bengtsson received his B.Sc. degree in Electrical Engineering from the University of Gävle, Sweden, in 1997 and the Lic.Tech. and Ph.D. degrees from Uppsala University, in 2006 and 2008, respectively. From 1998 to 2009, he was teaching microwave engineering at the University of Gävle. Since April 2009, he has been with the Ferdinand-Braun-Institut (FBH), Berlin, Germany. His main interests are RF-power device design, physical device simulations (TCAD), large-signal device characterization, and RF-power amplifier design.

J. Olsson received his Ph.D. degree in Electronics from Uppsala University, Sweden, in 1996. During 1997 he was a visiting scientist at Digital Semiconductor, Hudson, MA, USA, working on modeling of ion implantation and CMOS process integration. In 2008, he was appointed Professor in Solid-State Electronics, Uppsala University. He is the head of the Solid State Device Group at the Ångström Laboratory, Uppsala University. His research interests are primarily in the fields of high-frequency MOS-based devices and processes, SOI-technology, and RF-power devices. He is also the director of postgraduate studies at the Department of Engineering Sciences. He is author of over 160 scientific papers in international journals and conferences.

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