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Research Paper

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Abstract

This paper presents a systematic comparison of the relationship between transmission line characteristic impedance and Q-factor of CPW, slow-wave CPW, microstrip, and slow-wave microstrip in the same CMOS back-end-of-line process. It is found that the characteristic impedance for optimal Q-factor depends on the ground-to-ground spacing of the slow-wave transmission line. Although the media are shown to be similar from a mode of propagation point of view, the 60-GHz optimal Q-factor for slow-wave transmission lines is achieved when the characteristic impedance is $\approx 23 \Omega$ for slow-wave CPWs and $\approx 43 \Omega$ for slow-wave microstrip lines, with Q-factor increasing for wider ground plane gaps. Moreover, it is shown that slow-wave CPW is found to have a 12% higher optimal Q-factor than slow-wave microstrip for a similar chip area. The data presented here may be used in selecting Z_0 values for S-MS and S-CPW passives in CMOS that maximize transmission line Q-factors.

Introduction

Slow-wave transmission lines (SWTL) are promising building blocks for mm-wave integrated circuit (IC) designs in CMOS due to the high achievable transmission line Q-factors [1, 2]. For a required electrical length, a higher transmission line Q-factor results in lower loss, leading to more efficient circuits like couplers, filters and power dividers. The most common SWTLs investigated in literature are the slow-wave coplanar waveguide (S-CPW) [1–4] and a transmission medium designated by prior literature as slow-wave microstrip (S-MS) [5, 6]. The operating principles have been described in detail in prior literature [2, 4, 5], with some recent examples in literature [7–14] clearly illustrating its value in mm-wave CMOS circuit design.

S-CPW has been the topic of extensive parametric study for transmission line slow-wave factor and Q-factor [1, 15], as well as equivalent circuit modelling [3]. There has, however, not been a systematic comparison of S-CPW and S-MS in terms of (i) propagation mode, and (ii) Q-factor for comparable characteristic impedance (Z_0). Some studies have been carried out on the effect of Z_0 on Q-factor in slow-wave CPS (S-CPS) [15], but they did not elaborate on the methods or process geometry, and, to the best of the authors' knowledge, no measurement verification has been shown.

This paper presents the first comparative study on the propagating modes and effect of Z_0 on Q-factor for S-CPW and S-MS. The data presented here may be used to select Z_0 values for S-CPW and S-MS line components in CMOS circuits that maximise transmission line Q-factors. This may be valuable to the application of S-MS and S-CPW in designs where there is a need for low-loss transmission line sections, but freedom in the selection of Z_0 . Examples include impedance matching networks [9], transmission zeros for filters [16], or tank resonators for mm-wave VCOs [14]. It also shows that these two types of SWTL are very similar in terms of propagation mode, despite the differentiating nomenclature established in literature. The analysis setup and transmission line geometries are discussed in Section II, followed by the simulation setup and measurement validation in Section III. The analysis of the mode propagation is carried out in Section IV. Results of the effect of Z_0 on the Q-factor are shown and discussed in Section V, and the paper concludes in Section VI.

Analysis setup

Parameter extraction

The symmetric transmission line ABCD parameters can be calculated from S-parameters, from which the parameters α , β , $\epsilon_{r(\text{eff})}$, γ , Q and Z_0 can be extracted using [12, 17]:

$$\gamma = (\cosh^{-1}(A))/l \quad (1)$$

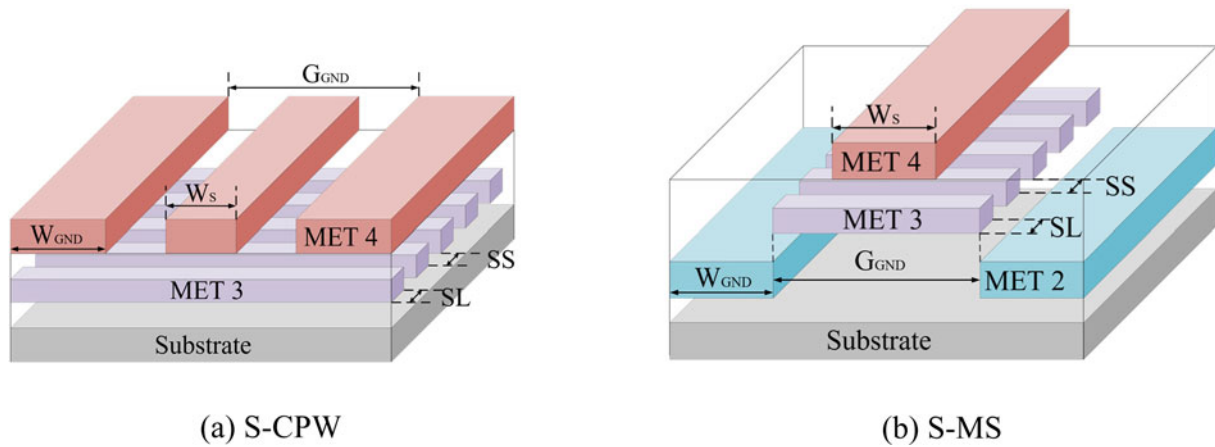


Fig. 1. Cross-sectional views of the slow-wave transmission line structures. (a) S-CPW (b) S-MS.

$$Z_0 = \sqrt{B/C} \tag{2}$$

$$\alpha = 8.686 \cdot \Re(\gamma) \tag{3}$$

$$\beta = (180/\pi) \cdot \Im(\gamma) \tag{4}$$

$$Q = \beta/2\alpha \tag{5}$$

$$\epsilon_{r(eff)} = c_0^2 \cdot \left(\frac{1000 \cdot \beta}{\omega} \right)^2, \tag{6}$$

where γ is the complex propagation constant, l the length (mm), Z_0 the characteristic impedance (Ω), α the attenuation constant (dB/mm), β the phase constant (degrees/mm), Q the quality factor, and $\epsilon_{r(eff)}$ the effective relative permittivity.

Simulations were performed using the HFSS 3D FEM solver with the gap port inductance de-embedded [18]. The transmission lines were implemented in the AMS C35 process with four metal layers and thick M4 ($\approx 3\mu\text{m}$) option. All the simulated transmission lines have a length of $300\mu\text{m}$, which results from a compromise between the precision of the extracted attenuation constant (dB/m), and the inaccuracies in extracting characteristic impedance at frequencies where the line length approaches $\lambda/2$ electrical length (due to standing-wave effects).

Transmission line geometries

The slow-wave transmission lines under consideration are shown in Fig. 1. The CPW and S-CPW strips are implemented on the top metal layer (M4), with S-CPW using M3 for the shielding strip patterning (Fig. 1(a)). The microstrip uses M4 for the signal conductor and M2 for the ground plane, while the S-MS [5] uses M4 for the signal conductor, M3 for the shielding strip layer, and M2 for the slotted ground plane (Fig. 1(b)). This ensures similar separation between the shielding strips and the signal conductor in both S-CPW and S-MS lines, leading to comparable Z_0 ranges. The gap in the S-MS ground plane increases the linear inductance as compared to classical microstrip line, without changing the

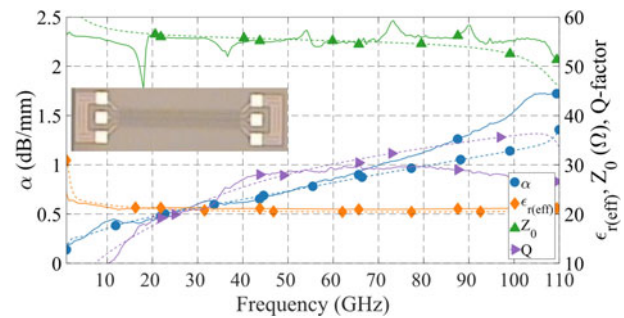


Fig. 2. Broadband validation of parameter extraction method for S-CPW1.

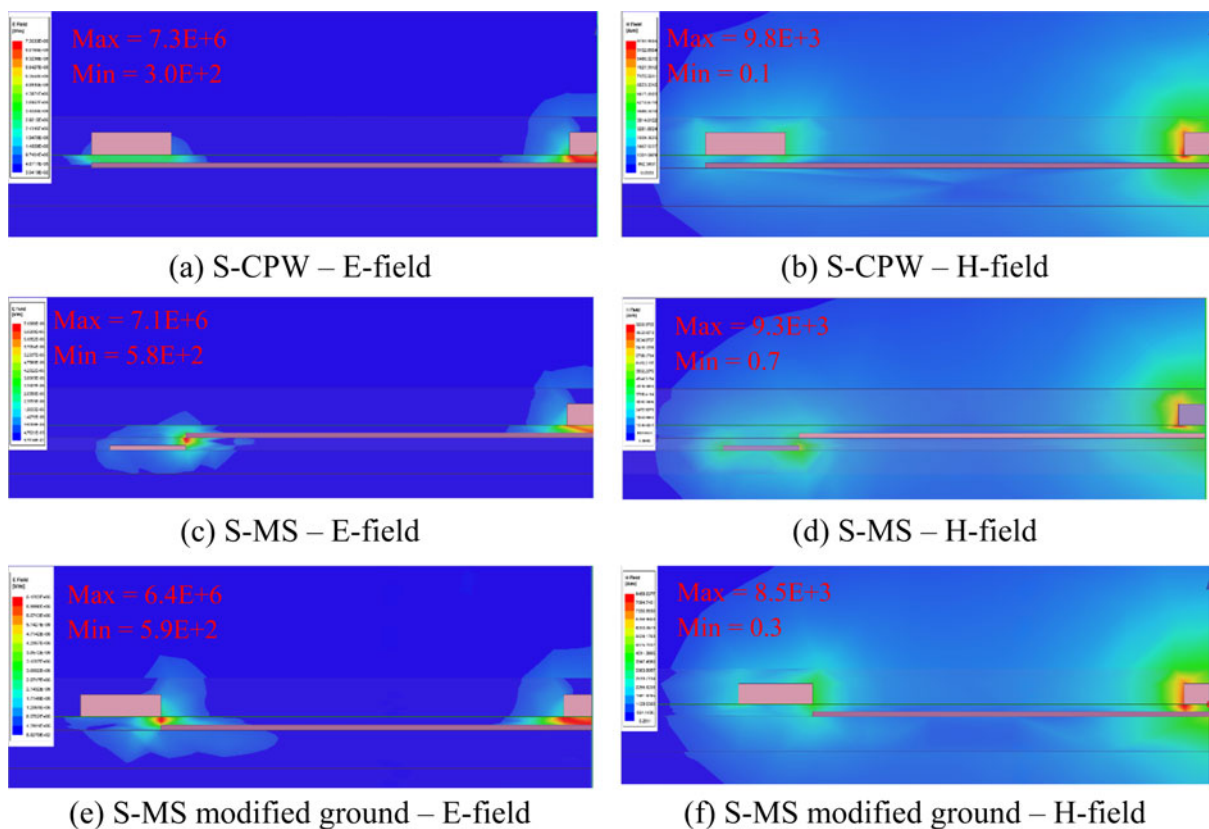
linear capacitance (resulting in a slow-wave behaviour), at the cost of increased chip area. By the same way, for the S-CPW, the shielding strip patterning leads to an increase of the linear capacitance, as compared to classical CPW without changing the linear inductance (resulting in a slow-wave behaviour), here again at the cost of increased chip area. This increase in inductance for S-MS lines and capacitance for S-CPWs may suggest that the propagation modes are different, but this is simply due to the reference taken for the linear inductance or capacitance increase, either microstrip or CPW. As already specified above, we show in section III that the two modes are in fact similar.

Measurement validation of simulation setup and extraction method

To validate the simulation approach, the S-CPWs from [1, 19] were simulated and compared to measurement results, extracting the transmission line parameters as described in Section II. Prototypes were characterized on an Anritsu VNA with GSG wafer probing, with the effects of probe pads de-embedded using the technique in [20]. The resulting comparison for S-CPW1 is shown up to 110 GHz in Fig. 2. The results at 60 GHz, for all four S-CPW geometries, are summarized in Table 1, and compare extremely well with the parameters extracted in [1, 19]. A maximum error of below 5% for $\epsilon_{r(eff)}$ and below 16% for α is obtained in all cases, which are comparable to the measurement error. An increased error in α is evident above 70 GHz (also observed in [1]) and may be attributed to incomplete de-embedding of the

Table 1. Comparison of simulated and measured S-CPW parameters at 60 GHz to validate simulation approach.

S-CPW geometry (μm)	Parameter	Measured	Simulated	Error (%)
S-CPW1:	α (dB/mm)	0.86	0.82	4.7
$W_S = 7$; $G_{\text{GND}} = 107$; $SL = 0.6$; $SS = 1$; $W_{\text{GND}} = 10$	$\epsilon_{r(\text{eff})}$	21	20.5	2.4
S-CPW2:	α (dB/mm)	1.06	1.19	12.3
$W_S = 10$; $G_{\text{GND}} = 210$; $SL = SS = 0.6$; $W_{\text{GND}} = 60$	$\epsilon_{r(\text{eff})}$	37.3	36.4	2.4
S-CPW3:	α (dB/mm)	1.15	1.33	15.7
$W_S = 18$; $G_{\text{GND}} = 218$; $SL = SS = 0.6$; $W_{\text{GND}} = 60$	$\epsilon_{r(\text{eff})}$	50.5	48.0	5.0
S-CPW4:	α (dB/mm)	1.42	1.51	6.3
$W_S = 18$; $G_{\text{GND}} = 318$; $SL = SS = 0.6$; $W_{\text{GND}} = 60$	$\epsilon_{r(\text{eff})}$	56.5	57.6	2.0

**Fig. 3.** SWTL field lines (a) S-CPW – E-field, (b) S-CPW – H-field, (c) S-MS – E-field, (d) S-MS – H-field, (e) S-MS modified ground – E-field, (f) S-MS modified ground – H-field.

tapered feed lines used in the S-CPW prototype [1]. Nevertheless, these results indicate good agreement between simulation and measurement for further analysis. All further results are presented at 60 GHz. Although the specific values presented here may differ at other frequencies and with different BEOL process stacks, it is found that the observed trends are also present in literature where similar parametric variations are applied [15, 21], though a systematic analysis to establish an optimal impedance for maximum Q-factor was not pursued in any of the prior studies.

Propagation mode analysis

In this section, we compare the propagation modes of S-CPWs and S-MS lines, based on the layouts shown in Fig. 1. The electric

and magnetic fields for each of these two lines are given in Figs 3(a)–3(d). Although the two media present similar magnetic field patterns, dissimilar electric field patterns are evident in Figs 3(a) and 3(c). However, if the location of the S-MS ground planes is modified, placing it coplanar with the signal strip, as shown in Figs 3(e) and 3(f), we obtain an electric field with a form similar to that of S-CPW. This leads to the conclusion that the S-CPWs studied in [1, 2] and the S-MS lines studied in [5, 7] propagate a very similar mode, despite the separate designations in prior literature. The distinguishing feature between the geometries is the width of the floating shield. For the transmission lines designated here (in keeping with prior literature [5]) as S-MS, the width of the floating shield is narrower, modifying the linear capacitance and enabling variation of characteristic

Table 2. Signal conductor width ranges for different G_{GND} values.

W_{GND} (μm)	G_{GND} (μm)	W_S (μm)
25	10	0.5–9.5
	30	0.5–25
	50	0.5–45
	80, 100, 120	0.5–60

impedance by modifying its width. This is demonstrated in Section V.

Results

With the validity of the simulation and extraction methods established by measurement, a large parametric simulation study was conducted. $W_{GND} = 25 \mu\text{m}$ and $SS = SL = 0.7 \mu\text{m}$ are kept constant, while G_{GND} is varied from 10 to 120 μm . To vary the characteristic impedance (Z_0), the signal strip width (W_S) is varied (Table 2). This allows for a wide Z_0 tuning range, from which design rules may be derived. As some geometries may violate

PDK layout rules multi-strips and dummy layout strategies may be required in some cases in order to implement these transmission lines.

Figure 4 shows the 60-GHz Q-factor versus Z_0 for S-CPWs versus ground-to-ground spacing G_{GND} and, consequently, required chip area. For comparison, standard CPWs of the same G_{GND} are also simulated. The peak Q-factor for standard CPW increases up to $G_{GND} = 30 \mu\text{m}$ (reaching 14 for $Z_0 = 69 \Omega$) and then decreases for larger G_{GND} . This is due to the electric field that increasingly penetrates the lossy bulk silicon substrate as G_{GND} increases. The narrow-gap S-CPW of $G_{GND} = 10 \mu\text{m}$ exhibits a Q-factor comparable to the best-performing standard CPW, though the S-CPW Q-factor increases as G_{GND} increases, peaking above 30, similar to the trend observed in [21].

In the same way, the Q-factor versus Z_0 for the S-MS lines of various Z_0 values is shown in Fig. 5. For comparison, a standard microstrip line is also considered, achieving a peak Q-factor of 15.6 for Z_0 between 45 and 55 Ω . The S-MS line has a lower Q-factor compared to standard microstrip for small G_{GND} values but increases with increased G_{GND} as is the case with the CPW versus S-CPW comparison.

From the results in Figs 4 and 5, it is evident that the Z_0 for which peak Q-factor is achieved, lowers as G_{GND} increases (see

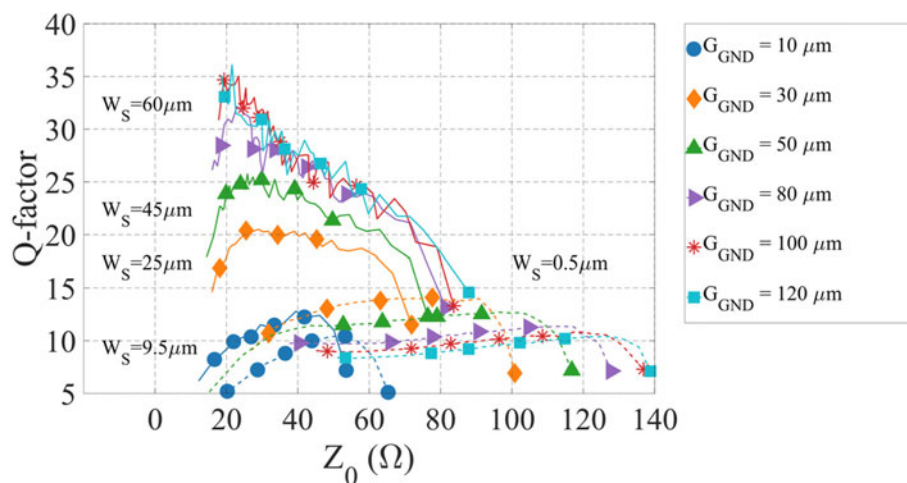


Fig. 4. 60-GHz Q-factor versus Z_0 for CPW (dashed traces) and S-CPW (solid traces) for different G_{GND} values.

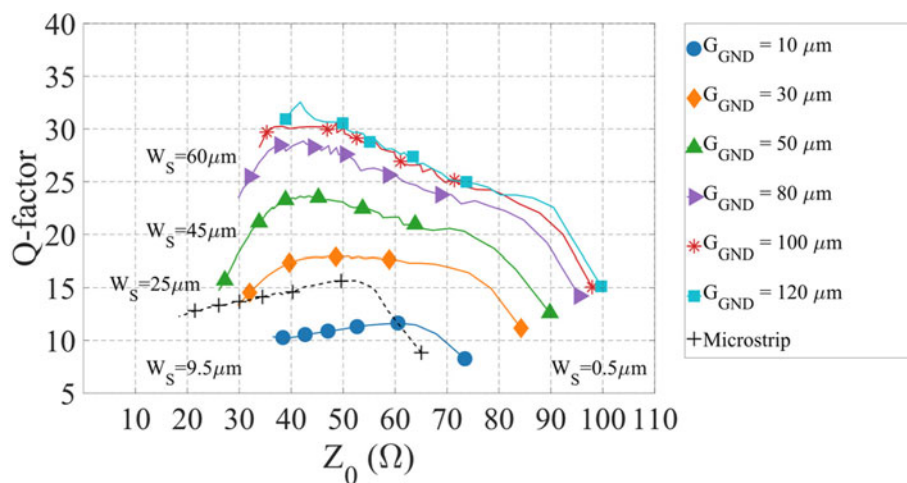


Fig. 5. 60-GHz Q-factor versus Z_0 of S-MS line for different G_{GND} values.

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