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SIP antenna on 0.13 μm SiGe technology at 79 GHz for SRR automotive radar

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This paper describes the analysis and the design of an integrated antenna on 0.13 μm SiGe BICMOS technology. A non-resonant dipole antenna integrated on SiGe is electromagnetically coupled to a radiating element reported on a printed circuit board (PCB) substrate. This integrated solution, also compatible with system in package (SIP) concept, provides significant improvements with respect to direct System On Chip (SoC) integration. The main objective of this SIP antenna lies on the optimization of integrated millimeter wave front-ends modules, considering the immediate antenna environment (especially the lossy substrate and technological dielectric/metallic levels), in order to achieve performances compatible with short range radar specifications at 79–81 GHz. One solution, using a RT/Rogers Duroid 6006 PCB (er = 6, thickness h = *127 μm), is presented, providing a 2.93 dBi gain, and 45% radiation efficiency antenna.*

Keywords: System in package, Radar antenna, On-silicon antenna, On-chip antenna, Integrated antenna, 3D electromagnetic modeling

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I. INTRODUCTION

Recent advances in silicon (Si) technologies allow the design of millimetre-wave integrated systems offering low-cost high performances. Civil applications as future automotive radar sensors are concerned by such technological success to improve road safety and to propose new mobility paradigm.

Current researches [1, 2] have demonstrated that the SiGe BiCMOS technology has promising performances for automotive radars. Achievable HBT transistors on such process offer an FT/FMAX = 230 GHz/200 GHz and present consequently significant advantages in terms of power capability and gain/noise performances. The main challenge is now addressed to the design of SiGe single-chip modules for fully integrated automotive radar, including critical elements such as antennas. This paper is focused on the study of integrated antennas for radar applications. Drastic constraints are addressed by the radar specifications, concerning both the directivity (expected gain # 13–15 dBi for short range radar (SRR) up to 26–30 dBi for long range radar (LRR)) and the half-power beamwidth (30° for SRR, about 2° for LRR). Conventionnal solutions, based upon microstrip arrays [3], dielectric lens [4, 5], and reflectors [6] are usually proposed, but the complete association/integration with Si technologies has never been investigated.

Some works [7, 8], focused on on-Si antenna studies, exhibit quite low radiation performance results. Directivity gain values of −2 and −10 dBi are obtained on high resistivity and low resistivity (LR) Si substrate, respectively. Therefore, the integration of antenna on Si for meeting radar specifications is a fundamental and critical challenge, due to the contrast between antenna expectations and performances induced by Si substrate characteristics. The main objective of our investigation deals therefore on SOC/SIP with on-Si integrated antennas.

In a previous work [9], an integrated antenna on 0.13 μm SiGe BiCMOS technology has been studied, and technological tricks are adopted to conciliate high integration viability and radiation performances. In fact, an integrated dipole provides low performances as expected (gain # – 6.8 dBi; radiation efficiency # – 8.9%) in relation with the lossy Si high permittivity substrate incidence. Technological solutions involving substrate modifications (improving Si resistivity [10, 11], using membrane technology [12]) have already been investigated. Unfortunately, these solutions are not advisable for co-integration requirements (with the RF radar transceiver as well as the digital IC). Indeed, the high resistivity Si is not compatible with bipolar devices specifically required for RF power achievement, and membrane implementation requires a complex fabrication process.

Moreover, in [13, 14], the authors demonstrated that above-IC integration technique is compatible with SiGe technology, offering simultaneously low cost and good performances. The above-IC integrated antennas offer enhanced radiated performances, but still under the expected ones for radar applications. Therefore, a design challenge remains today, with the opportunity of combining system on chip with system in package solutions for solving opposite constraints (integration level versus electrical performances), considering the non-adequate supporting environment. Some examples have being proposed in the literature, and original and innovative configurations are proposed in this paper.

In [15], an hybrid solution is analyzed, proposing an integrated above-IC antenna electromagnetically coupled to a focusing system. The gain directivity is improved by the presence of the dielectric lens. In [9], a reference antenna

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dedicated to array design is presented, considering the above-IC process. The radiation efficiency is improved due to the masking effect of the above dielectric layer that reduces lossy Si incidence with respect to the radiating element.

This contribution is mainly focused on the possibility of exploiting higher integration levels while optimizing on-Si antenna performances. The main idea consists in exploiting the benefit of combining system on chip (SOC) and system in package (SIP) architecture, in order to improve radiation efficiency. A non-resonant slot dipole on SiGe BiCMOS is electromagnetically coupled with a radiating structure implemented on polymer substrate. Such configuration tends to reduce drastically backward radiation in the lossy Si substrates while providing greater upper radiating area thanks to the upper low permittivity structure.

This article is organized as follows: Section II describes the design and optimization of basic SIP antennas on 0.13 μm SiGe BiCMOS. Section III presents the implementation analysis. Section IV deals with radar antenna solution analysis and Section V gives some conclusions and perspectives.

II. IP INTEGRATED ANTENNA ON 0.13 μM SIGE BICMOS TECHNOLOGY

A) Antenna design

It has been demonstrated that above-IC process is compatible with SiGe BiCMOS technology [13, 16]. This is an alternative solution that offers opportunities and flexibility in terms of circuit integration. Indeed, a dielectric layer (polymer sheet or equivalent) is deposited on the top level of a SiGe BiCMOS wafer. Passive elements (transmission lines, passive functions) can therefore be integrated on this layer, reducing the previously induced Si losses because of the LR Si substrate vicinity. The radiation efficiency of antennas also reported on such additional lossless dielectric sheet can be significantly increased as its thickness (*h*) grows up. The E-field distribution is indeed mostly concentrated in this upper volume, therefore reducing the Si absorption phenomena on both guided and near-field radiated components.

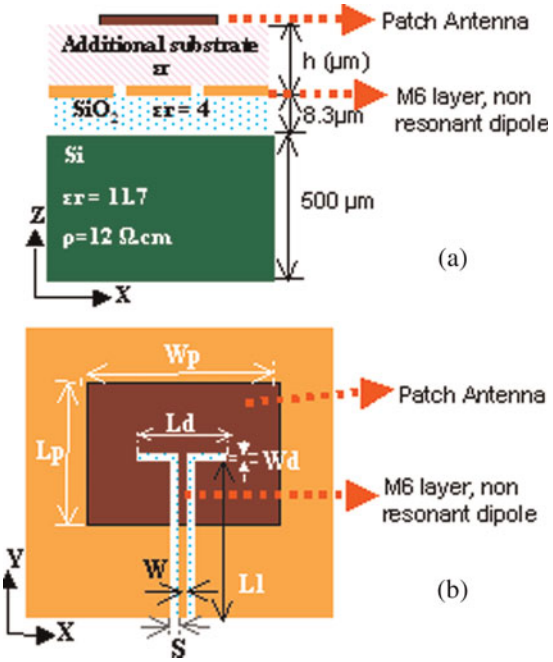

Fig. 1. SIP antenna on 0.13 μm SiGe BiCMOS technology. (a) Dielectric layers. (b) Antenna top view.

In [9], an efficient antenna combining above-IC process with 0.13 μm SiGe BiCMOS wafer is presented. Figure 1 shows the antenna topology. A non-resonant slot dipole is integrated on the last metallization layer of 0.13 μm SiGe BiCMOS process. This element excites a resonant structure (patch antenna) implemented on the above-IC dielectric layer. In this solution, a 30 μm thickness of benzocyclobutene (BCB) dielectric is used to implement the conventional patch antenna. The choice of the BCB polymer is due to its remarkable electrical and mechanical properties (low relative dielectric permittivity ($\varepsilon_r = 2.65$), planarity characteristics).

With this above-IC antenna solution, induced dielectric losses by the LR Si are hidden from an electromagnetic point of view. The simulation results (Fig. 2) show that the energy absorbed by the Si is reduced in a significant way. A 10.9 dB forward to backward radiation ratio is achieved with the above-IC solution compared with the 7.23 dB resulting from the "dipole on SiGe BiCMOS" configuration. In addition, the radiated performances (37.2% radiation efficiency – directivity gain: 2.65 dBi) are improved with respect to integrated SiGe antenna performances (10.39% radiation efficiency – directivity gain «0 dBi). However, a bandwidth reduction (2.05% at ROS = 2) is observed due the bandwidth dependence with respect to substrate thickness.

The additional above-IC polymer layer is the key element that provides suitable conditions: electrical area to achieve the required directivity and appropriate medium (low permittivity and low losses) for radiation efficiency. Optimizing integrated antennas requires consequently the use of such additional high performances dielectric layers with appropriate characteristic parameters.

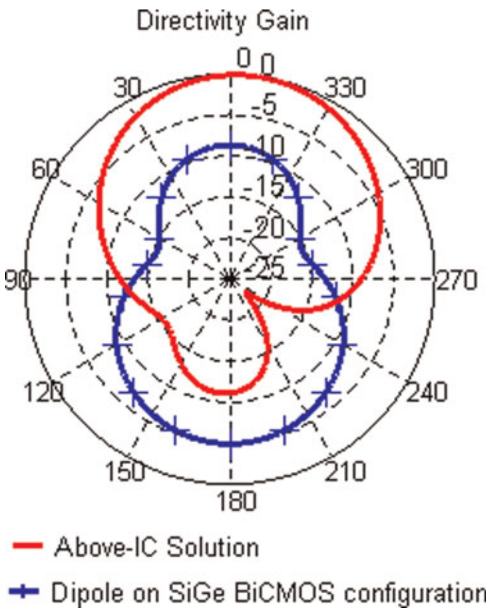

Fig. 2. Comparisons between above-IC solution and dipole on Si solution – normalized radiation patterns.

B) Substrate optimization

Antenna performances, in particular directivity gain and bandwidth, depend on the substrate properties (dielectric constant, and thickness). Figure 3 illustrates the performances of such integrated antenna for different substrate permittivities ($\varepsilon_r = 2.65, 4, 6{,}10$) and thicknesses (from 0.01 λg to 0.1 λg).

The results are obtained using IE3D^{TM} (New Zealand software). For each (ε_r, h) combination, the antenna is matched to 50 Ohms, with a resonant frequency at 79 GHz.

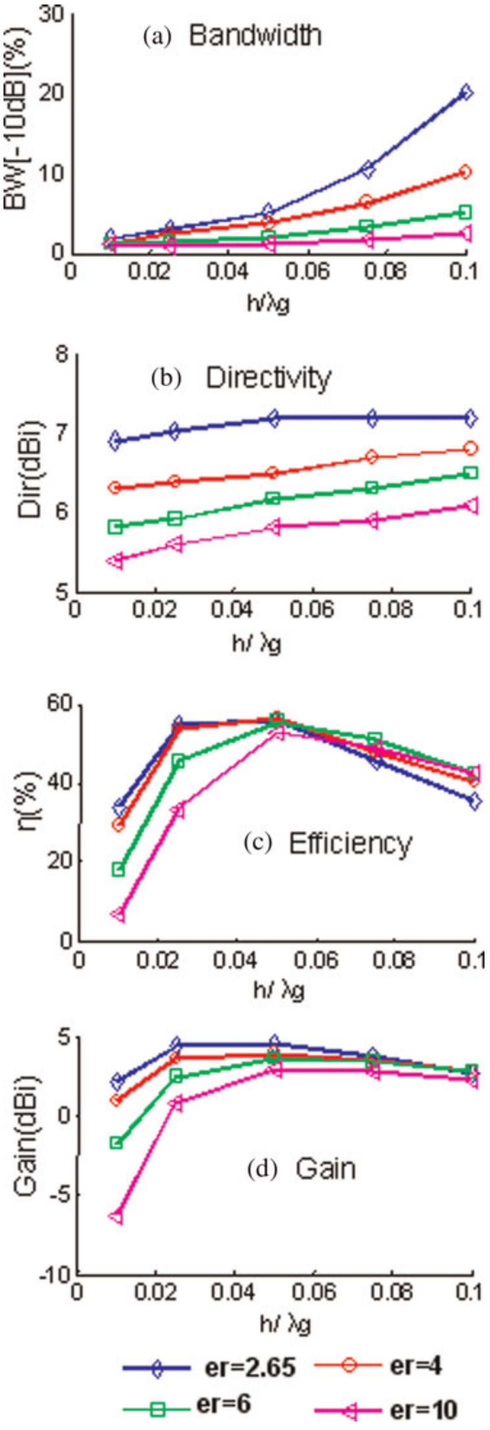

Fig. 3. Antenna performances for different (ϵ_r, h) configurations. (a) Bandwidth. (b) Directivity. (c) Radiation efficiency. (d) Gain.

The dipole and patch length (*Ld*, *Lp*) variations modify the resonant frequency while the dipole and patch widths (*Wd*, *Wp*) are used to control the input matching conditions.

Bandwidth, directivity, gain, and efficiency increase as the dielectric permittivity value decreases. Thick substrates contribute to improve bandwidth and directivity. However, the radiation efficiency is affected by both lower and higher thickness. An optimum thickness is about 0.05 λg, as mentioned in Fig. 3(c).

Choosing additional dielectric layer enhances integrated antenna performances, which become suitable with radar features. In the case of SRR radar applications, 5.06% bandwidth and 13 dBi gain are expected. Higher gain can be achieved by implementing an array antenna with a previously optimized above-IC basic antenna offering expected bandwidth and efficiency.

In this way, increasing the bandwidth of above-IC BCB antenna implies increasing thickness (Fig. 3(a)). Unfortunately, the conventional BCB technology has technical limitations according to the dielectric layer properties, limited to 30 μm. Then, SIP antenna configuration, using an additional substrate printed circuit board (PCB) layer remains an appropriate technological orientation for enhancing radiation performances.

III. IMPLEMENTATION ANALYSIS

The antenna is manufactured in two stages. First, the non-resonant dipole is implemented on a top metallization layer of a 0.13 μm SiGe BiCMOS wafer. The second step corresponds to the post-processing stage, where the radiated element, etched on the additional PCB or BCB substrate, is reported on the SiGe wafer.

This post-processing involves deposition, pasting or flip-chip techniques for mounting the PCB on the wafer. Technological parameters as alignment and air gap presence can cause electromagnetic degradations which must be evaluated. A parametric analysis of such sensitive factors using both IE3D^{TM} and HFSS^{TM} softwares is realized.

A) Alignment sensitivity

The two elements, i.e. the excitation dipole and the radiation patch, are electromagnetically coupled. They are manufactured using different process and assembled in a

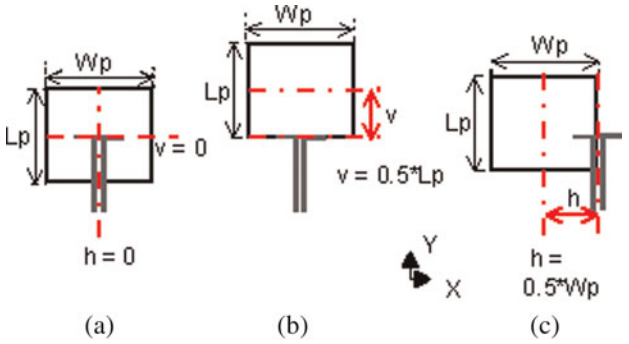

Fig. 4. Structure alignment. (a) Ideal alignment. (b) Y axis misalignment. (c) X axis misalignment.

post-processing. Misalignment between these two elements can appear. The sensitivity study is realized as follows.

Figure 4 displays the three studied cases. The first case corresponds to the ideal alignment when the excitation dipole is centered with respect to the patch (Fig. 4(a)). The second case is the misalignment in the E plane. The dipole is moving along the *Y*-axis, the "*v*" variable determining the distance between the center parts of the patch and the dipole (Fig. 4(b)). In the same way, the last case corresponds to misalignment in the H plane, the dipole is moving along *X*-axis and the "*h*" variable is the distance between the patch and the dipole (Fig. 4(c)).

The non-alignment diminishes coupling between the two elements. The magnetic field for the three studied cases is given in Fig. 5. As expected, the TM01 mode is clearly observed in ideal case (Fig. 5(a)). Magnetic field degradations are observed in misalignment situations, particularly with the *Y* axis default (Fig. 5(b)). In the case of misalignment in the *X*-axis, the TM01 mode is slightly observed (Fig. 5(c)). The antenna structure is more sensitive to misalignment in the *Y*-axis. This is related to the fact that the magnetic field mode is implicitly centered along the patch *Y*-axis (E plane).

The sensitivity analysis according to the matching conditions is shown in Fig. 6. Different "*v*" and "*h*" position values are evaluated. Figure 6(a) confirms that non-alignment in the E plane is an interfering parameter that causes mismatching impedance. On the other hand, H plane misalignment sensitivity remains low (Fig. 6(b)).

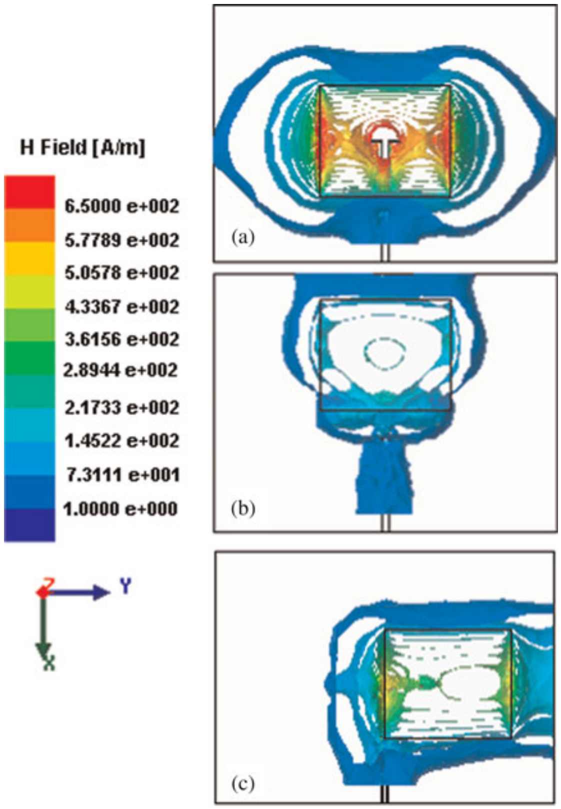

Fig. 5. Magnetic field alignment effect. (a) Magnetic field with perfectly aligned elements. (b) Magnetic field with *Y*-axis misalignement. (c) Magnetic field with *X*-axis misalignment.

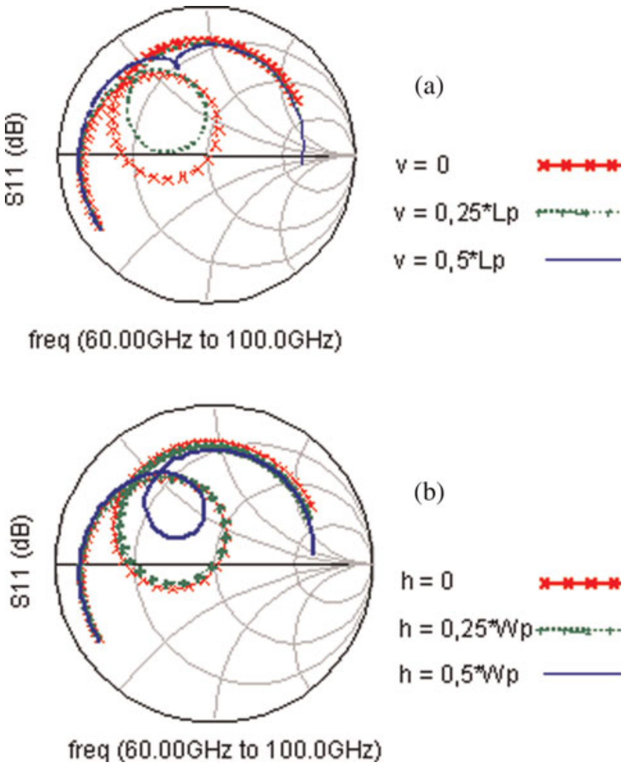

Fig. 6. Matching alignment effect. (a) Magnetic field in *Y* axis misaligned elements. (b) Magnetic field in *X* axis misaligned elements.

B) Air gap incidence study

Two post-processing solutions are considered to associate the SiGe wafer and the PCB substrates. Two elements can be pasted using dielectric glue or bumps by flip-chip process. An air gap can therefore appear in both conditions, which must be properly estimated and controlled.

Dielectric glue properties (permittivity and thickness) can affect the antenna matching conditions. Therefore, the antenna design should take into account these parameters. However, this air gap is not completely defined, and introduced some uncertainties in the antenna design, which must be evaluated and reduced.

The air gap thickness influence on matching antenna is shown in Fig. 7. Both frequency and matching impedance shift considerably with air gap incidence, even for a reduced gap value (10 μm). To maintain a perfect matching condition, the air gap thickness should be reduced.

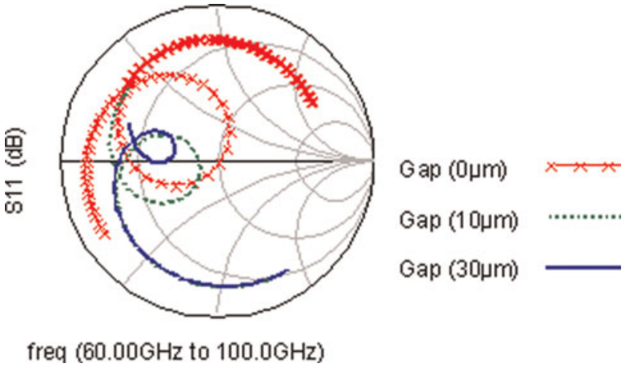

Fig. 7. Air gap matching effect.

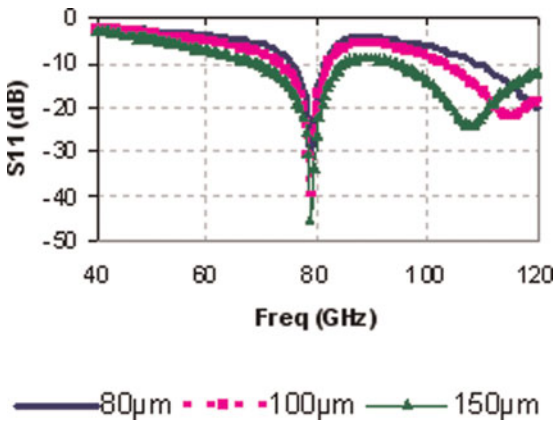

Fig. 8. Return loss of the antenna for different air gap thickness.

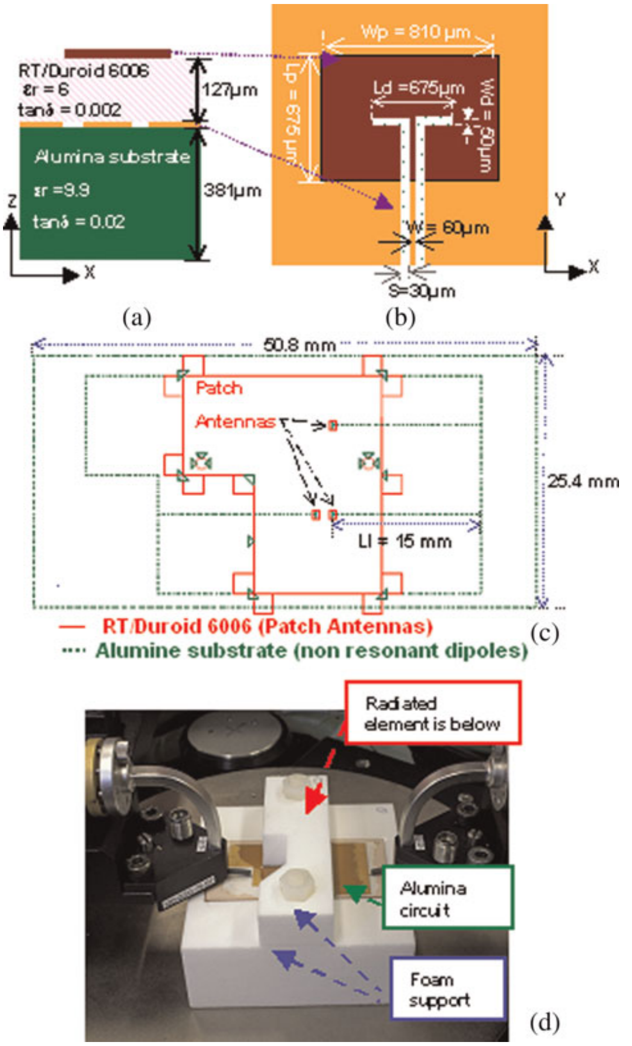

Fig. 9. Intermediate experimental structure. (a) Dielectric layers. (b) Antenna top view. (c) Layout view. (d) Alumina/foam structure.

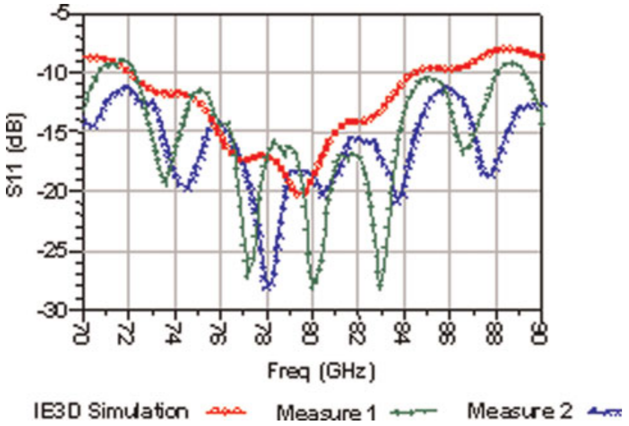

Fig. 10. S11 measured and simulated result.

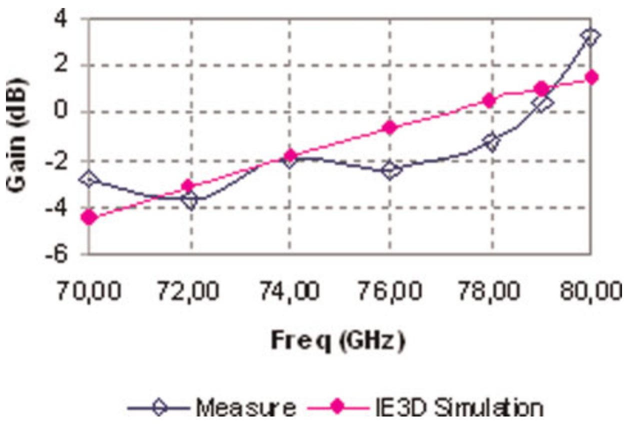

Fig. 11. Measured and simulated gain results. (Measurements were realized using a vector network analyzer MVNA6435.)

With the flip-chip approach, metallic bumps are used to connect Si and PCB circuits. The bumps provide spacing, preventing perfect electrical contact between the chip and substrate conductors. A simulation analysis is realized taking into account bumps height in the antenna design. Figure 8 shows return losses for antennas with different air gap thicknesses (80, 100, and 150 μm). As air gap grows new resonances at higher frequencies appear. That is because of the modifications on the patch antenna near environment.

A pasting approach seems more advisable than a flip-chip approach, because in pasting approach glue properties can be known. On the contrary, flip-chip approach has a stronger dependence on bump dimensions.

C) Intermediate experimental validation

An intermediate experimental structure is evaluated in order to validate the basic antenna principle. Having a first alignment control technique and air gap suppression procedure are key points for on-wafer post-processing. Figure 9 presents the manufactured structure. The non-resonant dipole is etched on an alumina substrate ($\varepsilon_r = 9.9$, $h = 381$ μm) and the radiated patch reported on RT/Duroid 6006 ($\varepsilon_r = 6$, $h = 127$ μm). The two elements are assembled maintained to each other using a foam support.

This structure was implemented and measured. Figures 10 and 11 show the results. The [S] parameter measurements were realized using a vector network analyzer (MVNA6435). A good agreement is obtained for return loss ($S11$) parameters (Fig. 10) and gain results (Fig. 11) (extracted from $S21$ measurements). Resonances observed for the $S11$ measurements are due to stationary wave phenomena, produced by antenna feeding lines (length 15 mm, $\sim 3\ \lambda o$).

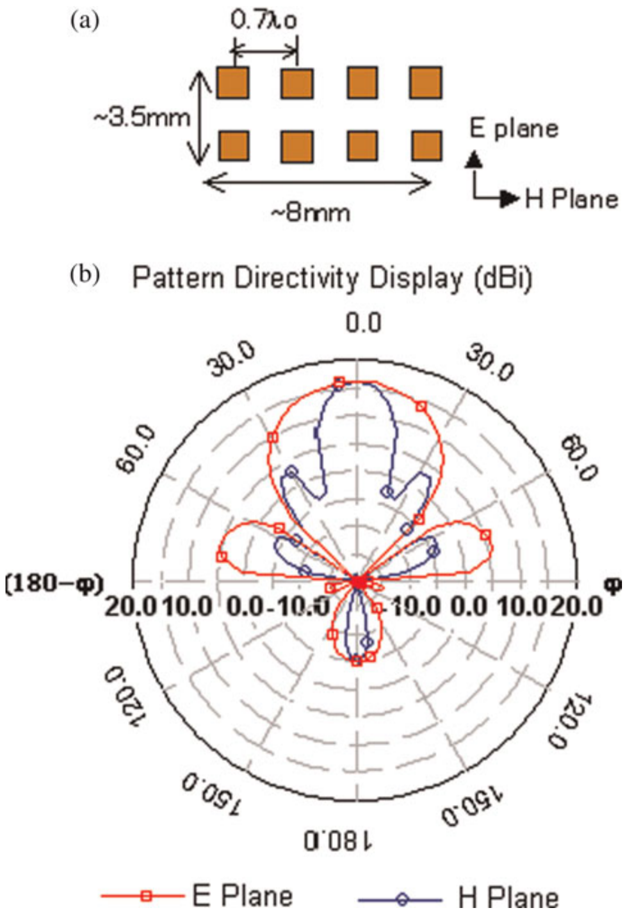

Fig. 12. SIP integrated array antenna. (a) 4 × 2 configuration dimensions. (b) Radiation pattern directivity.

IV. INTEGRATED ANTENNA ARRAY

Focusing on radar antenna solution, an array antenna is analyzed using the mathematical approach available on IE3D^{TM}. Mutual coupling effects are neglected in this numerical approximation. The SIP antenna proposed on 0.13 μm SiGe BiCMOS with RT/Duroid 6006 ($\varepsilon_r = 6$, $h = 127$ μm) is used as a reference antenna to build the integrated array.

A 4 × 2 array configuration, occupying a 28 mm^2 area, exhibits a 12.7 dBi gain. The simulation results are plotted in Fig. 12. This result is optimized regarding to the above-IC BCB antenna array because the Si area is reduced from 34 to 28 mm^2. Indeed, the SIP reference antenna has a smaller area because of PCB dielectric constant value ($\varepsilon_r = 6$). Besides the radiation performances (45% radiation efficiency – directivity gain: 2.93 dBi) are improved thanks to the substrate thickness.

V. CONCLUSIONS AND PERSPECTIVES

In this paper, an integrated antenna combining SIP and SOC approaches is presented. A radiated element is implemented on an SIP structure offering optimized antenna performances. An SIP antenna, using above-IC mounted commercial substrate (RT/Duroid 6006), offers enhanced performances with respect to SOC antenna and above-IC antenna on BCB. This reference antenna is used as a basic element for array implementation. The simulation results exhibit a 12.7 dBi gain for a 4 × 2 array antenna in 28 mm^2 Si surface.

The antenna topology has been studied. Misalignment and air gap presence can cause electromagnetic degradations and deviation with respect to expected electrical performances. However, these factors can be controlled and a parametric study has been engaged in order to validate the design rules and technological orientations.

The antenna principle has been validated by using an intermediated structure. The next issue concerns fully integrated Si antenna validation.

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Daniel Gloria received, in 1995, the engineering degree in Electronics from the Ecole Nationale Supérieure d’Electronique et de Radioélectricité and the M.S.E.E. in Optics, Optoelectronics and Microwaves Design Systems from the Institut National de Grenoble (INPG). He spent two years, from 1995 to 1997, in ALCATEL Bell Network System Labs, in Charleroi (Belgium) as an RF designer engineer and was involved in the development of the Cablephone RF front end and its integration in Hybrid-Fiber-Coax telecommunication networks. Since 1997, he has been working for ST Microelectronics, Technology R&D Crolles, TPS lab, where he is in charge of HF characterization and RF passives modeling group. His interests are in optimization of active and passives devices for HF applications in BiCMOS and CMOS advanced technologies.

Andreia Cathelin started her electronic studies at the Polytechnic Institute of Bucarest, Romania, and graduated from the Institut Supérieur d’Electronique du Nord (ISEN), Lille, France, in 1994. From 1994 to 1998, she prepared a Ph.D. thesis with IEMN/ISEN, Lille, France, and MS2 Company, Roubaix, France, on a fully integrated BiCMOS low-power–low-voltage FM/RDS receiver. From 1997 to 1998, she was with Info Technologies, Gradignan, France, working on analog and RF communications design. Since 1998, she has been with STMicroelectronics, Crolles, France, in the Central R&D Division. Her major fields of interest are analog filtering, RF systems for mobile communication solutions, and MEMS devices co-integration.

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Robert Plana (M'98–SM'08) was born in March 1964, in Toulouse, France. He received the Ph.D. degree on the noise modeling and characterization of advanced microwave devices (HEMTs, pseudomorphic HEMTs (pHEMTs), and HBTs) that includes reliability from the Laboratoire d'Analyse et d'Architecture des Systèmes (LAAS), Centre National de la Recherche Scientifique (CNRS), Toulouse, France, and Paul Sabatier University, Toulouse, France, in 1993. In 1993 he was an Associate Professor with LAAS, CNRS, where he began a new research area concerning the investigation of millimeter-wave capabilities of silicon-based technologies. More precisely, he has focused on the microwave and millimeter-wave properties of SiGe devices and their capabilities for low-noise circuits. In 1995, he began a new project concerning the improvement of the passives on silicon through the use of microelectromechanical systems (MEMS) technologies. In 1999, he worked with SiGe Semi-conductor, Ottawa, ON, Canada, where he was involved with low-power and low-noise integrated circuits for RF applications. In 2000, he was a Professor with Paul Sabatier University and the Institut Universitaire de France, and started a research team with LAAS, CNRS, in the field of microsystems and nanosystems for RF and millimeter-wave communications. The team's main interests are on the technology, design, modeling, test, characterization, and reliability of RF MEMS for low-noise and high-power millimeter-wave applications and the development of the MEMS integrated circuit (IC) concept for smart microsystems. He built a network of excellence in Europe in this field, "AMICOM," regrouping 25 research groups. He has authored or coauthored over 200 international journals and conferences. In 2004, he became the Deputy Director of the Information and Communication Department, CNRS. From January 2005 to January 2006, he was Director of the Information and Communication Department, CNRS. He currently heads a research group with LAAS, CNRS, in the field of microsystems and nanosystems for wireless communications. Dr. Plana was the recipient of the 1999 special award presented by the CNRS for his work on silicon-based technologies for millimeter-wave communications.