RESEARCH PAPER

A 77-GHz antenna and fully integrated radar transceiver in package

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A 77-GHz–directional folded dipole antenna integrated in an embedded wafer level ball grid array package is presented. For the characterization of the antenna, a frequency multiplier is embedded, which scales the 4.25-GHz input signal up to 76.5 GHz and allows the use of a commercial signal source. The antenna structure is manufactured at the metallic layer, in the fan-out area of the package, and is directly connected to the monolithically integrated transceiver. The gain of the antenna is about 7 dBi, measured over a large bandwidth of about 8 GHz. The combination of the frequency multiplier with a 77-GHz transceiver and the on-package antenna is a promising approach for a system-in-package to future radar modules for automotive radar applications. Such a module avoids 77-GHz transitions to the printed circuit board and hence simplifies the design and manufacturing of the radar sensor significantly.

I. INTRODUCTION

The improved capabilities and cost reduction of SiGe HBT technology and the increasing functionality and performance of silicon-based fully integrated circuits in the frequency range of 77 GHz have opened the door to automotive applications [1]. State-of-the-art radar frontends are based on bare-die monolithic microwave–integrated circuits (MMIC) mounted on a PCB with special mm-wave characteristics. The MMICs are glued into cavities to minimize the length of the bond-wires connecting the chip to the RF structures on the PCB, which is critical at a frequency of 77 GHz. High-precision processes for the manufacturing of the PCB, the placement and bond-wiring of the chip are necessary to achieve the high reliability required by automotive applications. While the increasing requirements in functionality and performance of automotive radar systems equalize the cost reduction due to a higher degree of integration of the core elements such as the microcontroller, the base-band circuitry, and the radar frontend, the PCB is the remaining part with the highest savings potential. Due to the integration of a frequency multiplier, a 77-GHz transceiver and an antenna into a package of no 77-GHz transitions from chip to PCB are necessary and the bare-die MMIC can be replaced by a packaged chip that allows the use of PCB substrates based on low-cost materials and reduces the complexity of the PCB significantly. While the integration of the frequency multiplier and the transceiver into an MMIC is straightforward,

the integration of the antenna is more difficult and demands further investigation in processing an antenna-on-chip (AoC) or antenna-in-package (AiP) solution. An improvement of the inherent poor radiation efficiency of on-chip antennas can be achieved by additional measures such as backside etching, focusing with superstrat material [2] or parasitic resonator elements [3]. Such special processing steps plus the packaging make the AoC solution less attractive than package-integrated antennas. Countless antennas on different substrates have been presented over the last few years with more or less capability for packaging with integrated circuits. Low-temperature co-fired ceramic (LTCC) has become popular as it offers low-loss dielectrics and easy integration of passives. The MMIC is connected with bond-wires [2] or flip-chip attached to the package [4]. A recently reported solution for mm-wave packages is the embedded wafer level ball grid array (eWLB) package. The chip is embedded in mold compound, the backside is covered with a protection layer and the area array solder balls are attached via the redistribution layer (RDL) to the active side of the chip. The antenna, the matching structure, and the connection to the chip are realized in one thin-film process step on the RDL, resulting in short and highly reliable transitions between chip and antenna. The antenna is placed at a certain distance to the chip in the fan-out area of the package. The integrated frequency multiplier with a multiplication factor of 18 [5] scales the 4.25-GHz input signal up to 76.5 GHz and hence simplifies the distribution of the local oscillator (LO) signal on the application PCB. The major advantage of this concept lies within the signal generation that is not a part of the MMIC and is no more a subject to technology parameter variations of the silicon process. The whole frequency synthesizer including the 4.25-GHz oscillator, the phase locked loop, as well as a frequency ramp generator can be integrated, for instance, in CMOS as it is done in mobile transceivers. The performance of the transmitter part

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depends on such synthesizer, which has to have a 25 dB better phase noise performance compared to state-of-the-art transceivers at 77 GHz [1, 6–8].

II. DESIGN

A) eWLB package concept

The eWLB package technology [9–11] combines the advantages of wafer level packages (WLP), such as smallest form factor, excellent electrical, and thermal performance, the ease of fabrication, and reduced assembly cost with an extended package area (fan-out) surrounding the silicon die. The fan-out area is available for solder balls, interconnects, and embedded passives such as planar inductors or antennas. The core process of the technology is the encapsulation of the silicon die. The edges of the bare-die silicon chip are embedded in mold compound as shown in Fig. 1. The backside of the package is covered with a protection layer. At the active side of the chip (fan-in area), as well as at the fan-out area of the package, a thin-film technology is used to realize the redistribution layer. A dielectric, protecting the active side of the chip, increases the thickness of the isolating layer, thus reduces parasitic coupling of the redistribution layer to the chip. The interconnecting elements to the gold pads of the chip are defined by openings in the dielectric and are applied by an electroplating process of the redistribution lines. A solder stop mask defines the landing pads for the balls. The diameter of the balls is 0.3 mm at a pitch of 0.5 mm. The package without balls is 0.5 mm thick and the distance of the RDL to the top metal of the PCB after soldering is about 0.18 mm.

B) Chip design

For the integration of a chip into an eWLB package, some constraints for the chip design have to be taken into account. The dimensioning of the die-size depends on the area needed for the chip layout and the position where the chip is placed in the ball-grid of the package. The minimization of the length of RF transition lines at the RDL determines the position of RF, as well as signal pads within the pad-frame of the chip. The circuitry is mainly designed for the characterization of the package-antenna with the focus on flat output power over a wide input frequency range with good suppression of unwanted harmonics. In addition to the input balun, amplifier and frequency multiplier chain presented in [5], a variable gain amplifier (VGA) for the regeneration of the single-ended 4.25-GHz input signal (LO_{IN}) and a transceiver as presented
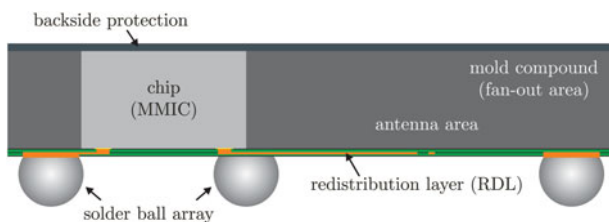

Fig. 1. Cross-section view of the embedded fan-out eWLB. The chip/package interconnection and the antenna structure are realized at a redistribution layer. The enlarged fan-out area allows spacing between the radiating element of the antenna and the highly conductive silicon chip.

in [6] are integrated, as depicted in Fig. 2(a). The single-ended output of the unbalanced VGA, connected to an output port (LO_{OUT}), enables the cascading of multiple chips. The main components of the transceiver are a switchable power amplifier (PA), a double-balanced mixer, and a rat–race coupler for separation of transmit and receive signal, which is connected to the antenna port (ANT). The circuit was designed and manufactured in a 200-GHz f_T Silicon–Germanium (SiGe:C) bipolar technology [12].

C) Package design

The package is mainly defined by the placement of the MMIC and the antenna, the arrangement of balls and the RDL layout. To realize an applicable package and keeping in mind that for signal routing within the package only one layer (RDL) is available, the design of the package and the pad-frame as well as the top-level layout of the chip are done in parallel. Some more boundary conditions are taken into account in the RDL layout, which is shown in the micrograph of the package in Fig. 2(b). Balls connected to signals are placed at the outer border of the package to simplify the routing of the PCB. Due to the parasitic influence of the RDL to RF signals, no RDL is routed and no ball is placed within the fan-in area except for thermo-balls. These thermo-balls make a direct vertical contact to the silicon substrate of the chip with a low thermal resistance and require a special pad structure at the chip where no active and passive elements can be placed. The connection of the 4.25-GHz signals to the chip (LO_{IN}, LO_{OUT}) is realized by a coplanar structure with a very short signal path at the RDL. The 77-GHz signal is provided by a ground-signal-ground-signal-ground (GSGSG) configuration with a pad-pitch of 0.1 mm requiring a taper and a matching structure to provide an interface with a differential impedance of 100 Ω for the simplification of the antenna design. The placement of the antenna is a compromise of a long distance between antenna and MMIC to minimize the influence of the silicon die to the radiation pattern and a short transition line for low transition losses.

D) Antenna design

In the first approach a well-known folded dipole antenna is designed and implemented in the package. The design and simulation are done in CST Microwave Studio with a simplified model of the package without the chip and a coplanar differential feeding line with 35 μm line width, 20 μm gap, and a simulated impedance of 100 Ω. The length of a dipole for maximum gain is given by half of the wavelength, which is 1.24 mm at 76.5 GHz, and an effective permittivity $\varepsilon_{r,eff}$ of about 2.5, which is not well known due to the different materials in the layer-stack of the package. A good matching to the feeding-line is reached by an additional loop connected to the dipole with a line-width of 30 μm.

III. MEASUREMENT

The performance of the antenna is defined by the radiation pattern in E- and H-plane and the frequency behavior of the antenna gain presented in Section III-A. To determine the achievable range measurement accuracy, a corner cube is moved to a variable distance in front of the radar sensor,
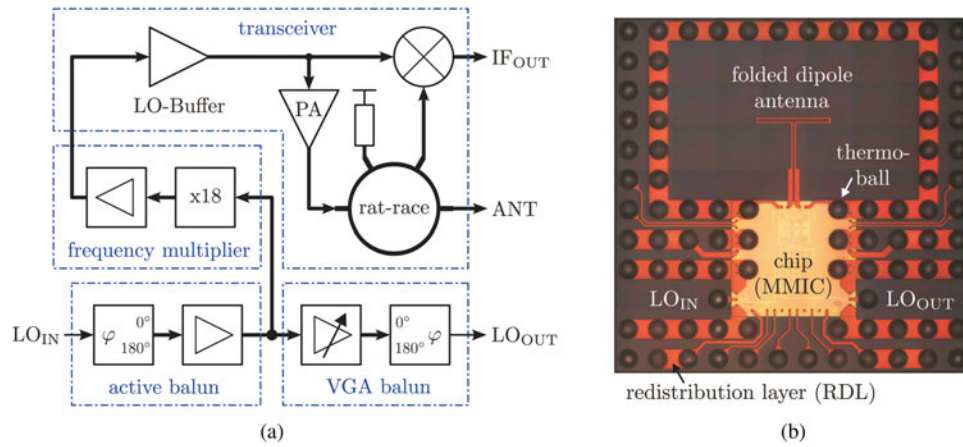
Fig. 2. Block diagram of the silicon chip integrated in the eWLB package, with the 4.25-GHz input signal (LO_{IN}) distribution, the frequency multiplier, the transceiver, and the VGA regenerating the signal for cascading of multiple chips (a) and micrograph of the bottom view of the proposed package with integrated antenna and MMIC with a package area of 6×6 mm² (b).

described in Section III-B. Each transceiver at the 2-channel frontend can act as a monostatic radar. When the transmitter (TX) and receiver (RX) antenna are not separated by a considerable distance, the system is called quasi-monostatic, as shown in Fig. 5(b) with ch2 as TX and ch1 as RX and vice versa. All measurements are made in an anechoic chamber to prevent multipath propagation and the remaining reflecting parts are covered with absorber material.

A) Antenna characterization

For the measurement of the antenna beam pattern, a PCB is designed, which allows undisturbed radiation to nearly the whole half-space. Therefore, all connectors are mounted at the back of the PCB and the board is placed at a certain distance to the rotary table. The 4.25-GHz input signal (LO_{IN}) is provided by an Agilent E8257D signal source. The receiver antenna, an E-band standard-gain horn, is mounted orthogonally to the PCB in the far-field and electrical boresight of the package-antenna (DUT) as shown in Fig. 3(a). The received power is measured by a Rohde & Schwarz FSQ40 (20–40 GHz) spectrum analyzer in combination with a Rohde & Schwarz FSZ90 harmonic mixer, which is connected to the receiver antenna.

The effective isotropic radiated power (EIRP) of the antenna in dBm is

$$P_{EIRP} = P_{OUT} + G_t, \tag{1}$$
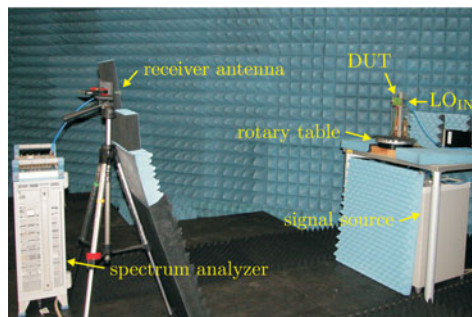
where G_t is the gain of the package-antenna and P_{OUT} the output power of the chip, which is measured on wafer at the single-ended in-phase and out-of-phase ports and superimposed to the differential value. The EIRP results from the measurement with the setup shown in Fig. 3(a) as

$$P_{EIRP} = P_r - G_r + L_{FS}, \tag{2}$$

where G_r is the gain of the receiver antenna, L_{FS} is the free-space loss, and P_r is the received power measured with the spectrum analyzer in dBm. The free-space loss in dB is defined as

$$L_{FS} = 20 \log_{10}\left(\frac{4\pi r f_{OUT}}{c}\right), \tag{3}$$

where r is the distance between the package and the receiver antenna and f_{OUT} is the frequency of the transmitted signal. The measurement of the beam pattern is done over $\pm 90°$ in E- and H-plane, where the E-Plane (azimuth) is perpendicular and the H-plane (elevation) is parallel to the feeding lines. In both planes, 0° is the direction of the electrical boresight of the antenna. For each step of the rotary table (0.5°), the received power at 76.5 GHz is measured with the spectrum analyzer.

1) RADIATION PATTERN
According to (1) the antenna gain includes the losses of the contacts to the chip pads, the taper with the matching structure and the feeding line of the antenna. For the simulation,
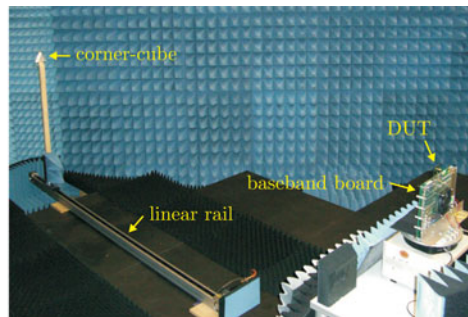
Fig. 3. These photographs show the setup for the antenna characterization (a) and an FMCW range measurement (b), done in the anechoic chamber.
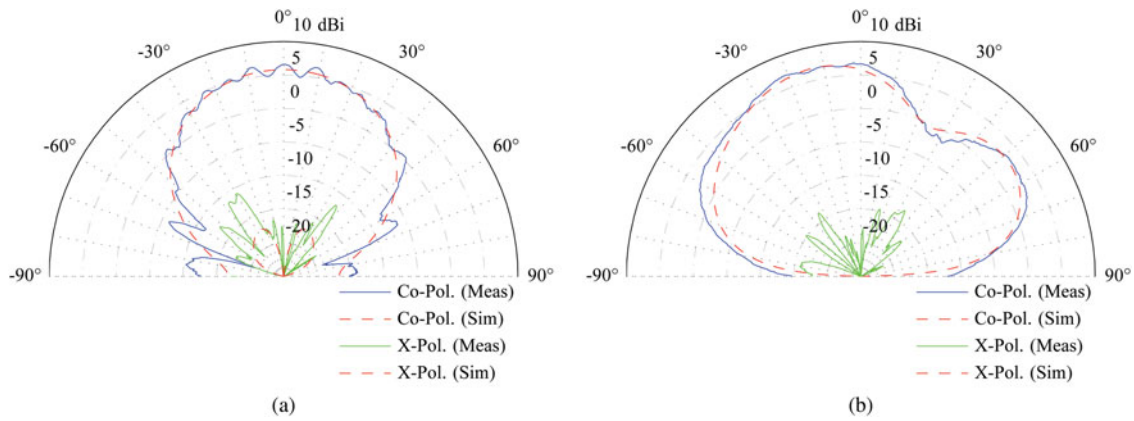
Fig. 4. Measured and simulated gain in *E*-plane (a) and *H*-plane (b) for co- and cross-polarization at a frequency of $f_{OUT} = 76.5$ GHz.

a section of the package and PCB, including the guarding balls surrounding the antenna and the silicon chip in full size, is used. The stimulus for the simulation is placed within the chip, at a transition line that is well known from the chip design. Elements and layers of the chip, influencing the transition such as the chip pad, the pad shielding, and the pad-compensation structure, are considered in the model. The simulated and measured radiation patterns at 76.5 GHz are presented in Figs 4(a) and 4(b). A fairly good agreement between simulation and measurement in co-polarization is obtained. The influence of the silicon die can be observed in Fig. 4(b) by a drop of the gain in the direction of 30° and as a consequence a lower signal-to-noise ratio (SNR) of a target within this area. The maximum sensitivity of the sensor is shifted by about $-10°$ in *H*-plane.

2) FREQUENCY BEHAVIOR

Fig. 5(a) shows the frequency behavior of the gain and the radiated power in co- and cross-polarization in the direction of the electrical boresight of the package-antenna. For automotive long-range radar (LRR) and short-range radar (SRR) applications, the frequency ranges from 76 to 77 GHz, respectively 77 to 81 GHz, are of interest. Within these ranges the radiated power P_{EIRP} is at a maximum and shows a good flatness. The gain of the package-antenna is calculated with (1) and is about 7 dBi over a wide frequency range. The

peak around 80 GHz in the characteristic of the gain can be explained by the measurement of P_{OUT}, which is done on-wafer, at a different chip than that molded into the package, and shows a drop of about 1 dB at 80 GHz. The on-wafer characterization at 77 GHz prior to the packaging process is disadvantageous due to the damage of the chip-pads caused by contacting the pads with probes. The condition of the pads has an impact on the quality of the connection to the RDL of the package, which affects especially the performance of the RF transitions.

B) FMCW range measurement

For the FMCW measurement two system-in-package (SiP) and a 4.25-GHz VCO are mounted on a PCB as shown in Fig. 5(b), forming a 2-channel radar frontend. The PCB (DUT) is connected to a baseband board on which the frequency ramp is generated and the intermediate frequency (IF) signal is amplified and analog to digital converted. The target, a corner-cube with a radar cross-section of 6.1 m² at 77 GHz, is mounted on a linear rail as shown in Fig. 3(b). For each range step of the linear rail and each channel sequentially acting as a transmitter, the IF of 500 frequency sweeps is measured. The bandwidth-limiting component in this system is the VCO that can be locked within a frequency range of 4.06–4.35 GHz resulting in a sweep-bandwidth at 77 GHz of
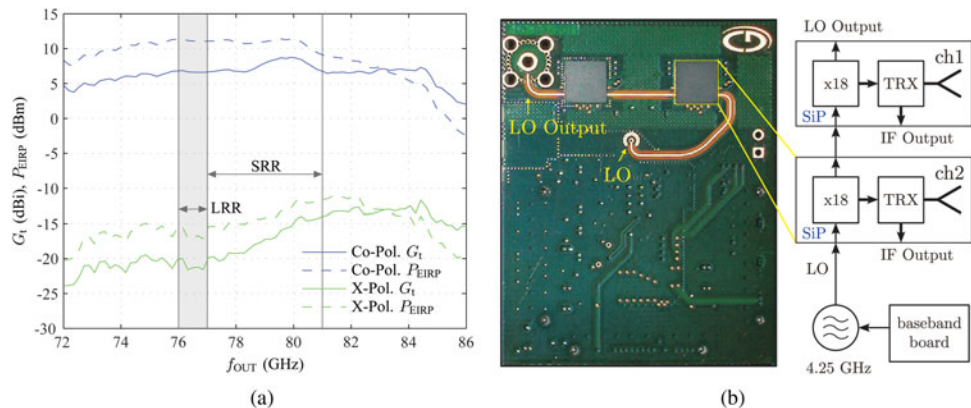

Fig. 5. Gain and EIRP of the package-antenna in co- and cross-polarization measured at 0° in *E*- and *H*-plane (a) and block diagram and PCB of a 2-channel radar frontend for FMCW range measurement (b).

$B = 5.2$ GHz, leading to a target resolution of the radar of

$$\Delta R = \frac{c}{2B} = 28.7 \text{ mm.} \quad (4)$$

The measured IF signal is evaluated by a discrete Fourier transformation (DFT), resulting in the magnitude spectrum versus the normalized frequency, which can be expressed as

$$\psi = \frac{\tau B}{N}, \quad (5)$$

where τ is the delay of the frequency sweeps at the LO and RF ports of the mixer and N is the amount of sampling points. The range of an FMCW radar is defined as

$$R = \frac{\tau_R c}{2}, \quad (6)$$

where τ_R is the round-trip delay-time. By neglecting the delays in the receive and transmit paths within the radar frontend τ equals τ_R and the range is

$$R = \frac{\psi N c}{2B}. \quad (7)$$

With $N = 1250$, the unambiguous range is $R_{MAX} = 18$ m. The range estimation of the target is done by a combination of DFT and chirp z-transform.

1) PEAK ESTIMATION

Fig. 6(a) shows the magnitude spectrum (blue) of a single frequency ramp with the target at $R = 4$ m and the noise density of the receiver, measured in the anechoic chamber with all transmitters turned off (red). The estimation of the target range delivers the peak value of the received signal as well. Fig. 6(b) shows the mean of the estimated peak value versus the range for monostatic (green) and quasi-monostatic operation (blue). In monostatic operation, the signal is transmitted and received by the same channel (ch1), and separated by the rat–race coupler within the transceiver. Due to the leakage of the transmitted signal to the RF input of the mixer, caused by the finite isolation of the coupler and the matching of the antenna, a high DC–level is generated at the IF output, which degrades the gain, by about 4 dB, as well as the noise-figure of the mixer. A good agreement between the simulation of the received power level and the measurement in quasi-monostatic operation (blue) is observed.

2) RANGE ESTIMATION

In the quasi-monostatic mode with cascaded LO distribution as shown in Fig. 5(b), the LO signal at ch1 is delayed by the propagation delay of the amplifier τ_{Amp} at ch2, regenerating the LO signal, and the signal propagation delay of the transition line between the SiPs τ_{TL}. With ch1 acting as a receiver, the signal at the RF port of the mixer is delayed by the round-trip delay-time τ_R and the LO signal by $\tau_{Amp} + \tau_{TL}$

$$\tau_1 = \tau_R - (\tau_{Amp} + \tau_{TL}) \quad (8)$$

and hence the estimated range is decreased, which is observed by the mean error in Fig. 7(a) (solid blue). With ch2 as receiver, the RF signal is additionally delayed by $\tau_{Amp} = \tau_{TL}$

$$\tau_2 = \tau_R + (\tau_{Amp} + \tau_{TL}). \quad (9)$$

and the estimated range is increased (Fig. 7(a)) (dotted blue). The range of the monostatic system, calculated by (7), is very accurate as depicted by the mean error in Fig. 7(a). The standard deviation of the estimated range is in the sub-millimeter range for the quasi-monostatic measurement as shown in Fig. 7(b), which is comparable with systems with much larger antennas as summarized in [13] and reported in [14]. The characteristic of the monostatic measurement (green) shows a degradation by the factor of 2.3, resulting in a difference of about 7.5 dB. The increase of standard deviation matches with the decrease of SNR, mainly caused by the degradation of the mixer noise-figure, which is about 7 dB. The maximum detectable range is 10 m for the quasi-monostatic, respectively, 6.4 m for the monostatic operation.
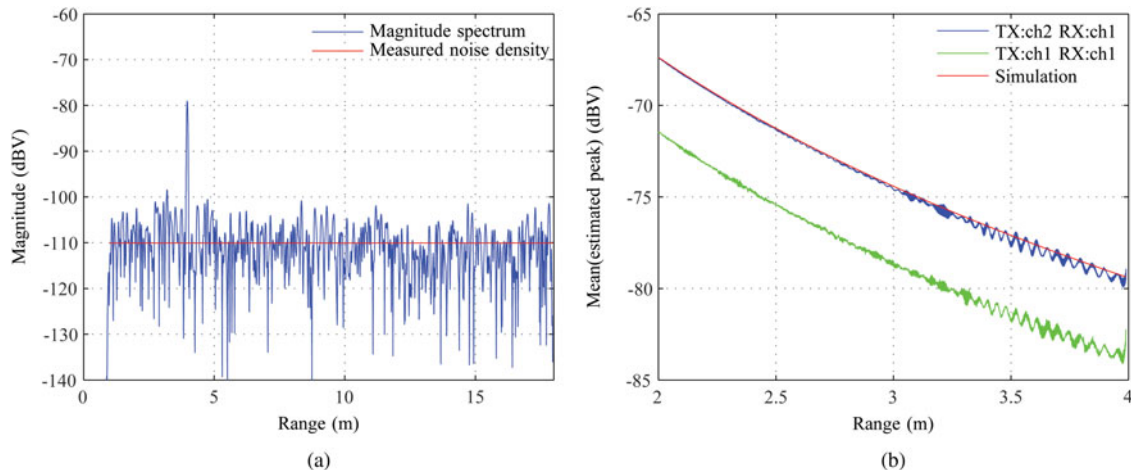

Fig. 6. Magnitude spectrum of a single frequency ramp with the target at $R = 4$ m (blue), measured noise density of the receiver (red) (a), mean of the estimated peak level for quasi-monostatic (blue) and monostatic operation (green), and the simulated peak level (red) (b).
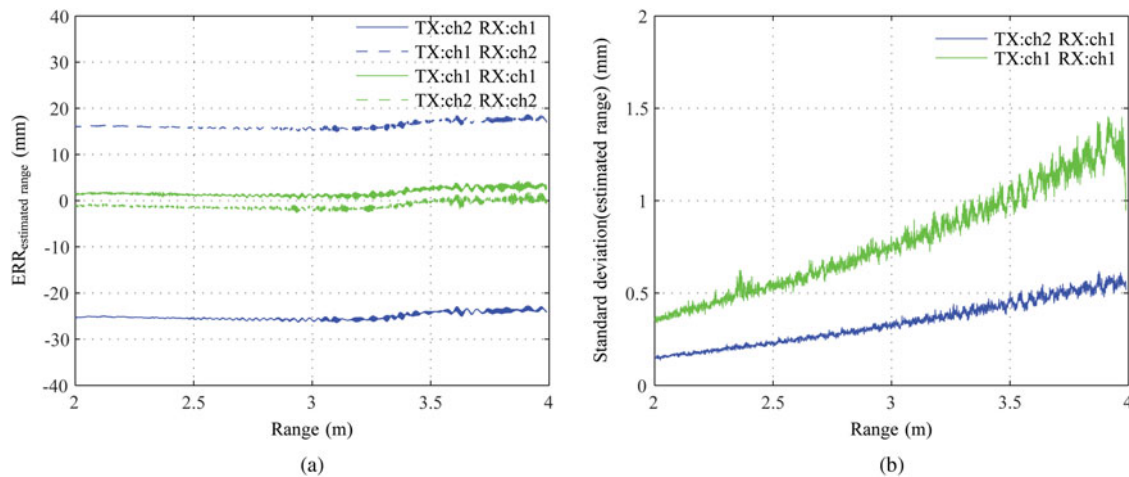
Fig. 7. Absolute error of the estimated range (a) and standard deviation of the estimated range (b).

VI. CONCLUSION

A directional folded dipole antenna in the 77-GHz band integrated in an embedded wafer level ball grid array package is presented. The antenna structure is manufactured at the redistribution layer, in the fan-out area of the package, and directly connected to a monolithically integrated transceiver. The advantages of the eWLB technology, which are low permittivity of the mold material, highly reliable structuring of the RDL down to 20 μm, and shortest possible distances between active and passive components, are reflected in the excellent performance of the antenna. The gain of the antenna is about 7 dBi in the direction of the main lobe, measured over a large bandwidth of about 8 GHz. The integrated frequency multiplier enables the reduction of the frequency of the signal supplied by an external voltage controlled oscillator to 4.25 GHz, which allows a very easy handling of the package and decreases the requirements for the PCB significantly. The combination of the frequency multiplier and the transceiver with the on-package antenna is a promising approach to future automotive as well as single package industrial radar sensors. The phase-noise at 100 kHz offset frequency of the presented system, supplied with a commercial available 4.25-GHz frequency synthesizer, is measured at −77 dBc/Hz and is comparable to state-of-the art 77-GHz transceiver with −74 dBc/Hz [1, 7] and −80 dBc/Hz [8, 15], respectively.

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