

## RESEARCH PAPER

# Flexible and miniaturized power divider

FRANÇOIS BURDIN, FLORENCE PODEVIN AND PHILIPPE FERRARI

*A new flexible and miniaturized power divider (PD), based on the Wilkinson PD topology, is carried out in this paper. Flexibility and size reduction are achieved simultaneously thanks to both an open-stub loading the input port and additional transmission lines (TLines) connecting the output ports to the isolation resistance. Design equations and rules are given. As a proof-of-concept, two PDs working at 2.45 GHz were fabricated and measured. Then, on the basis of the previous developments, a 1:4 power-dividing feeding network was realized. It highlights the high performance and flexibility of the proposed PD. Agreement between simulation and measurement results is very good, for PDs as well as for the feeding network, thus validating the proposed approach. This concept is straightforward to be applied at higher frequencies, in particular in the millimeter-wave range on CMOS technologies, where flexibility in the choice of the TLines characteristic impedances and size reduction are mandatory.*

**Keywords:** Wilkinson power dividers, Flexibility, Miniaturization

Received 1 August 2014; Revised 26 January 2015; Accepted 30 January 2015; first published online 23 March 2015

## I. INTRODUCTION

Power dividers (PDs) are key devices in communication systems for differential power amplification or antenna arrays feeding purposes. Wilkinson PDs constitute efficient components thanks to high isolation between the output ports, and easy design when dealing with planar structures [1, 2].

However, they suffer from a lack of flexibility, (i) when connecting the resistance necessary for isolation between the output ports, and (ii) in the choice of the characteristic impedance of the quarter-wave length arms. They also suffer from a large surface area, with two quarter-wave length transmission lines (TLines). In [3], the authors added extra TLines for connecting the isolation resistance. This avoids parasitic coupling between the two out ports, which constitutes a real drawback when dealing with millimeter-wave frequencies. More recently, a general model was developed to give design rules for the synthesis of these additional TLines [4]. A large variety of characteristic impedances can be chosen in such a way that various power ratios between the out ports can be reached. In [5], the quarter-wave length arms of the conventional impedance transformer were miniaturized thanks to the use of open stubs and/or step impedances. This also enhanced flexibility in the choice of the TLines characteristic impedance. In counterpart, this topology leads to a complex impedance transformation instead of the classical real one. Hence, a capacitance must be added in series with the resistance of the isolation branch so as to compensate the imaginary part.

Miniaturization and flexibility in design are of higher interest. Size reduction is important, for cost reasons, at RF frequencies in PCB technologies, and, even more important, at millimeter-waves in CMOS technologies, where distributed circuits based on TLines are used, as explained in [3]. In that case, the PDs must be both efficient and compact, and offer design flexibility. In particular, the choice of the characteristic impedance of the TLines is critical. As discussed in [6], the quality factor of the TLines realized in the Back-End-Of-Line of a CMOS technology strongly depends on their characteristic impedance. It is thus mandatory to develop flexible topologies for which the optimal characteristic impedance can be chosen. In this context, PDs proposed in [3] suffer from their bigger surface compared with the classical Wilkinson one (Fig. 1(a)). This is due to the extra length of TLines 1 since  $\theta_1 = \theta_3 + 90^\circ$ , as shown in Fig. 1(b). Capacitive or stub loading at the three ports of Fig. 1(a) enables size reduction, 53 or 74%, respectively, as shown in [7, 8]. A design procedure was proposed in [7] but it did not consider the isolation resistance feeding TLines. Another solution based on a  $\Pi$ -type stub in the parallel arms, instead of classical TLines, reduces the PD size as well [9]. However, such PDs need TLines with high characteristic impedance, which constitutes a drawback with CMOS technologies. Besides, the design is complicated by a strong meandering to get high miniaturization. Hence, no solution includes at the same time flexibility, reduced-size, and high-performance.

In this paper, it is shown that flexibility and high-performance can be addressed simultaneously. The novel design method proposed by the authors consists in searching sets of solutions that enable to reach targeted high electrical performances. The authors developed simple design equations to extract three essential design parameters, which could potentially become solution sets. They also demonstrated that one criterion is enough to complete the search for

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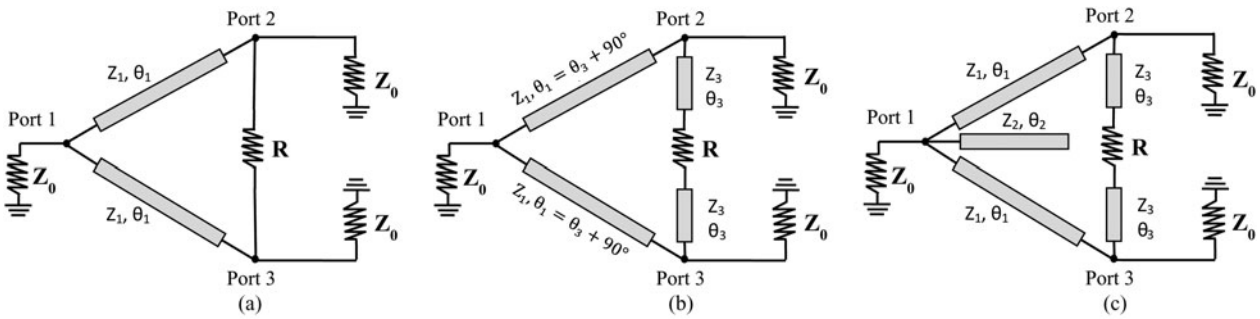


Fig. 1. (a) Wilkinson PD. (b) Modified PD [3]. (c) Modified PD with open stub, the proposed solution.

solutions. Theory and design equations are addressed in Section II. Then a design procedure is described in Section III, and finally experimental results are given in Section IV, showing a very good agreement between measurement and simulation results. They are compared with others' work in Section V.

## II. THEORY AND DESIGN EQUATIONS

Figure 1(c) gives the proposed PD topology. Compared with the one presented in [3] (Fig. 1(b)), an open stub of characteristic impedance  $Z_2$  and electrical length  $\theta_2$  was added at port 1. The characteristic impedance and electrical length of the arms between ports 1 and 2 (or ports 1 and 3) were named  $Z_1$  and  $\theta_1$ , while the ones connecting the output ports to the resistor were named  $Z_3$  and  $\theta_3$ . When both TLine ( $Z_3, \theta_3$ ) and open stub ( $Z_2, \theta_2$ ) are used, perfect matching at all ports and perfect isolation cannot be achieved. However, they can be brought close to zero by means of the design procedure explained in the next section. Matching and isolation will be slightly degraded compared with the classical Wilkinson topology, but the corollary will be an extended bandwidth as demonstrated by Fano, as a general rule and for any kind of circuit, in [10].

For simplicity, all the characteristic impedances were normalized to the system characteristic impedance  $Z_0$ , i.e.  $z_i = Z_i/Z_0$  and  $r = R/Z_0$ . An "even-odd mode" analysis was carried out considering the circuit symmetry, as illustrated in Fig. 2.

The open stub was replaced by two parallel open stubs with a characteristic impedance  $2z_2$ . Similarly, port 1 impedance

was doubled. The plane of symmetry cut out the resistance  $r$  in two, so that it should be replaced by two series resistances of value  $r/2$ . When given  $Z_0$  and  $r$ , the two circuits, corresponding to even and odd modes, totalize six unknown variables for the three TLines ( $z_i, \theta_i$ ), so that six independent equations are required to find the solutions.

To facilitate the understanding, the even and odd analyses are carefully described. For easier reading, Table 1 in Section II.C summarizes the theoretical results.

### A) Even-mode analysis

For even-mode excitation, the voltages at ports 2 and 3 have similar magnitude and phase. No current flows through the resistance  $r/2$  which is open circuited. The value of the impedances  $z_{IN2-e}$  and  $z_{IN3-e}$  looking toward the open stubs ( $z_2, \theta_2$ ) and ( $z_3, \theta_3$ ), in Fig. 2, are:

$$z_{IN2-e} = -jz_2 \cot(\theta_2), \tag{1}$$

$$z_{IN3-e} = -jz_3 \cot(\theta_3), \tag{2}$$

$z_{IN2-e}$  is parallel to port 1 impedance. The equivalent impedance  $z_{eq1-e}$  is given by equation (3):

$$z_{eq1-e} = \frac{2z_2}{z_2 + j \tan(\theta_2)}. \tag{3}$$

The impedance  $z_{IN4-e}$  is then derived as follows:

$$z_{IN4-e} = z_1 \frac{z_{eq1-e} + jz_1 \tan(\theta_1)}{z_1 + jz_{eq1-e} \tan(\theta_1)}. \tag{4}$$

Impedance  $z_{IN4-e}$  is parallel to  $z_{IN3-e}$  and should be equal to

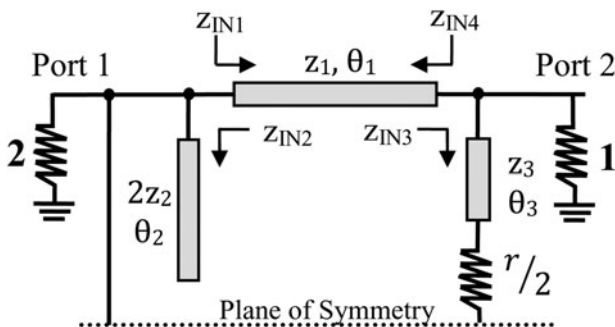


Fig. 2. Half of the normalized topology shorted within the odd-mode and open within the even-mode. Normalized impedances and resistance are considered.

Table 1. Theoretical description summary.

Given	$r$
Given	$z_1, z_2, z_3$
Calculated	$\theta_3 = \tan^{-1} \left( \frac{\sqrt{-(r/2) + 1}}{\sqrt{(2z_3^2/r) - 1}} \right)$
Calculated	$\theta_1 = \tan^{-1} \left( \frac{z_3 \tan(\theta_3)}{z_1 (r/2 - 1)} \right)$
Calculated	$\theta_2 = \tan^{-1} \left( \frac{z_2}{z_3 \cot(\theta_3) + z_1 \tan(\theta_1)} \right)$
Condition	$r > 2$ with $z_3 < \sqrt{\frac{r}{2}}$

port 2 impedance to get a matching condition at port 2, leading to equation (5):

$$\frac{1}{z_{IN3-e}} + \frac{1}{z_{IN4-e}} = j \frac{\tan(\theta_3)}{z_3} + \frac{z_1 + jz_{eq1-e} \tan(\theta_1)}{z_1 z_{eq1-e} + jz_1^2 \tan(\theta_1)} = 1. \quad (5)$$

From (5), the real and imaginary parts of the two members of the equation are split in two complex equations. Equation (6) is obtained by equating the real parts, while equation (7) corresponds to the imaginary parts.

$$\begin{aligned} z_1 z_2^3 z_3 - 3z_1^2 z_2^2 z_3 \tan(\theta_1) \tan(\theta_2) + z_1^2 z_3 \tan(\theta_1) \tan(\theta_2)^3 \\ = -z_1 z_2 z_3 \tan(\theta_2)^2 - 4z_2^2 z_3 \tan(\theta_1) \tan(\theta_2) \\ - 4z_1 z_2^2 \tan(\theta_2) \tan(\theta_3) - z_1^2 z_2^3 \tan(\theta_1) \tan(\theta_3) \\ + 3z_1^2 z_2 \tan(\theta_1) \tan(\theta_2)^2 \tan(\theta_3), \end{aligned} \quad (6)$$

$$\begin{aligned} z_1 z_2^2 z_3 \tan(\theta_2) + z_1^2 z_2^3 z_3 \tan(\theta_1) - 3z_1^2 z_2 z_3 \tan(\theta_1) \tan(\theta_2)^2 \\ = z_1 z_3 \tan(\theta_2)^3 + 2z_2^3 z_3 \tan(\theta_1) - 2z_2 z_3 \tan(\theta_1) \tan(\theta_2)^2 \\ + 2z_1 z_2^3 \tan(\theta_3) - 2z_1 z_2 \tan(\theta_2)^2 \tan(\theta_3) \\ - 3z_1^2 z_2^2 \tan(\theta_1) \tan(\theta_2) \tan(\theta_3) \\ + z_1^2 \tan(\theta_1) \tan(\theta_2)^3 \tan(\theta_3). \end{aligned} \quad (7)$$

Similarly, impedance  $z_{IN3-e}$  looking toward TLine ( $z_3, \theta_3$ ) is parallel to port 2 impedance, so that the equivalent impedance named  $z_{eq2-e}$  is:

$$z_{eq2-e} = \left( 1 + \frac{1}{z_{IN3-e}} \right)^{-1} = \frac{-jz_3 \cot(\theta_3)}{1 - jz_3 \cot(\theta_3)}, \quad (8)$$

$z_{IN1-e}$  is the input impedance of TLine ( $z_1, \theta_1$ ) loaded by  $z_{eq2-e}$  given by (9):

$$z_{IN1-e} = z_1 \frac{z_{eq2-e} + jz_1 \tan(\theta_1)}{z_1 + jz_{eq2-e} \tan(\theta_1)}. \quad (9)$$

The combination of  $z_{IN1-e}$  parallel to  $z_{IN2-e}$  should be equal to port 1 impedance to obtain a matching condition at port 1, leading to equation (10):

$$\begin{aligned} \frac{1}{z_{IN1-e}} + \frac{1}{z_{IN2-e}} &= \frac{z_1 + jz_{eq2-e} \tan(\theta_1)}{z_1 z_{eq2-e} + jz_1^2 \tan(\theta_1)} + j \frac{\tan(\theta_2)}{2z_2} \\ &= \frac{1}{2}. \end{aligned} \quad (10)$$

By developing and equating the real and imaginary parts of the two members of equation (10), equations (11) and (12) are derived:

$$\begin{aligned} z_1 z_3 \tan(\theta_2) \cot(\theta_3) - z_1^2 \tan(\theta_1) \tan(\theta_2) \\ + 2z_1 z_2 + 2z_2 z_3 \tan(\theta_1) \cot(\theta_3) = z_1^2 z_2 z_3 \tan(\theta_1) \cot(\theta_3), \end{aligned} \quad (11)$$

$$\begin{aligned} z_1 z_3 \tan(\theta_1) \tan(\theta_2) \cot(\theta_3) - z_2 z_3 \cot(\theta_3) \\ = z_1 z_2 \tan(\theta_1). \end{aligned} \quad (12)$$

Finally, the even-mode analysis leads to four different equations, (6), (7), (11), and (12).

### B) Odd-mode analysis

For the odd-mode analysis, the voltages at ports 2 and 3 have the same magnitude and are 180° out of phase. The voltage is consequently null along the plane of symmetry of the circuit which can be thus short circuited in its middle part. The impedance looking toward the circuit from port 2 can be calculated through the impedances  $z_{IN3-o}$  and  $z_{IN4-o}$ :

$$z_{IN3-o} = z_3 \frac{r/2 + jz_3 \tan(\theta_3)}{z_3 + jr/2 \tan(\theta_3)}, \quad (13)$$

$$z_{IN4-o} = jz_1 \tan(\theta_1). \quad (14)$$

The combination of these two parallel impedances should match port 2 impedance, which leads to the following equation (15):

$$\frac{1}{z_{IN3-o}} + \frac{1}{z_{IN4-o}} = \frac{z_3 + j(r/2) \tan(\theta_3)}{z_3(r/2) + jz_3^2 \tan(\theta_3)} - j \frac{\cot(\theta_1)}{z_1} = 1. \quad (15)$$

Equations (16) and (17) are obtained by equating the real and imaginary parts of equation (15), respectively:

$$z_3 \cot(\theta_1) \tan(\theta_3) = z_1 \left( \frac{r}{2} - 1 \right), \quad (16)$$

$$-z_3 \cot(\theta_1) \cot(\theta_3) = z_1 \left( \frac{2}{r} z_3^2 - 1 \right). \quad (17)$$

Next, equation (16) is substituted into (17) in order to get:

$$\theta_3 = \tan^{-1} \left( \sqrt{\frac{-(r/2) + 1}{(2z_3^2/r) - 1}} \right), \quad (18)$$

which implies the following condition on  $r$  according to  $z_3$ :

$$\text{if } r < 2, \text{ then } z_3 > \sqrt{\frac{r}{2}}; \text{ or if } r > 2, \text{ then } z_3 < \sqrt{\frac{r}{2}}. \quad (19)$$

What is more, equation (16) can be rewritten as follows:

$$\theta_1 = \tan^{-1} \left( \frac{z_3 \tan(\theta_3)}{z_1 (r/2 - 1)} \right). \quad (20)$$

From equation (20), it is obvious that the value of  $r$  cannot be lower than 2, which would lead to a negative value of the electrical length  $\theta_1$  or an electrical length longer than a quarter wavelengths which is not acceptable. Thus, the right condition among the two suggested in equation (19) is:

$$r > 2 \text{ with } z_3 < \sqrt{\frac{r}{2}}. \quad (21)$$

Meanwhile equation (12) can also be rewritten as follows:

$$\theta_2 = \tan^{-1}\left(\frac{z_2}{z_3 \cot(\theta_3)} + \frac{z_2}{z_1 \tan(\theta_1)}\right). \quad (22)$$

### C) Theory and design equations summary

It is remarkable that equation (18) gives  $\theta_3$  versus  $r$  and  $z_3$  only, equation (20) gives  $\theta_1$  versus  $r$ ,  $z_1$ ,  $z_3$ , and  $\theta_3$ , and equation (22) gives  $\theta_2$  versus  $z_1$ ,  $z_2$ ,  $z_3$ ,  $\theta_1$ , and  $\theta_3$ . Table 1 summarizes the theoretical description to calculate easily the length parameters of the three TLines as a function of initial parameters.

### III. DESIGN PROCEDURE

With an adequate procedure, it seems possible to find, in that order, the TLines electrical lengths  $\theta_3$ ,  $\theta_1$ , and  $\theta_2$  which solely depend on  $z_1$ ,  $z_2$ ,  $z_3$ , and  $r$ . A set of solutions consists in a fixed  $r$  and the three values  $z_1$ ,  $z_2$ , and  $z_3$ . For a given  $r$ , the exact solution of the six equations, (6–7), (11–12), and (16–17) is reached in the particular case  $\theta_2 = 0$ , i.e. without open stub. This case is already known and does not lead to miniaturization. More precisely, those six equations were obtained by considering perfect matching on port 1 for the even mode ( $S_{11_e} = 0$ ) and perfect matching on port 2 for both even and odd modes ( $S_{22_e} = 0$ ) and ( $S_{22_o} = 0$ ). In the

Appendix, we show that this is equivalent to having a perfect matching on port 2 only ( $S_{22} = 0$ ). We show as well that considering ( $S_{22} = 0$ ) is equivalent to have both matching at all ports and perfect isolation. Consequently a close solution corresponds to  $S_{22}$  as close to 0 as possible. Meeting the criterion  $|S_{22}| < S_{22\_max}$  means that the initial set of  $z_1$ ,  $z_2$ , and  $z_3$  corresponds to valid characteristic impedances for a compromise solution within the defined limits.

Hence, even if a perfect set of characteristic impedances cannot be found, there are some sets that enable to go as close as possible to the ideal solution, depending on  $S_{22\_max}$ . Equations (6), (7), and (11) are too complex to be solved in an algebraic way with equations (18), (20), and (22), so that only the three last are used. The “approximate solutions” can be obtained thanks to the use of a simple algorithm. It consists in calculating  $S_{22}$  and to compare it with  $S_{22\_max}$ , to be fixed as low as possible. On the basis of the demonstration in the Appendix,  $|S_{22}| < S_{22\_max}$  means that  $S_{22}$  is as close to zero as possible which implies that  $S_{11}$  and  $S_{23}$  are also close to 0. The maximum values that  $|S_{11}|$  or  $|S_{23}|$  can reach are not easy to express as a function of  $S_{22\_max}$  since they will depend on both real and imaginary parts of  $S_{22}$  but the tendencies are the same: being close to 0.

It is easy to derive  $S_{22}$  from Fig. 2.  $S_{22}$  is the sum of  $S_{22_e}$  for the even mode and  $S_{22_o}$  for the odd mode.  $S_{22_e}$  and  $S_{22_o}$  were calculated on the basis of the equivalent admittances looking toward the circuit from port 2. Equation (23) summarizes the relationship between  $S_{22}$  and the other parameters.

$$S_{22} = S_{22_e} + S_{22_o} = \frac{z_{IN3_e} + z_{IN4_e} - 1}{z_{IN3_e} + z_{IN4_e} + 1} + \frac{z_{IN3_o} + z_{IN4_o} - 1}{z_{IN3_o} + z_{IN4_o} + 1}, \quad (23)$$

$z_{IN3_e}$ ,  $z_{IN4_e}$ ,  $z_{IN3_o}$ , and  $z_{IN4_o}$  are related to the isolation resistance ( $r$ ) and the six parameters of the TLines ( $z_i$ ,  $\theta_i$ ) by equations (2), (4), (13), and (14), respectively.

In practice, the algorithm described in Fig. 3 is used to find close solutions, only based on the port 2 matching condition. This algorithm is implemented on Matlab with the help of the RF toolbox.

First,  $r$  must be fixed to the desired value and  $z_1$ ,  $z_2$ , and  $z_3$  to the minimum achievable characteristic impedance given by the technology. Included in the three overlapping loops of  $z_1$ ,  $z_2$ , and  $z_3$  (symbolized with only one block in the algorithm), the three electrical lengths  $\theta_3$ ,  $\theta_1$ , and  $\theta_2$  are calculated in this order, according to equations (18), (20), and (22). Then  $S_{22}$  is compared with the initial condition. Typically, it is a good choice to start the procedure with  $S_{22\_max} = -35$  dB. If after any combinations of  $z_1$ ,  $z_2$ , and  $z_3$ ,  $S_{22}$  stays higher than  $S_{22\_max}$ , this means that the goal is not achievable. Consequently,  $S_{22\_max}$  should be slightly increased. The softer the conditions concerning  $S_{22\_max}$  is, the worse the isolation and matching of the PD are. In practice, the choice of  $S_{22\_max}$  is deserved to the designer, depending on the specifications related to the application.

Finally, additional conditions concerning  $\theta_i$  and/or  $z_i$  ranges, may have consequences on the device maximum size and on the quality factor of the TLines (in particular if integrated technologies are targeted). The designer thus can choose a compromise between the PD electrical performance

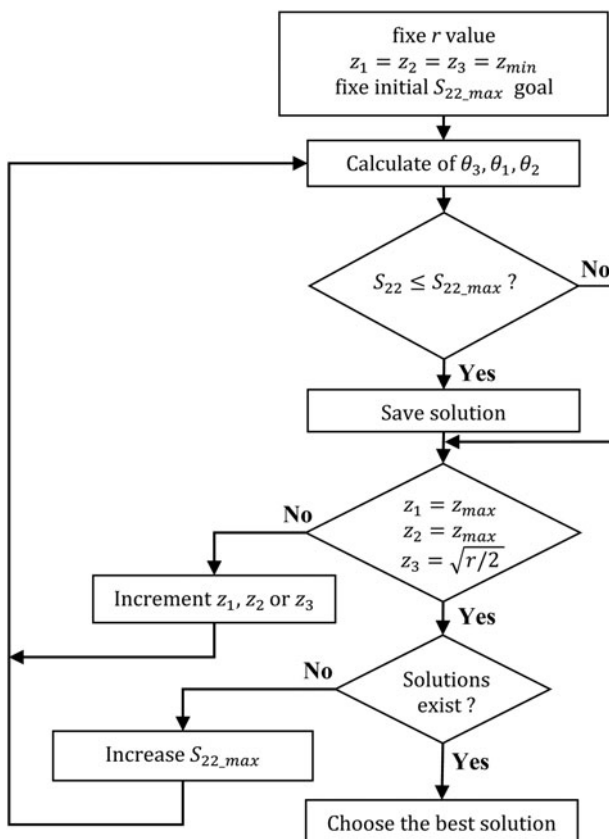


Fig. 3. Algorithm to find solutions.

and its size by electing the appropriate values of the characteristic impedances and electrical lengths, as in [11].

#### IV. CIRCUITS DESIGN AND EXPERIMENTAL RESULTS

As shown in (21),  $r$  should be strictly bigger than the normalized value 2, i.e.  $R > 100 \Omega$  when considering a  $50\text{-}\Omega$  system characteristic impedance. In this paper, two PDs with two different values of  $R$  were fabricated to illustrate and validate the method described in Section III, one with  $R = 105 \Omega$  and one with  $R = 150 \Omega$ , respectively. Upper case letters used to describe the experimental characteristic impedances or resistances are related to the lower case ones of the theory by means of the system impedance  $Z_0 = 50 \Omega$ .

##### A) PD with $R = 105 \Omega$

The condition for  $S_{22}$  was fixed to  $-35$  dB. The characteristic impedances range of variation was fixed to  $(25 \Omega; 100 \Omega)$ , except for  $Z_3$  which is limited to  $51 \Omega$  from (21). A step of  $2 \Omega$  is a good compromise between time simulation and impedance resolution for the outline of the design graphs. . Once all the possible sets of impedances,  $Z_1$ ,  $Z_2$ , and  $Z_3$  in their respected range, have been explored, the process ends with various solution sets that fit the condition on  $S_{22}$ . Figure 4 is an easy way of representation of the solutions. It also enables to plot the various electrical lengths corresponding to the solutions sets. As  $\theta_3$  only depends on  $Z_3$ , it has been plotted alone in Fig. 4(a). This map shows that the higher  $Z_3$  is, the longer  $\theta_3$  is. It also shows that any value of  $Z_3$  within its variation range is part of a solution set. Fig. 4(b) focuses on  $Z_1$  and  $\theta_1$ . For each possible value of  $Z_3$ , two, three, or four  $Z_1$  may be part of a solution set. As  $\theta_1$  only depends on  $Z_3$  and  $Z_1$ , it can be thus calculated and represented in color scale on the same graph. It is interesting to point out that the higher  $Z_1$  is and the shorter  $\theta_1$  is. Finally, Fig 4(c) focuses on stub ( $Z_2$ ,  $\theta_2$ ). It can be seen that for any couple  $(Z_1, Z_3)$  that is part of a solution set, all the values of  $Z_2$  in the range  $[25 \Omega; 100 \Omega]$  may fit the criterion  $S_{22} < S_{22\_max}$ . It is noticeable that shorter stub length,  $\theta_2$ , is required when  $Z_2$  lowers.

Hence, there exists a large number of solutions sets that fit the criterion on  $S_{22}$ . Depending on the objective — strongly miniaturized PD or the specific shape for antennas array — the designer may choose one set or another. Our solution thus leads to high flexibility in the design, which is its major interest while maintaining good electrical performances.

In the present example, a strong miniaturization is required. It could be reached with the choice of  $Z_3 = 25 \Omega$  and  $\theta_3 = 14.4^\circ$ . With such solution, several values for  $Z_1$  and  $\theta_1$  are then available.  $Z_1 = 81 \Omega$  appears to be a good compromise to avoid too high characteristic impedances, which leads to  $\theta_1 = 57.7^\circ$ . Lastly, Fig. 4(c) gives the electrical length  $\theta_2$  versus  $Z_1$  and  $Z_2$ , for various achievable values of  $Z_3$ . Many possibilities exist for the pair  $(Z_2, \theta_2)$ . Based on  $Z_3 = 25 \Omega$  and  $Z_1 = 81 \Omega$ , a wide range remains possible. Design constraints can be taken into account for the choice of the pair  $(Z_2, \theta_2)$ . In particular,  $\theta_2$  should be chosen short enough to avoid parasitic coupling between the TLines  $(Z_1, \theta_1)$  and  $(Z_2, \theta_2)$ .  $Z_2 = 39 \Omega$ , leading to  $\theta_2 = 35.2^\circ$ , were chosen in the present design.

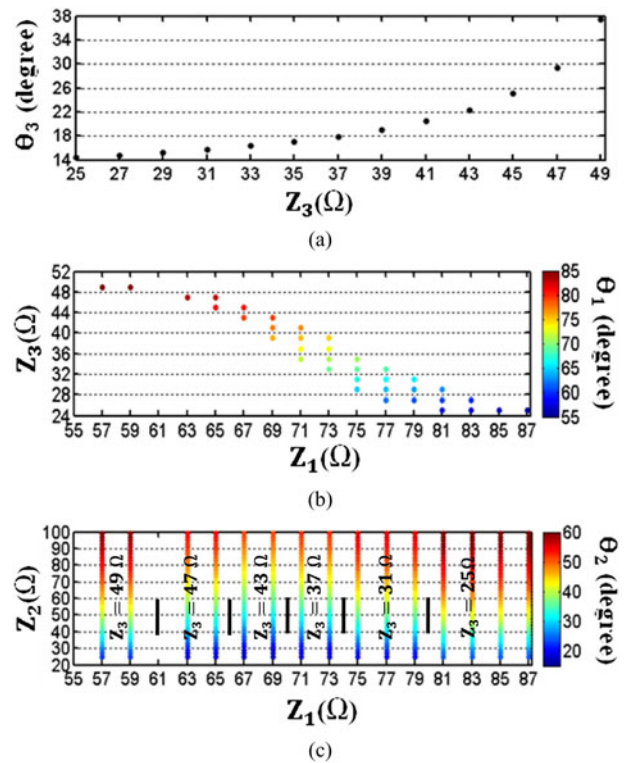


Fig. 4. Design graphs for  $R = 105 \Omega$ .

The circuits were fabricated on the dielectric substrate Rogers RO4003C<sup>TM</sup>, of relative dielectric constant 3.38 and thickness  $813 \mu\text{m}$ . All circuits are working at the frequency of  $2.45$  GHz. A SOLT calibration was carried out on an 8720 Vector Network Analyzer. The resistance  $R$  was measured equal to  $100.2 \Omega$ , 5% lower than the expected value of  $105 \Omega$ . Figure. 5 compares the  $S$ -parameters obtained from electromagnetic (EM) simulations on ADS-Momentum (with  $R = 105 \Omega$ , as in the design procedure) and measurements (with  $R = 100.2 \Omega$ , respectively). Despite the lower value of  $R$ , a very good agreement is obtained.

As expected the PD is very low loss with  $0.13$  dB of insertion loss only at  $2.45$  GHz, partially due to SMA RF connectors. The available bandwidth, defined by  $S_{11}$  below  $-15$  dB, reaches 34%, from  $2$  to  $2.84$  GHz. Considering this bandwidth, the output port return loss  $S_{22}$  and the isolation  $S_{23}$  are better than  $-17$  and  $-18$  dB, respectively. They reach  $-26$  and  $-34$  dB at  $2.45$  GHz, respectively. Remember that  $S_{22}$  was fixed to  $-35$  dB as an input condition of the design algorithm. Even if  $-35$  dB is reached in the design process on Matlab, calculi are based on theoretical equations only and do not take into account junctions' electrical models nor parasitic couplings that in practice contribute to degrade the return loss. Moreover, the value of  $R$  was 5% below the targeted value, which also explains the discrepancy between  $-35$  and  $-26$  dB at  $2.45$  GHz. It is worth emphasizing that  $-26$  dB as a measured return loss provides excellent matching conditions for a large majority of applications.

Figure 6 is a viewgraph of the fabricated PD compared with the modified PD early proposed in [3] and re-designed by the authors for valuable comparison. To design the latter, the value of  $R$  was fixed to  $95 \Omega$  to get an electrical length of the TLines equal to  $12.6^\circ$  between the output ports and

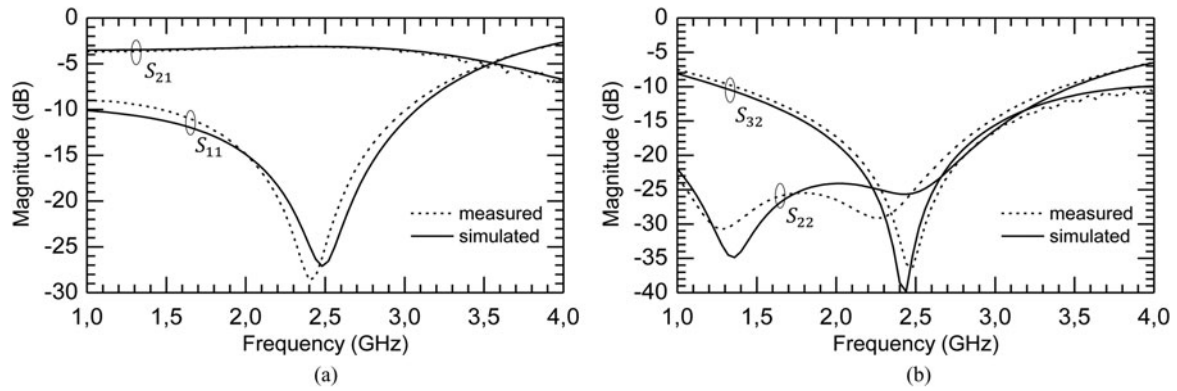


Fig. 5. Simulation and measurement results of the proposed topology with  $R = 105 \Omega$  in EM simulations,  $R = 100.2 \Omega$  for measurements, 5% smaller than expected.  $(Z_1, \theta_1) = (81 \Omega, 57.7^\circ)$ ,  $(Z_2, \theta_2) = (39 \Omega, 35.2^\circ)$ ,  $(Z_3, \theta_3) = (25 \Omega, 14.4^\circ)$ . (a) Insertion loss and input return loss. (b) Isolation and output return loss.

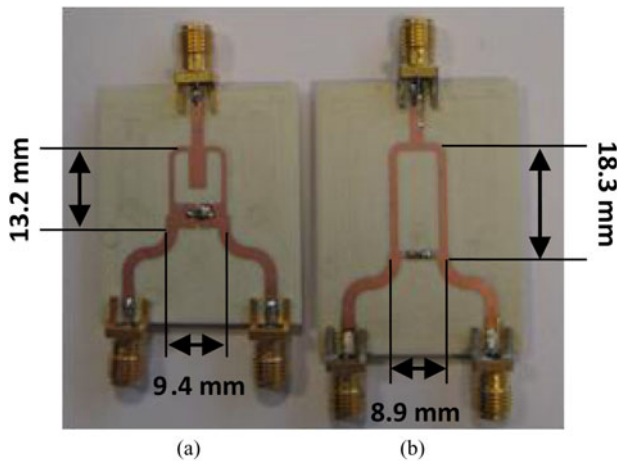


Fig. 6. Measured circuits. (a) Proposed design. (b) Modified PD from [3].

the resistance, which is close to the  $14.4^\circ$  chosen for the topology presented here. The TLines characteristic impedance

was fixed to  $69 \Omega$ , with an electrical length between ports 1 and 2 (or 3) equal to  $102.6^\circ$ . These values lead to a surface of the herein proposed circuit that is 24% smaller compared with that proposed in [3]. Scattering parameters are summarized in Table 2.

To conclude, these results suggest that the proposed PD is low loss, with really good matching and isolation. It is smaller and more flexible than the one proposed in [3] while keeping similar advantages such as the limitation of the parasitic coupling between the output ports thanks to the TLines connecting the resistance. In terms of simplicity, miniaturization, and performance, this design is also clearly well suited to further circuit integration considerations.

### B) PD with $R = 150 \Omega$ for antenna array feeding circuits

Another PD was achieved and measured with  $R$  fixed to  $150 \Omega$ . As for the previous one the maximum value of  $S_{22}$

Table 2. Pros and cons comparison with previous works.

Work	Specifications	Size (mm <sup>2</sup> ) ( $\lambda_g^2$ )	Freq. (GHz)	Bandwidth ( $S_{11} < -15$ dB) (%)	Within bandwidth		At center freq. IL (dB)
					$S_{22}$ (dB)	$S_{23}$ (dB)	
[3] (adapted by the authors at 2.45 GHz) $R=95 \Omega$	<ul style="list-style-type: none"> <li>Feeding lines in the isolation branch</li> <li>Compatible with CMOS process</li> <li>Not miniaturized</li> <li>Simplicity</li> <li>Not flexible</li> </ul>	$18.3 \times 8.9$ $0.25 \times 0.12$	2.45	60	-18	-14.5	-0.16
[5] $R = 66.5 \Omega$ $C_{series} = 2.7$ Pf (MCCT only Gysel type more cumbersome)	<ul style="list-style-type: none"> <li>Impedance transformer</li> <li>Capacitance in the isolation branch</li> <li>Stub at port 1</li> <li>Strong miniaturization</li> <li>Not compatible with CMOS process</li> <li>Complexity</li> </ul>	$16.7 \times 10.8$ $0.08 \times 0.05$	1	80	-9	-8	-0.08
Authors $R = 105 \Omega$ Miniaturization	<ul style="list-style-type: none"> <li>Feeding lines in the isolation branch</li> <li>Stub at port 1</li> <li>Compatible with CMOS process</li> </ul>	$13.2 \times 9.4$ $0.18 \times 0.13$	2.45	34	-17	-18	-0.13
Authors $R = 150 \Omega$ Shaping	<ul style="list-style-type: none"> <li>Miniaturization</li> <li>Simplicity</li> <li>Flexible design</li> </ul>	$7.0 \times 41.2$ $0.10 \times 0.56$	2.45	4.5	-17	-21	-0.23

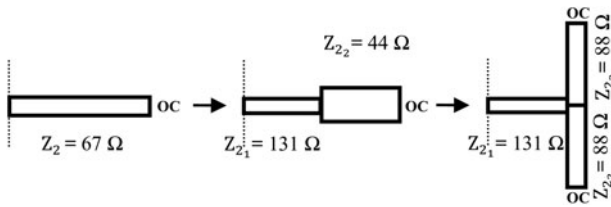


Fig. 7. Steps to design the open stub ( $Z_2, \theta_2$ ) to fit the free space in the PD (not to scale).

was fixed to  $-35$  dB for the initial design, the characteristic impedances still varied between 25 and 100  $\Omega$ , and  $Z_3$  was limited to 61  $\Omega$ . Following a design graphs procedure as the one proposed in Fig. 4, it is shown that the solution  $\theta_3 = 49^\circ, Z_3 = 49 \Omega, \theta_1 = 60^\circ$ , and  $Z_1 = 65 \Omega$  enables high flexibility in terms of PD shape with a relatively long TLine connecting the output ports to the resistance. In the counterpart, particular attention was paid on the electrical length  $\theta_1$  that should be longer than  $\theta_3$  to avoid meandering of the TLine ( $Z_3, \theta_3$ ). The open-circuit stub ( $Z_2, \theta_2$ ) was designed in a T shape to fit the free space in the PD loop. To get more flexibility and reduce the length of the stub, the TLine ( $Z_2 = 67 \Omega$  and  $\theta_2 = 66^\circ$ ) was realized by a stepped-impedance structure, as shown in Fig. 7, with  $Z_{21} = 131 \Omega, \theta_{21} = 6.2^\circ, Z_{22} = 44 \Omega$ , and  $\theta_{22} = 41^\circ$ , respectively.  $Z_{21}$  can be considered as a high characteristic impedance, but such a value is still achievable in a classical PCB technology. Its shortness should not bring too much loss. Finally, the TLine with the lower characteristic impedance was divided in two parallel TLines of similar electrical length but with characteristic impedance multiplied by 2, so that  $Z_{2,2}$  becomes now equal to 88  $\Omega$ .

Figure 8 compares the S-parameters obtained from EM simulations on ADS-Momentum and measurements. Here again, the agreement between simulation and measurement results is very good. The insertion loss is 0.23 dB at 2.45 GHz and the bandwidth reaches 4.5%, from 2.37 to 2.48 GHz (Fig. 8(a)). The return loss at the output port  $S_{22}$  is better than  $-17$  dB and the isolation  $S_{3,2}$  is better than  $-21$  dB in the defined bandwidth. They reach  $-19$  and  $-29$  dB at 2.45 GHz, respectively (Fig. 8(b)). This PD is only slightly smaller (6%) than the one presented in [3]. But its topology proves a huge shape flexibility which can, by the end, save much space in a global system. Here, the cost of such flexibility is a reduced bandwidth.

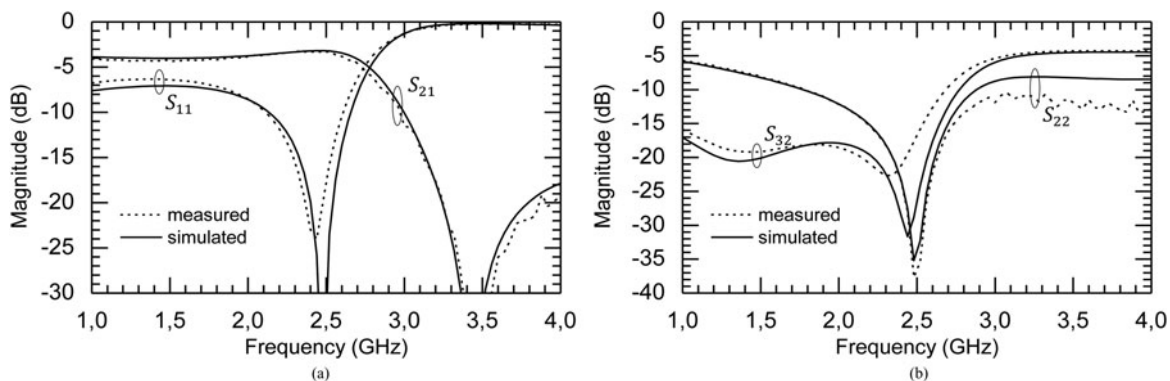


Fig. 8. Simulation and measurement results of the proposed topology with  $R = 150 \Omega$ . ( $Z_1, \theta_1$ ) = ( $65 \Omega, 60^\circ$ ), ( $Z_{21}, \theta_{21}$ ) = ( $131 \Omega, 6.2^\circ$ ), ( $Z_{22}, \theta_{22}$ ) = ( $88 \Omega, 41^\circ$ ), ( $Z_3, \theta_3$ ) = ( $49 \Omega, 49^\circ$ ). (a) Insertion loss and input return loss. (b) Isolation and output return loss.

A utilization of the fabricated PD is illustrated in the next section where a 4-antennas feeding circuit was realized as a proof of concept.

### C) Antennas array feeding circuit

The PD of Section IV.B was used in a 1:4 feeding circuit of an antennas array. Figure 9 shows the fabricated feeding circuit. Two PDs were connected in parallel at the outputs of a first one by means of TLines, called ( $Z_4, \theta_4$ ), in such a way that each output stays equidistant from its neighbors (see Fig. 9).  $Z_4$  and  $\theta_4$  were fixed after a tuning procedure. The choice of characteristic impedance  $Z_4$  different from 50  $\Omega$  offers the opportunity to slightly increase the feeding circuit bandwidth as compared with a single power divider.  $Z_4$  and  $\theta_4$  were taken equal to 45  $\Omega$  and  $165^\circ$ , respectively.

Figure 10 shows the comparison between the simulation and measurement results. The agreement is very good. The insertion loss is 0.48 dB below the ideal value of 6 dB at 2.45 GHz. The bandwidth, defined by  $S_{11}$  below  $-15$  dB, reaches 15% (Fig. 10(a)). In the considered bandwidth, the return loss at the output port  $S_{22}$  is better than  $-15$  dB. The isolation  $S_{2,3}$ , which is the one between two outputs of the same PD (i.e. between output ports 2 and 3, or 4 and 5, respectively) is better than  $-15$  dB, while the isolation  $S_{2,4}$  which is the one between two outputs from different PDs is better than  $-23$  dB (Fig. 10(b)). At 2.45 GHz,  $S_{11}, S_{22}, S_{2,3}$ , and  $S_{2,4}$  are equal to  $-17, -18, -21,$  and  $-35$  dB, respectively. It would be very easy to improve the network return loss thanks to the tuning of the TLines ( $Z_4, \theta_4$ ). This would lead, in counterpart, to the reduction of the bandwidth.

Thanks to the particular shape of the proposed circuit, it is possible to save more surface area compared with what could be obtained with more conventional Wilkinson-type PDs.

### V. COMPARISON WITH PREVIOUS WORKS

As aforementioned, compared with [3], the PD with 105  $\Omega$  enables to save space (24%), while maintaining similar or better electrical performances. Bandwidth is lower but the 60% bandwidth in [3] is unnecessary in most cases, for RX systems are already limited by the power amplifiers bandwidth. The PD realized in this paper is also compatible with

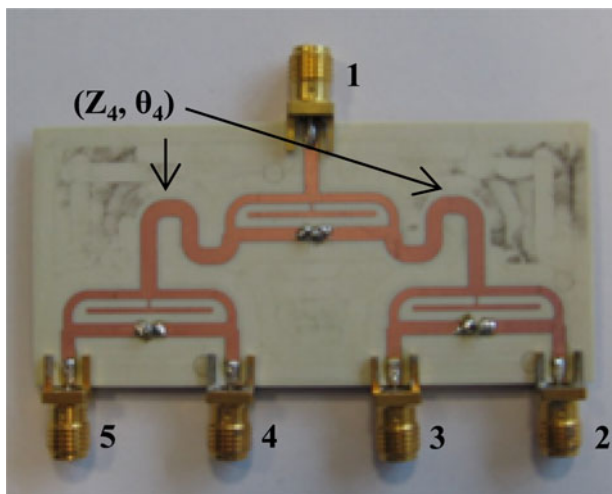


Fig. 9. 1:4 feeding circuit.

a CMOS process. The PD with  $150 \Omega$  claims the same advantages with a bigger surface. It has been shaped to save space once assembled in a 1:4 feeding circuit for antenna arrays. It is a very low bandwidth but it was demonstrated that bandwidth could be extended up to 15% when inserted in a 1:4 antenna array feeding network. Compared with [5], the proposed solution with  $105 \Omega$  is less miniaturized. However, [5] would need big changes in terms of re-design for CMOS compatibility. By imagining that feeding lines are considered in the isolation branch and that the overall re-design stays as much miniaturized in terms of  $\lambda_g^2$ , the connection to a Metal–Insulator–Metal capacitance will be necessary. The added surface due to the capacitance would finally lead to less miniaturization. In [5], matching at port 2 and isolation between ports 2 and 3 are poor as compared with the proposed PD. This is due to the trade-off between an extremely large bandwidth and the return loss.

## VI. CONCLUSION

This paper was focused on the design and fabrication of PDs working at RF frequencies and was carried out in a classical PCB technology. The design consists in a modified Wilkinson power divider. It takes into account the output isolation resistance feeding TLines used to avoid coupling

between the output ports. It also associates an open stub at the input port junction. While keeping very good isolation between output ports and matching on all ports, the proposed PD enables an optimal choice of the characteristic impedance of the transmission lines, flexibility in the output ports position, and size reduction. The PD is really easy to design, with no reactive lumped element. Depending on the considered technology, the best compromise may be chosen between size and electrical performance. Design rules were given thanks to design graphs, and a simple method consisting in searching sets of solutions was described. The design method is valid at center frequency; further circuit analysis is then required to explore the entire targeted frequency band.

Two PDs were realized for a proof-of-concept, with different characteristics, to show the potentiality for miniaturization or flexibility in the choice of the output ports position. Measurement and simulation results were in very good agreement. Then, a 1:4 antenna array feeding network was achieved. Thanks to the PD flexibility, the surface area of this feeding network was minimized. Here again, measurement and simulation results were in very good agreement.

This study confirms that the new proposed topology is well suited for CMOS millimeter-wave technologies. First, the considered characteristic impedances are achievable in a CMOS process, together with the isolation resistances values. Then, in order to fit the topology of the device placed just after PD, spacing between ports 2 and 3 can be specified as an initial condition. Using the proposed design process, a miniaturized solution may be found, which is of major importance in CMOS for cost reasons. Finally, the design can be very simple, with straight horizontal, vertical, or  $45^\circ$  only connection lines which is mandatory in CMOS design rules.

## ACKNOWLEDGEMENTS

The research leading to these results has been conducted in the frame of the European ENIAC MIRANDELA project and it received funding from the ENIAC Joint Undertaking under grant agreement number 120221 together with funding from the French Direction Générale de la Compétitivité, de l'Industrie et des Services under convention N°102930164.

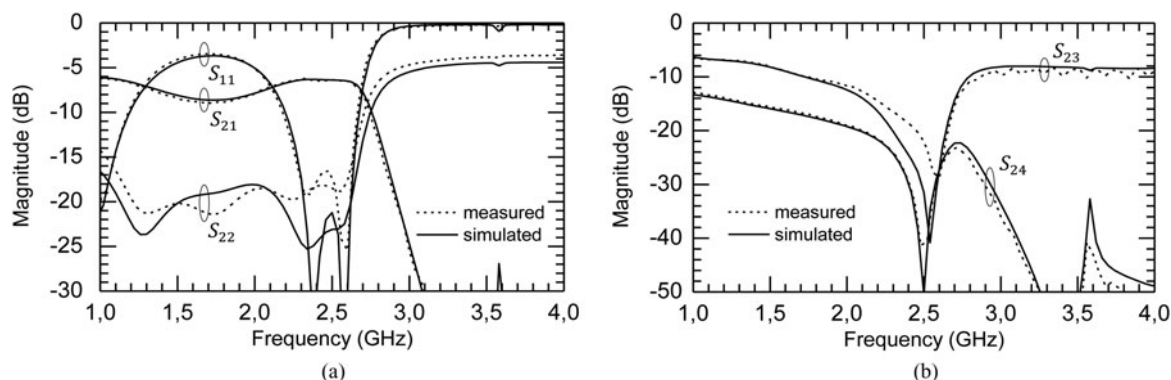


Fig. 10. Simulation and measurement results of the 1:4 feeding circuit. (a) Magnitude of  $S_{21}$ ,  $S_{11}$ , and  $S_{22}$ . (b) Magnitude of  $S_{23}$  and  $S_{24}$ .



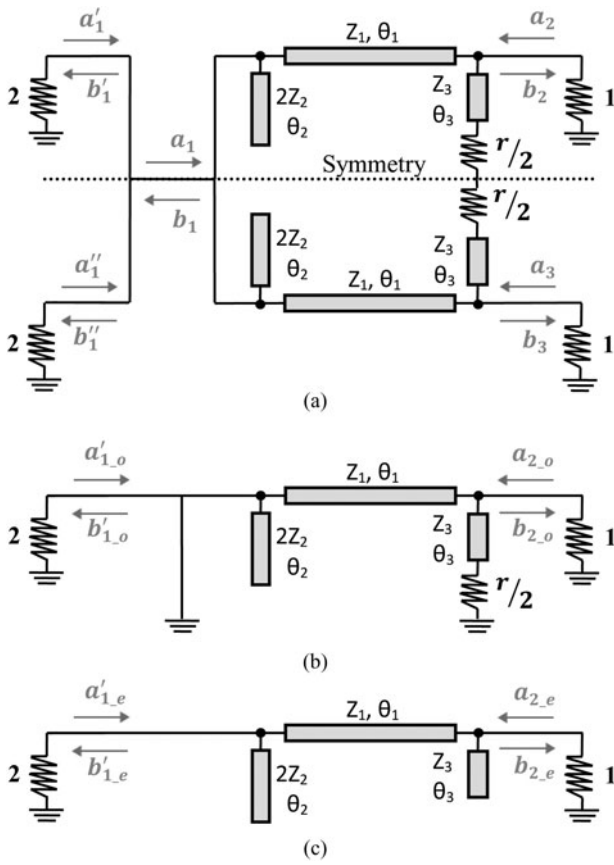


Fig. 11. (a) Normalized representation of Fig. 1(c) as a four ports network, (b) odd-mode, and (c) even-mode schematics.

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APPENDIX

This appendix aims at demonstrating that a matching condition on the scattering parameter  $S_{22}$  of a PD is enough to ensure good isolation and input matching. Statement is valuable for any three-port network as long as (i) the symmetry condition between ports 2 and 3 is verified (balanced network) and (ii) there is no loss in the equivalent even-mode circuit (which means no resistive element in the even-mode circuit). Those conditions are fulfilled by the PD represented in Fig. 1(c). Due to condition (i) the later can be redrawn as the four ports network in Fig 11(a).

Based on those considerations, the network can be analyzed by an even/odd-mode approach. Naming  $a_1$ , the input power wave at port 1, the following equations hold for the relationships between the power waves defined in Fig. 11:

$$\begin{aligned} a'_1 &= a'_{1-e} + a'_{1-o}, & b'_1 &= b'_{1-e} + b'_{1-o}, \\ a''_1 &= a'_{1-e} + a'_{1-o}, & b'_1 &= b'_{1-e} - b'_{1-o}, \\ a_1 &= a_{1-e} + a_{1-o}, & b_1 &= b_{1-e} + b_{1-o}. \end{aligned} \tag{A.1}$$

In the same manner, if an input power wave  $a_2$  is considered at port 2, or  $a_3$  at port 3, the following equations occur:

$$\begin{aligned} a_2 &= a_{2-e} + a_{2-o}, & b_2 &= b_{2-e} + b_{2-o}, \\ a_3 &= a_{2-e} - a_{2-o}, & b_3 &= b_{2-e} - b_{2-o}. \end{aligned} \tag{A.2}$$

A. ODD-MODE ANALYSIS

As port 1 is shunted (Fig. 11,b), no transmission may occur between ports 1 and 2. Consequently, the general form of the odd-mode reciprocal scattering matrix  $[S_o]$  is written as:

$$\begin{bmatrix} S_{11-o} & 0 \\ 0 & S_{22-o} \end{bmatrix}. \tag{A.3}$$

From Fig. 11(b), we get  $a'_{1-o} = -b'_{1-o}$ , which can be stated as  $|S_{11-o}| = 1$ . With the presence of a resistance in the network, the matrix cannot be unitary. Necessarily  $|S_{11-o}| \neq |S_{22-o}|$  and  $|S_{22-o}| \neq 1$ .

Moreover, as  $a_{1-o} = a'_{1-o} - a'_{1-o}$ , and  $b_{1-o} = b'_{1-o} - b'_{1-o}$ , power waves  $a_{1-o}$  and  $b_{1-o}$  may be expressed in the odd mode as:

$$a_{1-o} = 0, \quad b_{1-o} = 0. \tag{A.4}$$

## B. EVEN-MODE ANALYSIS

The even-mode scattering reciprocal matrix  $[S_e]$  takes the form below:

$$\begin{bmatrix} S_{11-e} & S_{12-e} \\ S_{12-e} & S_{22-e} \end{bmatrix}. \tag{A.5}$$

The even-mode network being lossless, the even matrix is unitary and the two following equations held:

$$S_{11-e}^2 + S_{12-e}^2 = 1 \quad \text{and} \quad |S_{22-e}| = |S_{11-e}|. \tag{A.6}$$

Moreover, in Fig. 11(a), at port 1, half power comes from the upper port 1' and half from the lower port 1'', so that power waves  $a_{1-e}$  and  $b_{1-e}$  may be expressed as:

$$a_{1-e} = \sqrt{2} \cdot a'_{1-e}, \quad b_{1-e} = \sqrt{2} \cdot b'_{1-e}. \tag{A.7}$$

## C. DISCUSSION ON THE SCATTERING PARAMETERS

Equations (24), (25), (27), and (30) give a relationship between even, odd, and global power waves. It is thus possible to link one to each other the parameters of the three-port matrix  $[S]$  with the parameters of the two-port matrices  $[S_o]$  and  $[S_e]$ :

$$\begin{aligned} S_{11} &= S_{11-e}, \\ S_{12} &= \frac{S_{12-e}}{\sqrt{2}} = S_{13} = S_{21} = S_{31}, \\ S_{22} &= S_{22-e} + S_{22-o} = S_{33}, \\ S_{23} &= S_{22-e} - S_{22-o} = S_{32}. \end{aligned} \tag{A.8}$$

To design a three-port device, a parametric study is often necessary. A defined limit of the design process may consist in conditions on the scattering parameters. Various possibilities can be enforced.

### C.1 Condition $|S_{11}| = 0$

This condition leads to  $|S_{11-e}| = 0$ , implying  $|S_{12-e}| = 1$ , and hence  $S_{12} = 1/\sqrt{2}$ .

This is sufficient as long as output ports matching is not required. However, such a condition is not enough for the use of a PD as a combiner where isolation is required.

### C.2 Condition $|S_{22}| = 0$

Two solutions exist. The first one consists in equating  $S_{22-e}$  to  $-S_{22-o}$  which is undoubtedly meaningless. The second one is equivalent to having at the same time matching for both even- and odd-modes at port 2:

$$S_{22-o} = S_{22-e} = 0. \tag{A.9}$$

Consequently:

- Matching on port 1 is realized:

Considering (29),  $S_{22-e} = 0$  implies:

$$S_{11-e} = 0. \tag{A.10}$$

Considering (31),  $S_{11-e} = 0$  implies:

$$S_{11} = 0. \tag{A.11}$$

- - 3 dB ratio between ports 1 and 2 is reached:

Considering (29),  $S_{11-e} = 0$  implies:

$$S_{12-e} = 1. \tag{A.12}$$

Considering (31),  $S_{12-e} = 1$  implies:

$$S_{12} = 1/\sqrt{2}. \tag{A.13}$$

- Perfect isolation is realized:

Considering (31),  $S_{22-o} = S_{22-e} = 0$  implies:

$$S_{23} = 0. \tag{A.14}$$

## D. CONCLUSION

A matching condition on the scattering parameter  $S_{22}$  alone holds for the four conditions on  $S_{22}$ ,  $S_{11}$ ,  $S_{12}$ , and  $S_{23}$  as long as the PD stands symmetrical and lossless (except the isolation resistance  $R$ ).

In practice, having  $|S_{22}| = 0$  may be impossible. Assuming, as a criterion to meet, that  $|S_{22}| < S_{22-max}$ , or in other words, trying to have  $S_{22}$  close to 0, implies  $S_{22-e}$  close to 0 too, which is equivalent to  $S_{11} = S_{11-e} = S_{22-e}$  close to 0 as well. The maximum value that  $|S_{11}|$  will reach is not easy to express as a function of  $S_{22-max}$  as it will depend on both real and imaginary parts of  $S_{22}$  but the tendency is the same: being close to 0. The argumentation is similar for  $S_{23}$ .



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