Phase-change materials in electronics and photonics

Wei Zhang, Riccardo Mazzarello, and Evan Ma, Guest Editors

The rapidly growing demand for data storage and processing, driven by artificial intelligence (AI) and other data-intensive applications, is posing a serious challenge for current computing devices based on the von Neumann architecture. For every calculation, data sets need to be shuffled sequentially between the processor, and multiple memory and storage units through bandwidth-limited and energy-inefficient interconnects, typically causing 40% power wastage. Phase-change materials (PCMs) show great promise to break this bottleneck by enabling nonvolatile memory devices that can optimize the complex memory hierarchy, and neuro-inspired computing devices that can unify computing with storage in memory cells. The articles in this issue of *MRS Bulletin* highlight recent breakthroughs in the fundamental materials science, as well as electronic and photonic implementations of these novel devices based on PCMs.

Challenges in data storage and processing

The global size of data generated in 2016 was approximately 16 zettabytes (16×10^{21} bytes), and this number doubles every two years. Storing this massive data and extracting relevant information quickly and accurately at a sustainable energy cost has become a serious challenge. All current electronic devices employ the classical von Neumann architecture, which physically separates central processing units (CPUs) from memory units (**Figure 1**a). The memory units, spanning a complex hierarchy of speed and capacity, are composed of memory components, including fast but volatile static and dynamic random-access memory (SRAM and DRAM), and storage components, including nonvolatile but slow solid-state drives (SSDs) and hard disk drives (HDDs). For each computing operation, data shuffling between the CPU and multiple memory and storage units in a sequential manner constitutes a serious bottleneck for data transfer and processing. Improving these components separately is insufficient to substantially elevate the computing and power efficiencies.[1]
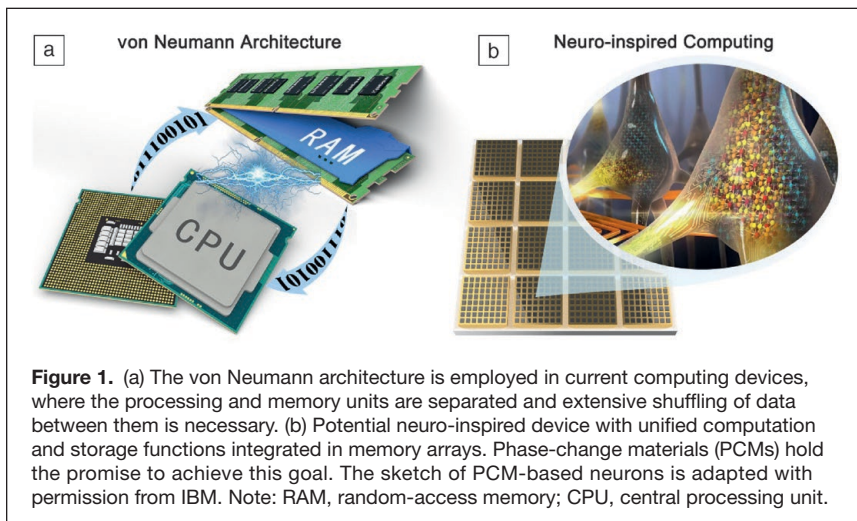
Besides conventional digital computing tasks, analog computing is also being pursued, which is more efficient for object recognition, natural language processing, decision making, and other artificial intelligence (AI)-related tasks.[2] The current achievements of AI applications are mainly driven by software programming,[3] such as the machine learning algorithms that mimic the functions and topologies of neural networks in human brains. Despite the success of AI algorithms, such as the AlphaGo program designed to play the board game Go,[4] they currently operate on conventional von Neumann digital-type computers, which consume a huge amount of electric power and spatial volume. All of these challenges are awaiting a fundamental change in computing hardware to increase the efficiency at reduced power consumption and chip dimensions.

Nonvolatile memory and neuro-inspired computing

In response to the increasing demand for data storage and processing power, nonvolatile memory[5–8] (NVM) and neuro-inspired computing[9–12] (NIC) electronic devices that are highly compatible with the current complementary metal oxide semiconductor (CMOS) technology are being developed. NVM combines the advantages of the fast operation speed of DRAM/SRAM and the persistent storage (retained when powered off) of SSDs/HDDs, holding the promise to optimize and even unify all memory and storage units in one memory chip. NIC shifts the focus of processing-centric computing toward memory-centric computing, breaking the von Neumann barrier by making calculations in memory arrays (Figure 1b). Depending on the degree of biological resemblance to the human brain, NIC implementations can be categorized into different levels.[11]

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Figure 1. (a) The von Neumann architecture is employed in current computing devices, where the processing and memory units are separated and extensive shuffling of data between them is necessary. (b) Potential neuro-inspired device with unified computation and storage functions integrated in memory arrays. Phase-change materials (PCMs) hold the promise to achieve this goal. The sketch of PCM-based neurons is adapted with permission from IBM. Note: RAM, random-access memory; CPU, central processing unit.

In addition to electronic NVM and NIC, photonic devices are also under active development. Although photonics is so far less technologically mature than electronics, optical systems can, in principle, offer a much higher bandwidth for data transfer.[13] Therefore, all-optical supercomputers equipped with photonic NVM and NIC components may be the future of computing devices.

Among the emerging material candidates for NVM[1] and NIC,[2] phase-change materials (PCMs) are the most mature for large-scale production.[14]

PCMs

PCMs[15–21] are a special group of semiconductors, mainly comprising chalcogenides or antimonides. The flagship PCM is $Ge_2Sb_2Te_5$[19,22] (GST) that is currently being used in PCM chips, such as the recently released 3D Xpoint products,[14] serving as storage-class memories to bridge the performance gap between DRAM and SSDs. Together with GST, GeTe,[23,24] $Ag_4In_3Sb_{67}Te_{26}$,[25,26] $Ge_{15}Sb_{85}$,[27,28] Sb,[29,30] and $Sc_{0.2}Sb_2Te_3$[31,32] have been extensively studied and applied for electronic memories and processors, rewriteable optical discs, as well as photonic memories, processors, and even displays.[13–48]
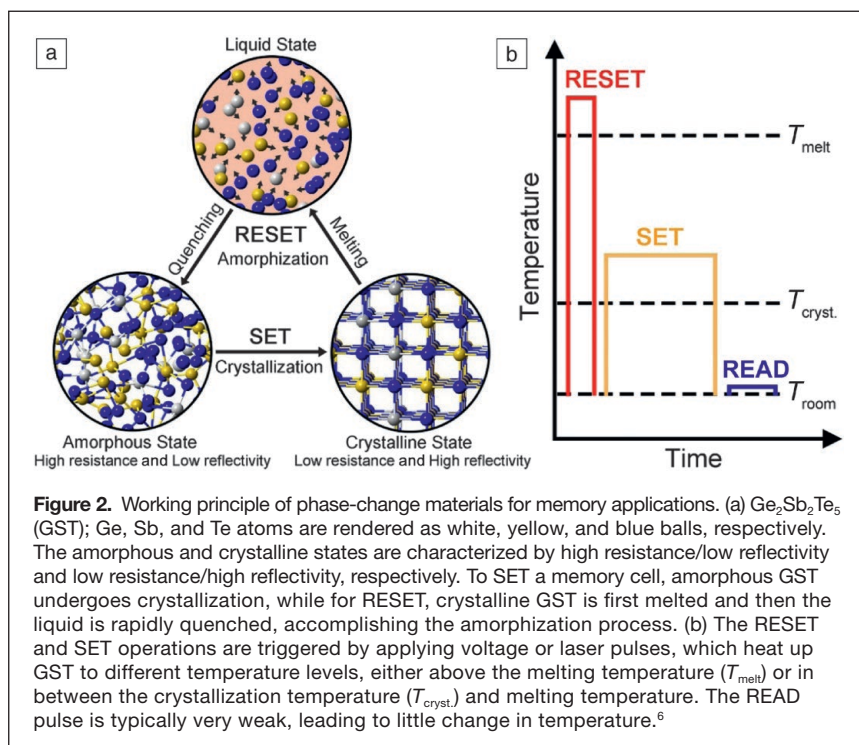
The basic working principle of a PCM using the example of GST is shown in **Figure 2**. The contrast in electrical resistance (~10^3) or optical reflectivity (~30%) between a disordered amorphous state and an ordered crystalline state of the PCM is utilized to identify the logic states "0" and "1" through a weak voltage or laser READ pulse.[6] To RESET or erase the memory cell, a high-level and narrow voltage or laser pulse is applied to the crystalline GST, which heats up the memory cell

above the melting temperature T_{melt} of GST (~900 K). A molten liquid state is reached and the subsequent rapid quenching of the liquid state results in an amorphous state. The RESET operation is typically rapid, finished over tens of picoseconds, but is power consuming and proper thermal insulation is compulsory to prevent heat loss.[15]
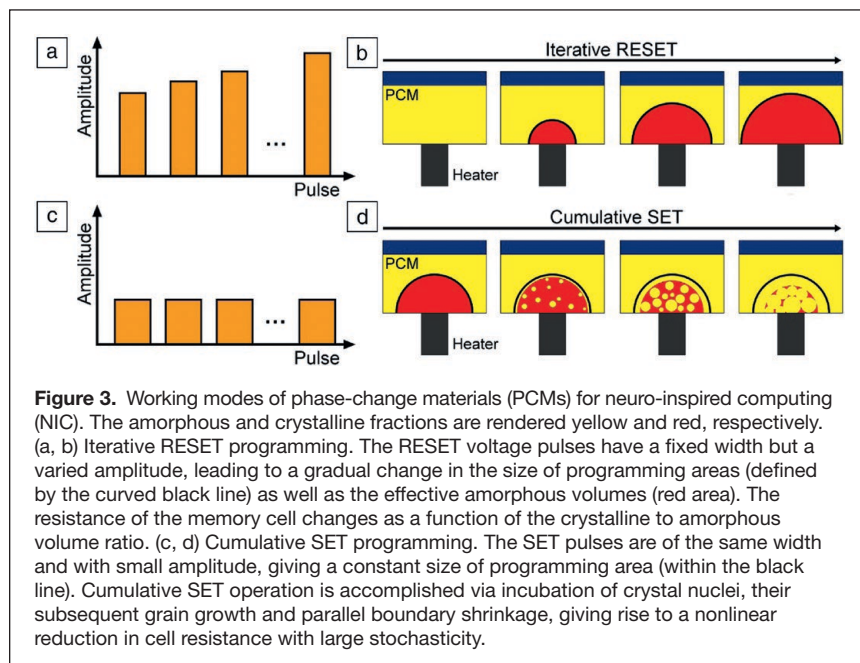
To SET or write the memory cell, a medium level and longer duration voltage or laser pulse is applied to amorphous GST, which raises the local temperature above the crystallization temperature, T_{cryst}, for fast crystallization (~500–600 K). For GST devices, the SET time is of the order of tens of nanoseconds,[15] with the stochastic nucleation process being the bottleneck. Nevertheless, this SET time limit can be drastically reduced to the subnanosecond regime either by applying a prepulse (where a 10-ns pulse of low voltage, such as 0.3 V, is applied for incubation of GST prior to the SET operation)[49] or by replacing GST with an alternative material such as the recently designed $Sc_{0.2}Sb_2Te_3$ compound with an intrinsically short incubation time for crystal nucleation.[31]

In addition to binary storage, multilevel storage has been demonstrated to be feasible using PCM-based electronic and photonic devices.[15,45] For example, in the electronic version, several partial RESET states can be obtained by adjusting the amplitude of the RESET voltage pulse (**Figure 3**a). A stronger pulse corresponds to a larger programming area and effective

Figure 2. Working principle of phase-change materials for memory applications. (a) $Ge_2Sb_2Te_5$ (GST); Ge, Sb, and Te atoms are rendered as white, yellow, and blue balls, respectively. The amorphous and crystalline states are characterized by high resistance/low reflectivity and low resistance/high reflectivity, respectively. To SET a memory cell, amorphous GST undergoes crystallization, while for RESET, crystalline GST is first melted and then the liquid is rapidly quenched, accomplishing the amorphization process. (b) The RESET and SET operations are triggered by applying voltage or laser pulses, which heat up GST to different temperature levels, either above the melting temperature (T_{melt}) or in between the crystallization temperature (T_{cryst}) and melting temperature. The READ pulse is typically very weak, leading to little change in temperature.[6]

Figure 3. Working modes of phase-change materials (PCMs) for neuro-inspired computing (NIC). The amorphous and crystalline fractions are rendered yellow and red, respectively. (a, b) Iterative RESET programming. The RESET voltage pulses have a fixed width but a varied amplitude, leading to a gradual change in the size of programming areas (defined by the curved black line) as well as the effective amorphous volumes (red area). The resistance of the memory cell changes as a function of the crystalline to amorphous volume ratio. (c, d) Cumulative SET programming. The SET pulses are of the same width and with small amplitude, giving a constant size of programming area (within the black line). Cumulative SET operation is accomplished via incubation of crystal nuclei, their subsequent grain growth and parallel boundary shrinkage, giving rise to a nonlinear reduction in cell resistance with large stochasticity.

amorphous volume (indicated by black lines and red areas, respectively, in Figure 3b). The cell resistance changes as a function of the crystalline to amorphous volume ratio. Such a programming scheme is termed as iterative RESET.[11] This scheme suffers from the spontaneous structural relaxation of amorphous PCMs at ambient temperatures,[50] causing resistance drift.[51] Iterative RESET serves as one of the two working modes for PCM-based neuro-inspired devices. The other one is termed as cumulative SET.[11] Instead of sending a strong SET pulse to fully crystallize the amorphous state, a train of weak SET pulses can be applied sequentially to the RESET amorphous state to obtain crystallization in a cumulative mode (Figure 3c). As shown in Figure 3d, the size of the programming area remains constant (within the black lines), while the effective amorphous volume changes in a random fashion (red areas) due to crystal nucleation, grain growth, and boundary shrinkage. Due to the stochasticity of crystallization, the cell resistance changes in a nonlinear way, and large fluctuations in cell resistance are found from pulse to pulse and cycle to cycle, causing variability issues.[52]

In this issue

The six articles in this issue of *MRS Bulletin* cover several important aspects of PCM fundamentals as well as electronic and photonic applications of PCMs. Recent breakthroughs in PCMs are summarized, and outlooks for future directions are presented.

The article by Wei et al.[53] presents an overview of the dynamics of liquid and supercooled-liquid PCMs. Liquid-to-liquid structural transitions, metal-to-semiconductor transitions, and other related phenomena are discussed in detail. Fragility of the liquid alloy, together with a new metallicity parameter proposed by the authors, are advocated as useful

indicators for screening of PCM candidates that are most suitable for applications.

Pries et al.[54] report recent progress on bonding mechanisms in PCMs, which is of fundamental importance for an understanding of the contrast in properties between the amorphous and crystalline states of PCMs. State-of-the-art atom probe tomography experiments for elucidating the bonding characteristics are thoroughly reviewed. Connections between metavalent bonding and kinetic properties of PCMs are also discussed.

The article by Sosso and Bernasconi[55] highlights the development of machine learning-based interatomic potentials for large-scale molecular dynamics simulations at an accuracy level comparable to *ab initio* simulations. They use machine learning potentials to model the structural, dynamical, and thermal properties of the amorphous and liquid phases of the prototypical GeTe compound. The authors also pinpoint future challenges in applying machine learning techniques for addressing critical issues of PCMs.

Kim et al.[56] focus on cycling endurance as a critical challenge that hinders further improvements in phase-change devices to rival DRAM. The current endurance limit is about 10^{12} write-erase cycles, which must be improved to 10^{15} or higher to meet the high-frequency memory requirements for data-intensive applications. The authors address various strategies for materials optimization, device engineering, and programming to break the cycle life bottleneck.

The Zhu et al.[57] article in this issue discusses the ovonic threshold switching (OTS) phenomenon in amorphous chalcogenides, a field-assisted transition that makes an amorphous semiconductor switch from a highly resistive to a conductive state when a threshold voltage is reached. In addition to reviewing the theoretical models developed to elucidate this phenomenon, this article outlines the critical challenges in OTS materials and device performance optimization. In particular, the integration of OTS selectors and PCMs is discussed as a key ingredient in making high-density PCM chips.

Finally, Wright et al.[58] summarize recent breakthroughs in PCM-based photonic devices and integrated systems. They show how PCMs can be integrated into standard silicon photonics circuits. By utilizing the unique optical characteristics of PCMs, they show how binary and multilevel NVM, arithmetic and logic processing, as well as synaptic and neuronal mimics for NIC can be achieved for a photonics platform.

Future outlook

We anticipate rapid progress over the next decade toward production of electronic and photonic memory and neuro-inspired chips. However, further materials optimization and device engineering are needed to resolve several critical issues such

as resistance drift, device variability, and power consumption. Progress in these areas is expected to benefit from the fundamental knowledge accumulated thus far, and in the future, at the atomic and electronic level for PCMs.
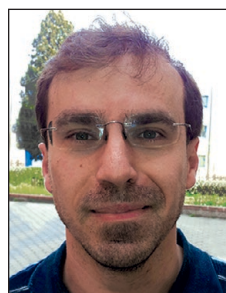
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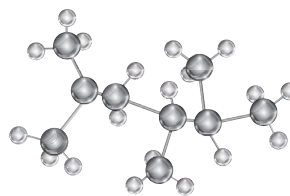58. D. Wright, H. Bhaskaran, W. Pernice, *MRS Bull.* **44** (9), 721 (2019). □

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