RESEARCH PAPER

A 1.2 V 15–32 GHz low-power single-balanced gate mixer with a miniature rat-race hybrid

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A 15–32 GHz miniature single-balanced gate mixer is proposed and analyzed. It achieves a smaller chip area with acceptable conversion gain and port-to-port isolation. In addition, the design procedure is described in detail. This mixer, fabricated in 90 nm digital CMOS technology, demonstrates a measured conversion loss of 1 dB and higher than 30 dB RF-to-LO port isolation from 17 to 32 GHz, at a local oscillator (LO) driver power of -4.3 dBm. The total dc power consumption is only 6 mW from a 1.2 V supply, including output buffer. The low dc power consumption and LO driver power reduce the power budget, and the proposed miniature rat-race hybrid facilitates integration in a receiver.

Keywords: Gate mixer, miniature, rat-race hybrid, single-balanced

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I. INTRODUCTION

Mixers play an important role in wireless communication systems. System requirements entail many considerations, such as conversion gain, noise figure (NF), port-to-port isolation, and linearity [1–3]. Moreover, both dc power consumption and local oscillator (LO) drive power should be low in a low-power millimeter-wave (MMW) communication system.

Although passive mixers have good linearity, the high LO drive power poses a challenge to integration in a CMOS MMW transceiver [4-7]. On the other hand, the resistive and drain mixers usually have large LO-RF feedthrough [8]. Among the active mixers, the Gilbert-cell mixer has rather high dc power and requires high voltage [9]. Unlike other active mixers, gate mixers have more efficient conversion gain at low LO drive power, low power consumption, and low supply voltage; however, the LO-RF feedthrough is also a severe impediment [8]. To enhance the RF port to LO port isolation, a rat-race hybrid, which provides in-phase and out-of-phase signals at the same time in a balanced mixer, is utilized in a balanced gate-pumped mixer. However, the conventional rat-race hybrid, especially the one that operates at lower frequencies, occupies a large chip area [9]. Although a miniature 60 GHz rat-race hybrid has

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been proposed in [10, 11], the rat-race hybrid is still large when it is applied in lower frequency applications, for example, below 30 GHz. The design procedure of the rat-race hybrid in [10, 11] is also complex. A combined hybrid is proposed in [12], but that double-balanced architecture still occupies a large area and has high dc power consumption. Moreover, the design considerations and procedures of a single-balanced gate-pumped mixer have not been described in detail in the literature.

In this paper, a miniature rat-race hybrid is proposed and analyzed. This rat-race hybrid occupies a smaller area than those in [10-12] at the same operation frequency. In addition, a rat-race single-balanced gate-pumped mixer is developed with very low LO power (-4.3 dBm). The design considerations and simplified design procedures of the single-balanced gate-pumped mixer with a rat-race hybrid are also described in detail.

II. CIRCUIT ARCHITECTURE

The presented rat-race single-balanced gate-pumped mixer is shown in Fig. 1. It is composed of a proposed miniature rat-race hybrid, gate-pumped mixers, and source followers.

The gate pumped mixers consist of transistors M_1 and M_2 , load resistors R_1 and R_2 , gate-biased resistors R_{G1} and R_{G2} , blocking capacitors C_{B1} and C_{B2} , and input-matching inductors L_{G1} and L_{G2} .

To drive low impedance loads $(R_{T_3} \text{ and } R_{T_4})$ the source follower output buffers for signal amplification and impedance transformation are used. Source followers, which comprise transistors M_3 and M_4 and load resistors R_3 and R_4 , provide suitable gain for the mixer.

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Fig. 1. A single-balanced gate-pumped mixer.

The schematic of the proposed miniature rat-race hybrid in Fig. 1 is shown in Fig. 2(a). The miniature rat-race hybrid can be implemented with a Marchand balun and thin-film microstrip (TFMS) lines to achieve the out-of-phase and in-phase signals at the output port [10, 11]. The Marchand balun can achieve a low loss with the ground plane shielding the high substrate loss. However, in this paper, the TFMS is replaced with a symmetric inductor L_s to achieve in-phase signals at the output port, as shown in Fig. 2. As can be observed, there is no ground plane under the symmetric inductor, so the routing length can be shorter than the TFMS line while still achieving the same inductance, thus reducing the size of the inductor, as well as its loss. Fig. 2(b) shows the layout of the proposed miniature rat-race hybrid, which is smaller than 150 μ m × 200 μ m.

III. CIRCUIT DESIGN

A) Device size and bias condition selection

The device f_T of nMOS reaches around 110 GHz in 90 nm CMOS [13]. Although 90 nm digital CMOS technology does provide a top thick metal layer, the 9-layer interconnecting metals can provide a high density fringe capacitor [14].

The V_{gs} is usually biased near the threshold voltage V_{TH} , 0.2 V, and the channel width is 250 μ m, respectively.

B) Rat-race hybrid

In order to achieve a higher LO-to-RF isolation in a mixer, the symmetry of the rat-race hybrid is important. For example, the output signals of port 3 and port 4 (Fig. 2) in the rat-race are

$$V_{P_3} = V_{\rm RF} \cos(\omega_{\rm RF} t + o^\circ) + V_{\rm LO} \cos(\omega_{\rm LO} t + o^\circ)$$

and

$$egin{aligned} V_{P_4} &= (V_{ ext{RF}} + \Delta V_{ ext{RF}})\cos(\omega_{ ext{RF}}t + ext{o}^\circ + heta) \ &+ (V_{ ext{LO}} + \Delta V_{ ext{LO}})\cos(\omega_{ ext{LO}}t + 180^\circ + \phi), \end{aligned}$$

where ΔV_{RF} , θ , and ϕ are the amplitude and phase offset of the RF path (in-phase), and LO path (out-of-phase),



Fig. 2. (a) Schematic and (b) layout of the proposed miniature rat-race hybrid.



Fig. 3. RF-to-LO isolations of the mixer versus phase offset.



Fig. 4. RF-to-LO isolations of the mixer when ΔV_{RF} and ΔV_{LO} are varied.

respectively. The effects of phase and amplitude mismatch for the RF-to-LO isolations in a gate mixer are shown in Figs 3 and 4. The simulation results are obtained by using 90 nm CMOS models provided by the foundry with an ideal 180° balun with variable phase and amplitude offsets. As can be observed, the in-phase signal is more sensitive than the out-of-phase signal. Fortunately, it is easy to lower the phase and amplitude mismatch to below 1° and 0.25 dB, respectively, by using a symmetric inductor, thus leading to an RF-to-LO isolation of a mixer higher than 40 dB.

In order to minimize chip area, we use the reduced-size Marchand balun. However, the design of the reduced-size Marchand balun is quite complex because of the multiple design parameters in a distributed structure [10, 11]. Fortunately, if we use a lumped-element model, these design parameters are closely related to only one key parameter, namely the total routing length (ℓ) , which greatly simplifies



Fig. 6. Amplitude mismatch and phase difference of the simulated lumped-element model for the Marchand balun ($\ell=310\,\mu m)$ from 20 to 30 GHz.

the design of the balun and is defined in this paper. In the preliminary design of the balun, the design procedures are described as follows:

- (1) Select a lumped-element model for TFMS lines, as shown in Fig. 5(a).
- (2) Determine the relationships between L_1 , C_2 , R_1 , and routing length (ℓ) through electromagnetic (EM) simulation based on a 3 μ m wide and 100 μ m long TFMS line, as shown in Fig. 5(b). The choice of the 3 μ m width is determined by the design rule and consideration of loss. In our case:

$$L_1(\text{pH}) = \ell(\mu m) \times 0.87 \times 10^{-6} (\text{H/m}),$$
 (1)

$$C_2(fF) = \ell(\mu m) \times 0.073 \times 10^{-9} (F/m),$$
 (2)

$$R_1(\Omega) = \ell(\mu m) \times 0.83 \times 10^4 (\Omega/m).$$
(3)

(3) Determine the relationships between C₁ and routing length (ℓ) through EM simulation based on a pair of edgecoupled lines with a width of 3 µm, spacing of 3 µm, and



Fig. 5. (a) Lumped-element model of TFMS lines, (b) a 3 μ m wide and $\ell \mu$ m long TFMS line, (c) a pair of edge-coupled lines with a width of 3 μ m, spacing of 3 μ m, and length of $\ell \mu$ m, (d) lumped-element model of the simulated Marchand balun, and (e) a pair of broadside-coupled lines with a width of 3 μ m, spacing of 0.715 μ m, and length of $\ell \mu$ m.





Fig. 7. Amplitude mismatch and phase difference of the EM-simulated Marchand balun from 20 to 30 GHz.

length of 100 μ m, as shown in Fig. 5(c). Again the spacing of 3 μ m is determined by the process design rule and reasonable coupling.

$$C_1(fF) = \ell(\mu m) \times 0.044 \times 10^{-9}(F/m)$$
 (4)

(4) Select the lumped-element model of the balun with the lumped-element model of TFMS lines, as shown in Fig. 5(d). Note that the output ports are port 3 and port 4, and the input port is port 1. Therefore, the amplitude mismatch is defined as the amplitude difference at port 3 and port 4, while port 1 is an input signal. On the other hand, the phase mismatch is defined as the phase difference at port 3 and port 4, while port 1 is an input signal.



Fig. 8. Die photo of the rat-race hybrid.



Fig. 9. EM-simulated and measured insertion loss of the rat-race hybrid.



Fig. 10. Die photo of the single-balanced gate-pumped mixer.

(5) Determine the relationships between C_M and routing length (ℓ) through EM simulation based on a pair of broadside-coupled lines with a signal line width of



Fig. 11. Conversion gain versus RF frequency (IF frequency = 0.1 GHz).



Fig. 12. RF-to-LO isolation of the gate mixer versus RF frequency.

3 μ m, spacing of 0.715 μ m, and length of 100 μ m, as shown in Fig. 5(e).

$$C_M(fF) = \ell(\mu m) \times 0.19 \times 10^{-9} (F/m).$$
 (5)

(6) Determine the total routing length based on the simulated frequency responses of phase and magnitude differences at the output ports. Referring to [10], the total routing length is around 300 μ m (ℓ) at 24 GHz. Figure 6 presents the simulated mismatch and phase difference of this balun from 20 to 30 GHz when the routing length is 310 μ m. It can be observed that this routing length (310 μ m) makes this balun operate at 24 GHz (amplitude mismatch = 1.5 dB; phase difference = 180°).

The selected parameters of this model, as shown in Table 1, are obtained through curve fitting via the Advanced Design System (ADS) and the Sonnet simulation tool. Due to the lumped-element model, the simulated frequency responses in Fig. 6 are not quite wideband. However, this simulated result still can provide insight for preliminary implementation of the physical layout of the reduced size Marchand balun. The routed length of the balun is preliminarily determined based on the value of L_{sp} in Table 1, and the final balun is determined through EM simulations for the precise size of



Fig. 13. RF return loss of the gate mixer.

the balun. In addition, the frequency responses of the EM simulations are wideband, unlike those of the lumped-element model of TFMS lines. In order to reduce the size, the width and space of the routing of this balun are 3 μ m. Furthermore, the outer radius and turn number of each spiral line are 55 μ m and 5, respectively. With these selections, the Marchand balun has phase and amplitude mismatches of less than 2° and 0.5 dB at 24 GHz, respectively (Fig. 7). With such properties, the RF-to-LO isolation of the mixer is better than 30 dB (Figs 3 and 4).

IV. EXPERIMENTAL RESULTS

A test circuit of the rat-race hybrid has also been fabricated, as shown in Fig. 8. The corresponding EM-simulated and measured insertion losses are shown in Fig. 9. As can be seen, the insertion loss from port 2 to port 3 (or port 4) is lower than 7.5 dB when the operation frequencies are higher than 15 GHz, and the simulation and measurement results agree well. In mixer application, the power level of the RF signal is very low; thus, port 2 is assigned to be the RF port

Tal	ble	2.	Performance	summary	and	comparisons.
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	Unit	This work	[4] (TMTT'08)	[8] (TMTT'05)	[9] (TMTT'08)	[15] (TMTT'07)	[16] (TMTT'06)
Technology	-	90 nm digital CMOS	0.31 µm RF CMOS	90 µm SOI CMOS	o.35 µm siGe Bi CMOS	0.18 μm RF CMOS	90 µm RF CMOS
Topology	-	Gate	Star	Gate-pumped passive	Gilbert micromixer	Distributed active	Sub-harmonic passive
Frequency	GHz	15-32	25-45	26.5-30	2.5-13	1-29	9-31
CG	dB	-1	-8 to -13	-10.3	12	12.5	-12 to -15
IF BW	GHz	0.1	-	2.5	-	0.01	2
P_{LO}	dBm	-4.3	6	0	0	3	3.3
IP _{1dB}	dBm	—7 (at 24 GHz)	-	-	-16	-	-
IIP ₃	dBm	6 (at 20 GHz)	-	12.7	-4	0	7 (at 10 14 GHz)
NF	dB	15	-	11.4	14	15	-
LO-RF	dB	>30 (17–40 GHz)	30-35	24	>30	>37.5	19
isolation							
DC power	mW	6	0	0	160	40	0
Chip size	mm ²	0.49 × 0.49	0.57×0.6	038×0.32	1.4×1.4	0.87×0.82	0.94×1.0

in this design to maintain the required conversion gain. Owing to the 0.85 μ m thickness of the top-metal in the digital process, the insertion loss is a little bit high, but we can slightly reduce the loss by reducing the length of the routing as much as possible. This proposed low-power miniature single-balanced gate mixer has been fabricated in 90 nm digital CMOS technology, as shown in Fig. 10.

The die photo of the mixer is shown in Fig. 10. The chip area is 0.49 mm \times 0.49 mm, including the testing pads. The core area is very small, occupying only $0.26 \text{ mm} \times 0.2 \text{ mm}$. It consumes 6 mW including buffers from a 1.2 V supply. Figure 11 shows the measured conversion gain of the mixer from RF frequencies of 10-40 GHz with a total supply current of 5 mA. The simulated conversion gain agrees reasonably with the measured one. The RF-to-LO isolation of the gate mixer is shown in Fig. 12. The isolation is better than 30 dB from 17 to 40 GHz. The measured RF return loss is shown in Fig. 13, and the return loss is very wideband as well. Table 2 presents a performance summary of the mixer alongside other reported mixers at similar operation frequencies. The developed mixer achieves a conversion gain of -1 dB with a very low LO power level of -4.3 dBm and a high LO-to-RF isolation of the gate mixer up to 30 dB at the same time. Due to the loss of the symmetric inductor, the NF is a little bit higher. But the proposed miniature rat-race hybrid is smaller than all those previously reported.

V. CONCLUSION

This paper presents a miniature rat-race hybrid for a gatepumped mixer that achieves lower conversion loss and higher port-to-port isolation. In addition, the design considerations and procedure are described in detail. The experimental results are presented to verify the proposed miniature hybrid rat-race and the design considerations and procedure for a gate-pumped mixer. From the experimental results, it is concluded that our proposed mixer can indeed achieve a low conversion loss and a high port-to-port isolation with a low LO power and lower dc power consumption at the same time. Finally, the demonstrated miniature singlebalanced gate-pumped mixer appears to be suitable for integration in a low-power receiver with a small size.

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REFERENCES

- Maas, S.A.: Microwave Mixers, 2nd ed., Artech House, Norwood, MA, 1993.
- [2] Razavi, B.: RF Microelectronics, Prentice Hall PTR, Upper Saddle River, NJ, 1998.

- [3] Lee, T.H.: The Design of CMOS Radio-Frequency Integrated Circuits, 2nd ed., Cambridge University Press, New York, 2004.
- [4] Kuo, C.C.; Kuo, C.L.; Kuo, C.J.; Maas, S.A.; Wang, H.: Novel miniature and broadband millimeter-wave monolithic star mixers. IEEE Trans. Microw. Theory Tech., 56 (4) (2008), 793–802.
- [5] Kuo, C.L.; Kuo, C.C.; Lien, C.H.; Tsai, J.H.; Wang, H.: A novel reduced-size rat-race broadside coupler and its application for CMOS distributed sub-harmonic mixer. IEEE Microw. Wirel. Compon. Lett., 18 (3) (2008), 194–196.
- [6] Yang, H.Y. et al.: Design and analysis of a 0.8–77.5 GHz ultrabroadband distributed drain mixer using 0.13 μm CMOS technology. IEEE Trans. Microw. Theory Tech., 57 (3) (2009), 562–572.
- [7] Chen, J.H.; Kuo, C.C.; Hsin, Y.M.; Wang, H.: A 15–50 GHz broadband resistive FET ring mixer using 0.18 μm CMOS technology, in IEEE MTT-S Int. Microwave Symp. Digest, Anaheim, May 2010, 784–787.
- [8] Ellinger, F.: 26.5–30 GHz resistive mixer in 90 nm VLSI SOI CMOS technology with high linearity for WLAN. IEEE Trans. Microw. Theory Tech., 53 (8) (2006), 2559–2565.
- [9] Tseng, S.C.; Meng, C.; Chang, C.H.; Chang, S.H.; Huang, G.W.: A silicon monolithic phase-inverter rat-race coupler using spiral coplanar striplines and its application in a broadband Gilbert mixer. IEEE Trans. Microw. Theory Tech., 56 (8) (2008), 1879–1888.
- [10] Lien, C.H.; Wang, C.H.; Lin, C.S.; Wu, P.S.; Lin, K.Y.; Wang, H.: Analysis and design of reduced-size Marchand rat-race hybrid for millimeter-wave compact balanced mixers in 130 nm CMOS process. IEEE Trans. Microw. Theory Tech., 57 (8) (2009), 1966– 1977.
- [11] Lien, C.H.; Wu, P.S.; Lin, K.Y.; Wang, H.: A 60 GHz single-balance gate-pumped down-conversion mixer with reduced-size rat-race hybrid on 130-nm CMOS process, In IEEE MTT-S Int. Microwave Symp. Digest, Atlanta, June 2008, 1481–1484.
- [12] Lien, C.H.; Huang, P.C.; Kao, K.Y.; Lin, K.Y.; Wang, H.: 60 GHz double-balanced gate-pumped down-conversion mixers with a combined hybrid on 130 nm CMOS process. IEEE Microw. Wirel. Compon. Lett., 20 (3) (2010), 160–162.
- [13] Razavi, B.: A millimeter-wave CMOS heterodyne receiver with on-chip LO and divider. IEEE J. Solid-State Circuits, 43 (2) (2008), 477-485.
- [14] Lee, J.; Liu, M.; Wang, H.: A 75-GHz phase-locked loop in 90 nm CMOS technique. IEEE J. Solid-State Circuits, 43 (6) (2008), 1414–1426.
- [15] Wu, C.R.; Hsieh, H.H.; Lu, L.H.: An ultra-wideband distributed active mixer MMIC in 0.18 μm CMOS technology. IEEE Trans. Microw. Theory Tech., 55 (4) (2007), 625–632.
- [16] Bao, M.; Jacobsson, H.; Aspemyr, L.; Carchon, G.; Xiao, S.: A 9– 31 GHz subharmonic passive mixer in 90 nm CMOS Technology. IEEE J. Solid-State Circuits, 41 (10) (2006), 2257–2264.



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