International Journal of Microwave and Wireless Technologies, 2014, 6(1), 13–21. © Cambridge University Press and the European Microwave Association, 2013
doi:10.1017/S1759078713001062

RESEARCH PAPER

A new GaN-based high-speed and high-power switching circuit for envelope-tracking modulators

PATRICK AUGEAU[1], PHILIPPE BOUYSSE[1], AUDREY MARTIN[1], JEAN MICHEL NEBUS[1], RAYMOND QUÉRÉ[2], LUC LAPIERRE[3], OLIVIER JARDEL[4] AND STÉPHANE PIOTROWICZ[4]

In this paper, we report a new high-speed and high-power switching circuit based on GaN HEMT's. The elementary switching cell, composed of two GaN HEMT's and two resistors, acts like a power threshold comparator with high-output voltage. Theoretical analysis of static and dynamic circuit operation points out the dependence of efficiency and switching speed to the main circuit elements. Four switching cells are then combined together thanks to SiC Schottky diodes to design a multi-level power switch that can be used as a power supply modulator for envelope tracking power amplifiers. The designed four-level supply modulator, based on Nitronex GaN HEMT's, exhibits more than 75% of efficiency for an envelope signal up to 4 MHz, a switching frequency of 20 MHz and output voltages in the range of 12–30 V.

Keywords: Power Amplifiers and Linearizers, Circuit Design and Applications

Received 28 June 2013; Revised 14 November 2013; first published online 19 December 2013

I. INTRODUCTION

New generations of wireless communication systems require data transmission rates that are constantly increasing. Modulation schemes needed to improve spectral efficiency result in radio frequency (RF) signals having large peak to average power ratios (PAPR). In order to ensure signal integrity, transmitters must meet stringent linearity specifications that put a challenging dilemma on DC consumption reduction and electrical efficiency enhancement of power amplifiers. Basically, linear amplification of non-envelope constant RF signals consists in using oversized PAs that operate at output power back off. Doing so, linearity performances are reached at the detriment of poor efficiency performances.

Envelope tracking (ET) is an interesting approach to overcome efficiency versus linearity antagonism. The quite simple idea is to save DC consumption of power amplifiers at backed off power levels by lowering dynamically the drain bias voltage synchronously with the instantaneous envelope decrease of the RF input signal. For that purpose, an envelope tracking power amplifier (ETPA) includes a drain bias modulator based on the use of a DC/DC converter to modulate drain bias versus instantaneous envelope variations of the input RF signal as illustrated in Fig. 1.

The output of the DC/DC converter supplies the drain port of the power amplifier with a time-varying voltage following a drain bias trajectory having a generic shape as illustrated in Fig. 2.

Drain bias trajectories required in ETPA can be done either in a continuous way (CET: continuous ET) or according to a discrete multilevel representation (MET: multilevel ET). In this work, a discrete four-level ET implementation is considered.

The drain bias modulator must be wideband and highly efficient, otherwise it impacts to much the overall efficiency and any implementation of ETPA architectures loses its interest. The design of wideband, high-power and efficient supply modulators still remains the cornerstone for adaptive, linear and efficient power amplification. GaN devices appear to be

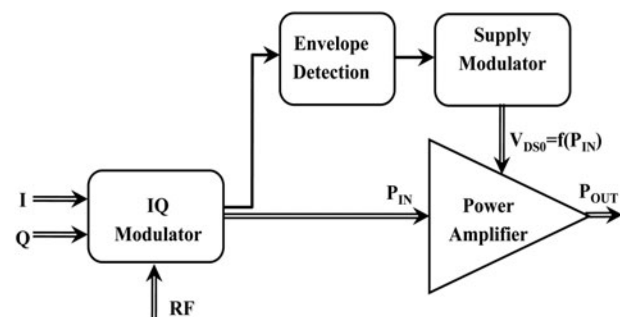

Fig. 1. Envelope tracking amplifier block diagram.

[1]XLIM C2S2, 123, Avenue Albert Thomas, 87000 Limoges Cedex, France. Phone: +33 555 457 295
[2]XLIM C2S2, 7, rue Jules Vallès, 19100 Brive, France
[3]CNES, 18 Av. Edouard Belin, 31055 Toulouse, France
[4]III-V Lab, route de Nozay, 91460 Marcoussis, France
Corresponding author:
P. Bouysse
Email: philippe.bouysse@unilim.fr

https://doi.org/10.1017/S1759078713001062 Published online by Cambridge University Press

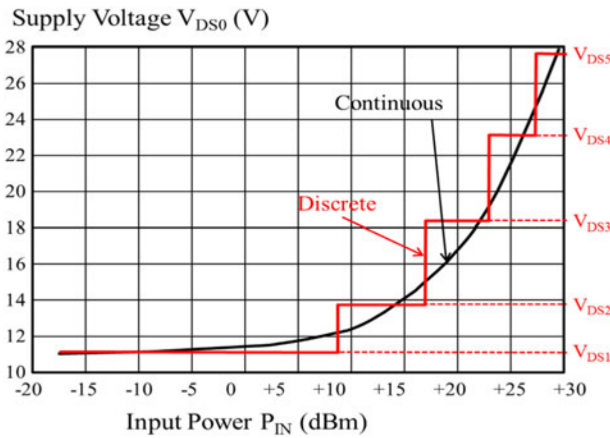

Fig. 2. Example of continuous and MET implementation.

the best potential candidates to face this challenge. A lot of works, proposing original supply modulator topologies, have been reported during the past years [1–10]. One of the most popular architecture is the hybrid switching amplifier (HSA) described in [2, 6–10].

This paper proposes a novel supply modulator topology, addressing the implementation of ETPA in base stations. The work reported here concerns the design and implementation of a discrete multilevel supply modulator. It is based on a novel high-speed and high-power GaN switching circuit that has not been yet reported to our knowledge.

In Section II, the core switching cell is presented. Static and dynamic behaviors are described. Fast transients and short switching times are highlighted.

Section III deals with the design of the supply modulator using an appropriate combination of the proposed switching cells. Some experimental results are discussed and demonstrated the potentialities of the proposed modulator.

To conclude further investigations are mentioned.

II. THE PROPOSED GAN HEMT SWITCHING CELL

A) The proposed core switching cell

The switching circuit topology is based on the use of two HEMT transistors as shown in Fig. 3.

For proper operation, transistor T_2, which is the main switching device delivering power to the load, is necessarily a normally-on transistor driven with a negative gate–source voltage. Transistor T_1 acts as a driver and controls the current in resistor R_2. T_1 and T_2 are power GaN devices of different sizes depending on the required output current as explained later in the paper.

The core switching circuit in Fig. 3 behaves like a threshold comparator with two stable ON/OFF states. Resistor R_1 ensures stability. Resistor R_2 enables the self-biasing of transistor T_2 during its OFF state.

ON State of the cell, ideally $V_{OUT} = V_{DD}$:

Transistor T_1 is pinched-off. No current flows across resistors R_1 and R_2. The gate–source voltage V_{GS2} is equal to zero. Transistor T_2 state is ON and its drain–source impedance is R_{ON}. The output voltage V_{OUT} is nearly equal to V_{DD}, neglecting the dropout voltage due to R_{ON}.

OFF State of the cell, ideally $V_{OUT} = V_P$:

Transistor T_1 state is ON. There is now a current flowing across resistors R_1 and R_2. Transistor T_2 reaches a self-biased point at a gate–source voltage V_{GS2} close to its pinch-off voltage V_P. Transistor T_2 is almost in an OFF state and V_{OUT} voltage is very close to V_P.

Dynamic switching characteristics

The analysis of switching transients is a key aspect to optimize maximum switching frequency and consequently the intrinsic speed capability of the proposed circuit for its use in wideband ETPA. Figure 4 shows the equivalent circuit used for the theoretical analysis of the circuit behavior. The goal here is to evaluate the dependence of the switching speed as a function of intrinsic capacitances of the main transistor T_2. The simplified model of T_2 is composed of two main capacitances C_{GS} and C_{DS} and a current controlled source I_D. Transistor T_1 is considered here as an ideal switch modeled by a serial resistor R_{T_1ON} or R_{T_1OFF}, depending on its ON/OFF state.

The current source I_D of T_2 is described by the piecewise equation (1) which is representative of the operating trajectory in the (I_D, V_{GS}) plane (see Fig. 5). The gate–source voltage V_{GS} is bounded between V_{GSOFF} and V_{GSON}, so that there is no need of defining an equation for V_{GS} values lower than pinch-off value $-V_p$. The ideal output load line in the (I_D, V_{DS}) plane, plotted in Fig. 5, is bounded between V_{DSON} voltage at low V_{DS} and V_{DSOFF} voltage at high V_{DS}. These ideal trajectories represent the static operation of the circuit. So, they depend only on resistive and convective intrinsic elements of transistors, there are no specific assumptions on capacitive elements. Concerning device T_1, the ON/OFF resistors R_{T_1ON}

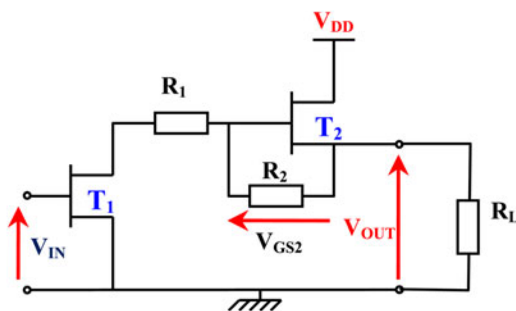

Fig. 3. Schematic representation of the core switching cell.

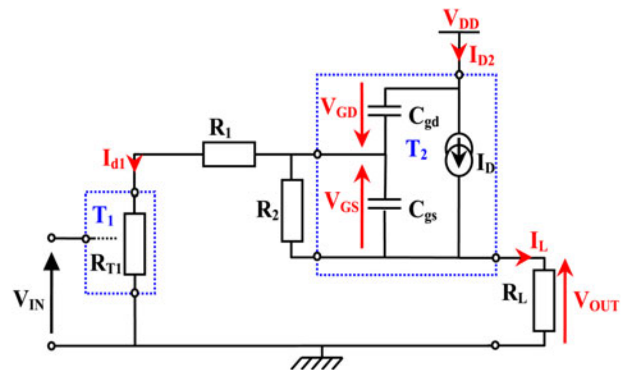

Fig. 4. Simplified schematic for theoretical analysis.

https://doi.org/10.1017/S1759078713001062 Published online by Cambridge University Press

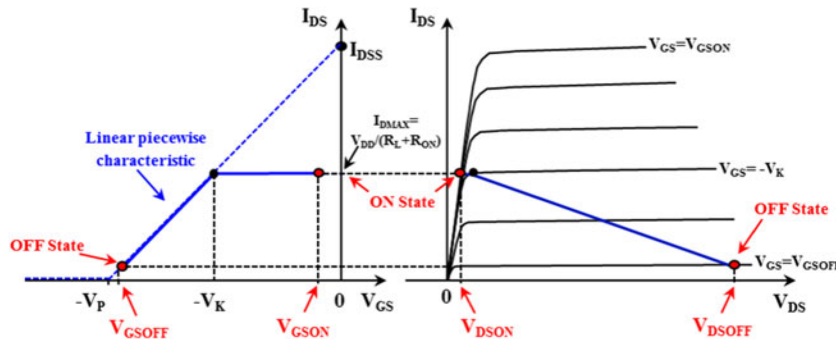

Fig. 5. Linear piecewise characteristic $I_D = f(V_{GS})$ of transistor T_2 and output ideal load line.

and R_{T1OFF} slightly impacts on V_{GSON} and V_{GSOFF} steady-state values. The resistor R_{ON} of device T_2 impacts on the value of V_{DSON} voltage and must be minimized to avoid a too important voltage drop at ON state.

$$\begin{cases} I_D = I_{DSS}\left(1 + \dfrac{V_{GS}}{V_p}\right) & \text{if } -V_P < V_{GS} < -V_K \\ I_D = \dfrac{V_{DD}}{R_L + R_{ON}} & \text{if } -V_K < V_{GS} < 0 \end{cases} \quad (1)$$

When switching from OFF to ON states, the current I_D reaches its maximum value I_{DMAX} (i.e. ON state value) at V_{GS} equal to the knee voltage $-V_K$. The value of V_K in equation (2) is obtained by combining equations (1) at the point $V_{GS} = -V_K$.

$$V_K = V_P\left(1 - \frac{V_{DD}}{(R_L + R_{ON})I_{DSS}}\right). \quad (2)$$

For V_{GS} values between $-V_P$ and $-V_K$, the current source I_D is described with the simplified linear equation of a transistor working in its saturation area. For V_{GS} values between $-V_K$ and 0, the transistor operates in the Ohmic area, and for convenience here, the drain current is assumed to be constant and independent of V_{GS} voltage. This particular trajectory, proper to this switch mode operation, has been validated by transient simulations achieved by using a complete non-linear transistor model.

Coming back to circuit schematic of Fig. 4 and going on with the piecewise analytical description of I_D current, two second-order differential equations of V_{GS} can be then derived. In order to simplify calculations, we use equations truncated to the first order (see equations (3) and (4)).

$$R_L I_{DSS} + \left(1 + \frac{R_{T1} + R_1 + R_L}{R_2} + \frac{R_L I_{DSS}}{V_P}\right)V_{GS}(t) + \left((R_{T1} + R_1)\left[C_{GS} + C_{GD}\left(1 + \frac{R_L I_{DSS}}{V_P} + \frac{R_L}{R_2}\right)\right] + R_L C_{GS}\right)\frac{dV_{GS}(t)}{dt} = 0, \quad \text{if } -V_P < V_{GS} < -V_K, \quad (3)$$

$$\frac{R_L V_{DD}}{R_L + R_{ON}} + \left(1 + \frac{R_{DS1} + R_1 + R_L}{R_2}\right)V_{GS}(t) + \left((R_{DS1} + R_1)\left[C_{GS} + C_{GD}\left(1 + \frac{R_L}{R_2}\right)\right] + R_L C_{GS}\right)\frac{dV_{GS}(t)}{dt} = 0, \quad \text{if } -V_K < V_{GS} < 0. \quad (4)$$

The initial value V_{GSOFF} is determined by solving equation (3) considering the steady-state $(d/dt = 0)$ and taking $R_{T1} = R_{T1ON}$.

$$V_{GSOFF} = \frac{-R_L I_{DSS}}{\left(\dfrac{R_{T1ON} + R_1 + R_L}{R_2} + \dfrac{R_L I_{DSS}}{V_P} + 1\right)}. \quad (5)$$

Starting from this initial value, the OFF–ON transition is analyzed using equations (3) and (4). The resolution of equations (3) and (4) leads to an OFF–ON transient composed of two steps as shown in Fig. 6. The first step, in which the output voltage V_{OUT} is established, has a duration t_K. Then, during the second step, the V_{GS} voltage continues to increase up to V_{GSON} final value.

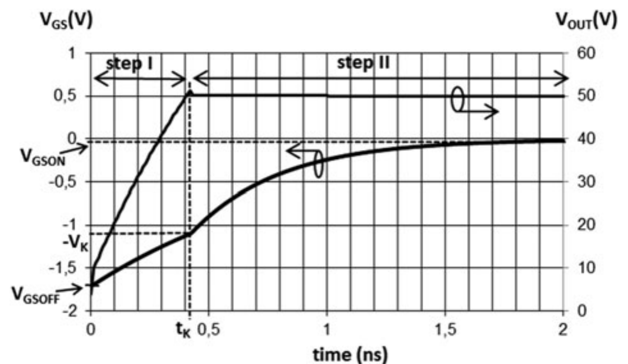

Fig. 6. V_{GS} and V_{OUT} time waveforms during OFF → ON transition for $R_1 = 8\ \Omega$, $R_2 = 35\ \Omega$, $R_L = 80\ \Omega$, $V_{DD} = 50$ V, $R_{ON} = R_{T1ON} = 2\ \Omega$, $R_{T1OFF} = 100$ KΩ, $I_{DSS} = 1.6$ A, $V_P = 1.8$ V, $C_{GS} = 10$ pF, $C_{GD} = 0.25$ pF.

https://doi.org/10.1017/S1759078713001062 Published online by Cambridge University Press

The expression of t_K is given in equation (6) where τ_1 and V_0 are constants derived from solving equation (3).

$$t_K = -\tau_1 \ln\left[\frac{V_K + V_0}{V_0 - V_{GSOFF}}\right], \quad (6)$$

where

$$V_0 = \frac{-R_L I_{DSS}}{1 + \frac{R_{T_1OFF} + R_1 + R_L}{R_2} + \frac{R_L I_{DSS}}{V_P}} \quad (7)$$

and

$$\tau_1 = \frac{(R_{T_1OFF}+R_1+R_L)C_{GS}+(R_{T_1OFF}+R_1)C_{GD}\left(1+\frac{R_L I_{DSS}}{V_P}+\frac{R_L}{R_2}\right)}{1+\frac{R_{T_1OFF}+R_1+R_L}{R_2}+\frac{R_L I_{DSS}}{V_P}}. \quad (8)$$

In the ideal case where R_{T1OFF} tends to infinity and R_1 to zero, the expression of t_K reduces to equation (9). This expression highlights the dependence of the switching time t_K as a function of intrinsic capacitances of T_2. A simple numerical evaluation shows that the contributions of C_{GS} and C_{GD} capacitances are almost the same. The switching speed is directly linked to the amount of electrical charges stored in the capacitances. Although C_{GD} is smaller than C_{GS}, it is charged with V_{GD} voltage, which is about 20 times higher than V_{GS} voltage. Finally, these two capacitances store almost identical charges.

Equation (9) also shows that the switching time t_K is minimized if $-V_K$ tends to V_{GSOFF}. This can be done by increasing I_{DSS}, i.e. by oversizing T_2 comparatively to the required I_{DMAX} current.

$$t_K = \left(R_2 C_{GS} + R_2 C_{GD}\left(1 + \frac{R_L I_{DSS}}{V_P} + \frac{R_L}{R_2}\right)\right) \times \ln\left[\frac{-V_K}{V_{GSOFF}}\right]. \quad (9)$$

The second step of the OFF–ON transition is done by solving equation (4). This step is characterized by a time constant τ_2 (equation (10)) and the V_{GSON} steady-state value (equation (11)). In this step, V_{OUT} voltage is already established and we can consider that the cell is switched on, the time constant τ_2 affects only V_{GS} voltage.

$$\tau_2 = \frac{(R_{T_1OFF}+R_1+R_L)R_2 C_{GS}+(R_{T_1OFF}+R_1)R_2 C_{GD}\left(1+\frac{R_L}{R_2}\right)}{R_{T_1OFF}+R_1+R_2+R_L}, \quad (10)$$

$$V_{GSON} = -\frac{R_L}{(R_L + R_{ON})}\frac{R_2 V_{DD}}{(R_{T_1OFF} + R_1 + R_L + R_2)}. \quad (11)$$

A similar theoretical analysis for the ON–OFF transition is performed and it shows that the ON–OFF switching time is at least five times lower than t_K, depending on component values.

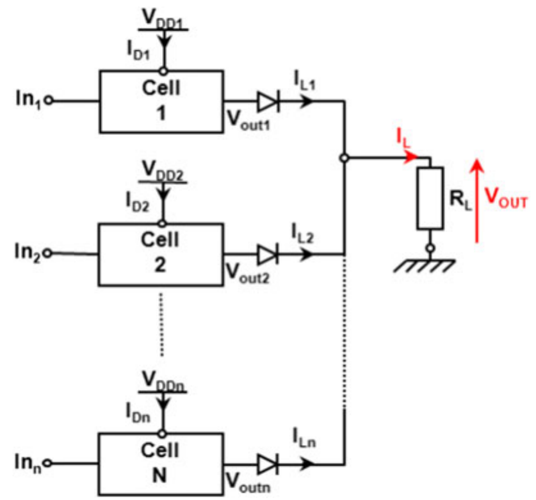

Fig. 7. Block diagram of the N cells multilevel modulator.

To sum up, the switching speed of the cell is limited by the OFF–ON switching time (t_k). It can be minimized by using large size power transistors with small pinch-off voltages.

III. IMPLEMENTATION OF THE ET MODULATOR

A) Schematic and performance analysis of the MET modulator

The block diagram of the proposed discrete multilevel supply modulator is given in Fig. 7. It consists in switching N DC supplies having different V_{DDi} voltage values to a common load R_L. For that purpose the output of each switching cell is connected to the load through a fast switching diode. Depending on the required voltage V_{DDi} across the load, only one switching cell among N is active at a same time and feeds the load with current flowing from DC bias V_{DDi}. Diodes ensure isolation between the output of the activated cell and the output of all other inactivated cells. Otherwise there would exist a current sinking at the output of inactivated cells.

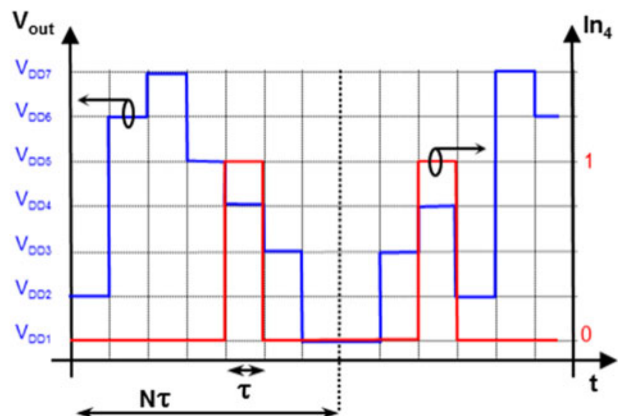

Fig. 8. Example of V_{OUT} time waveform and fourth cell input signal ($N = 7$).

https://doi.org/10.1017/S1759078713001062 Published online by Cambridge University Press

Let us now consider a theoretical analysis of the supply modulator DC consumption. In the following, power efficiency performances are calculated during the steady states and power losses occurring during voltage transients are not taking into account. An example of ideal discrete multilevel output voltage waveforms is given in Fig. 8, corresponding to the combination of seven switching cells. As mentioned earlier that only one switching cell is in an ON state, whereas all the others are in OFF states. It is also assumed that the activation of each cell follows a uniform density probability. Considering N cells and a recurrence time equal to $N\tau$, each switching cell is activated during a time τ and is inactivated during a time equal to $(N-1)\tau$. Each input control signal, noted In_i in Fig. 7, has a duty cycle $\lambda = 1/N$.

Considering the basic operation of each switching cell described in the Section II.B and following assumptions mentioned above, the expression of the average DC supply power and the average output power of the supply modulator are given respectively in equations (12) and (13).

$$P_{SUPtot} = \sum_{i=1}^{N} P_{SUPi} = \frac{1}{N}\sum_{i=1}^{N}\left(\frac{V_{DDi}^2}{R_L + R_{ON}} - (N-1)\frac{V_{GSOFF}V_{DDi}}{R_2}\right), \quad (12)$$

$$P_{OUT} = \frac{1}{N}\sum_{i=1}^{N}\frac{1}{R_L}\left(\frac{R_L}{R_L + R_{ON}}V_{DDi} - V_{Diode}\right)^2. \quad (13)$$

The supply modulator efficiency η is given equation (14).

$$\eta = \frac{P_{OUT}}{P_{SUPtot}} = \frac{\sum_{i=1}^{N}\frac{1}{R_L}\left(\frac{R_L}{R_L + R_{ON}}V_{DDi} - V_{Diode}\right)^2}{\sum_{i=1}^{N}\left(\frac{V_{DDi}^2}{R_L + R_{ON}} - (N-1)\frac{V_{GSOFF}V_{DDi}}{R_2}\right)}. \quad (14)$$

with V_{GSOFF} expression given in equation (5).

DC powers (P_{SUPtot}) and output powers (P_{OUT}) as well as efficiency are plotted versus the number of cells respectively in Figs. 9 and 10. Minimum and maximum supply voltages are respectively $V_{DD1} = 14$ V and $V_{DDn} = 50$ V. N intermediate values V_{DDi} are uniformly distributed in the range V_{DD1} to V_{DDn}.

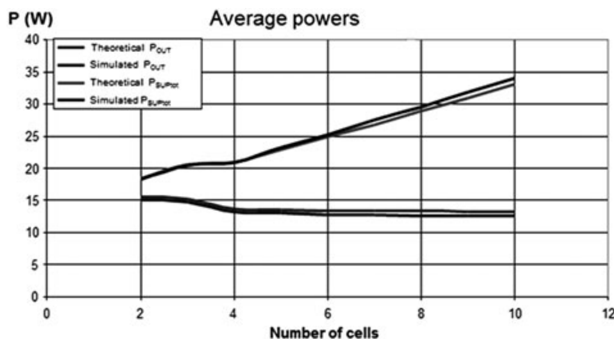

Fig. 9. Average powers versus the number of cells for $R_1 = 8\ \Omega$, $R_2 = 90\ \Omega$, $R_L = 80\ \Omega$, $R_{ON} = 2\ \Omega$, $I_{DSS} = 1.6$A, $V_P = 2.1$ V.

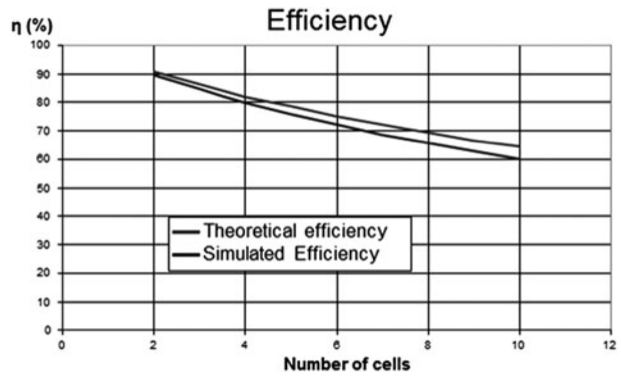

Fig. 10. Efficiency versus the number of cells for $R_1 = 8\ \Omega$, $R_2 = 90\ \Omega$, $R_L = 80\ \Omega$, $R_{ON} = 2\ \Omega$, $I_{DSS} = 1.6$ A, $V_P = 2.1$ V.

Analytical calculations are compared to ADS simulation results. ADS transient simulations are performed by taking a recurrence time $N\tau$ of 200 ns. For simulation purpose, a nonlinear model of a 6 × 400 µm GaN HEMT from III–V Lab foundry was used.

We can observe a good agreement between simulated and theoretical results. The simulated curves indicate slightly lower performances because they take into account power losses during transients.

When the number of cells increases, the output power remains quasi-constant, while the DC supply power increases, leading to efficiency decrease. In fact, inactive cells consume some energy. As the number of inactive cells increases, the corresponding dissipated power increases, inducing a reduction of the efficiency. Consequently, according to our experience, we can consider that an optimal number of switching cell is of the order of four.

In Fig. 10, the theoretical efficiency curve is the optimal curve for this set of values. The simulated curve is slightly lower because it takes into account transition losses.

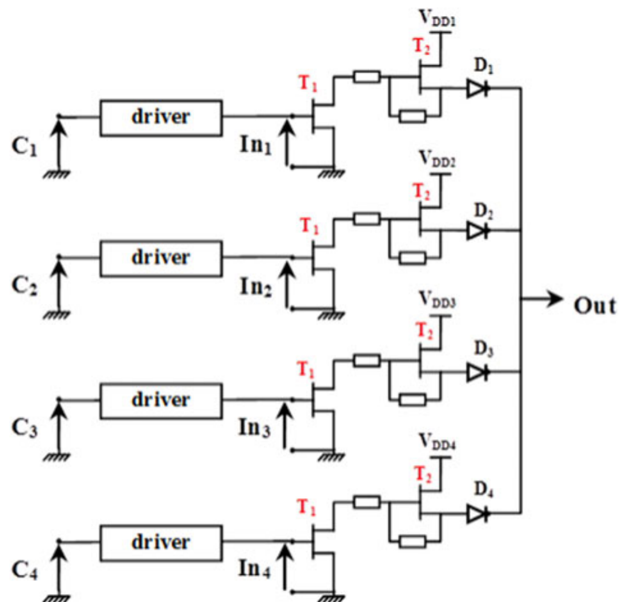

Fig. 11. Block diagram of the complete MET modulator (four cells).

https://doi.org/10.1017/S1759078713001062 Published online by Cambridge University Press

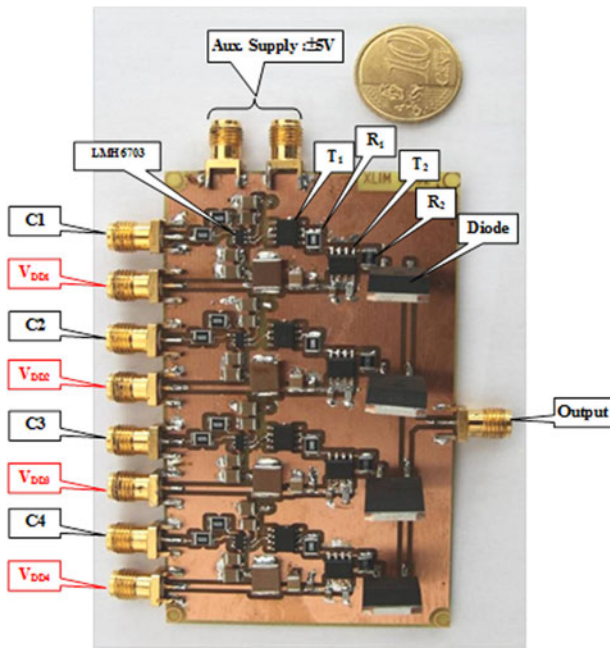

Fig. 12. Photography of the MET modulator.

IV. DESIGN AND IMPLEMENTATION

A) Four-level MET modulator

This part is devoted to the implementation of a four-cell supply modulator as presented in Fig. 11. T_1 and T_2 transistors are RF GaN HEMT's on Si substrate from Nitronex. Their nominal output powers are 5 W (NPTB00004) for T_1 and 45 W (NPT1004) for T_2. Maximum currents are respectively 1.3 and 9.5 A.

The input signals $C_{1,\ldots,4}$ (Fig. 11) are digital signals coming from an FPGA. Driver blocks are realized with fast 1 GHz bandwidth LMH6703 Operational Amplifiers from Texas Instruments.

These drivers allow us to:

- Match voltage levels between FPGA outputs and T_1 transistor gate ports. FPGA output voltages are between 0 and 3 V and signal driving T_1 gates must be between 0 and −3 V.
- Supply T_1 transistor gates at high frequency with sufficient current.
- Isolate FPGA outputs from the high-power switching circuit.

Silicon carbide Schottky diodes CSD01060 from CREE are used. These diodes present negligible recovery time and a sufficient current handling (5 A). They are not limiting components in terms of switching speed but it is necessary to take into account their DC consumption in the whole power efficiency budget.

The photography of the built-in four-level MET modulator is depicted in Fig. 12.

B) MET modulator characterization setup

The overview of the complete ET system is presented in Fig. 13. The input envelope signal is digitized by using a 14 bits −50 MHz ADC. Only the two MSB bits are used by the FPGA to generate four command signals (C_i) required for driving the switching cells.

The LTC2285 ADC demoboard from *Linear Technology* that we use has two channels, 125MSPS maximal sampling speed and 1–70 MHz input frequency bandwidth. The *Xilinx* FPGA is on a *Digilent* development board.

V. EXPERIMENTAL RESULTS

A) Measurements with an envelope signal having a ramp waveform

In a first validation test, we use a 5 MHz frequency ramp as the input envelope signal. The sampling frequency is fixed to 20 MHz. The discrete supply values are 12, 18, 24 and 30 V and the load R_L is 50 Ω. The output voltage V_{OUT} measured across the load resistance R_L is plotted in Fig. 14.

We can observe that measurements are very close to the ideal theoretical signal. We observe a dropout voltage of about 1.2 V compared to the power supply voltages for each of the four steady-state output levels. This dropout voltage is due to the dropout voltage across Schottky diodes estimated to 0.6 V and the saturation voltage V_{DSsat} of the power transistor T_2 estimated to 0.6 V. For the 30 V switching state, the current flowing across the transistor T_2, which is also the current in R_L, is equal to 580 mA. In this case, the R_{ON}

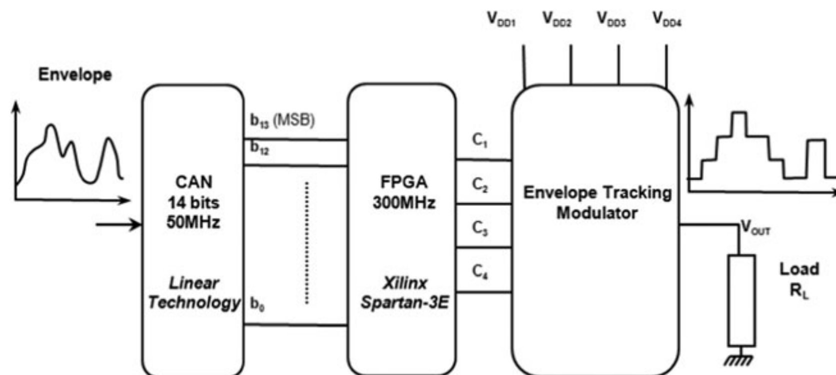

Fig. 13. Complete MET modulator system.

https://doi.org/10.1017/S1759078713001062 Published online by Cambridge University Press

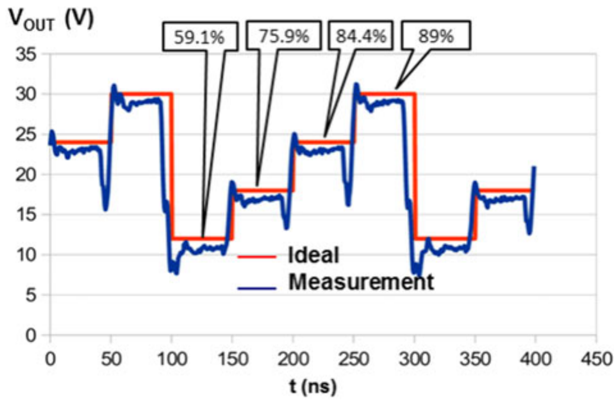

Fig. 14. Output voltage with a 5-MHz ramp waveform.

resistance of transistor T_2 is about 1 Ω. The efficiency of the system for every switching state is indicated in Fig. 14.

B) MET modulator performances versus envelope frequency

In a second test, we use a 2 MHz sinusoidal input envelope signal. The measured time domain waveform of the output voltage V_{OUT} is plotted in Fig. 15.

The average efficiency is calculated on one period of the envelope signal and is defined as the ratio between the average output power and the average supply power. The average output power is derived from the measured RMS value of V_{OUT} voltage. This average efficiency takes into account efficiencies at each switching state, it depends on the probability of each state and thus on the envelope waveform. The average efficiency of the system was measured when varying the envelope frequency in the range 200 KHz–4 MHz (see Fig. 16). The efficiency decreases with the envelope frequency.

When applying this sine wave envelope test signal, every cell is activated with a same probability and same time duration. In the case of a useful radiocommunication signals, the contribution of each cell to the output voltage Vout will be very different. The average efficiency of the MET modulator depends on the statistical properties of the envelope signal (PDF, PAPR). The target of this work is to build a supply modulator having at least 80% efficiency and 10 MHZ bandwitdh. A fully integrated implementation, using GaN dies instead of package and surface-mounted devices, is under development at III-V Lab foundry. This integrated structure, in progress, will enable to reduce switching times and will provide thermal dissipation improvements.

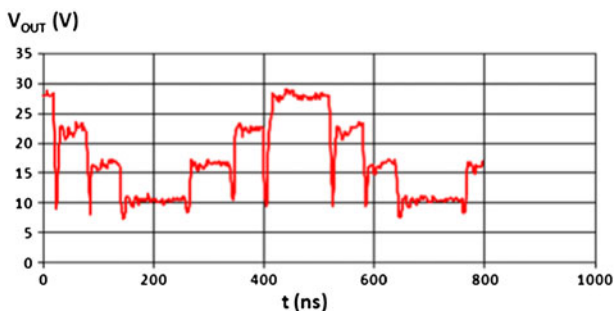

Fig. 15. Time waveform of the output voltage for $V_{DDmax} = 30$ V.

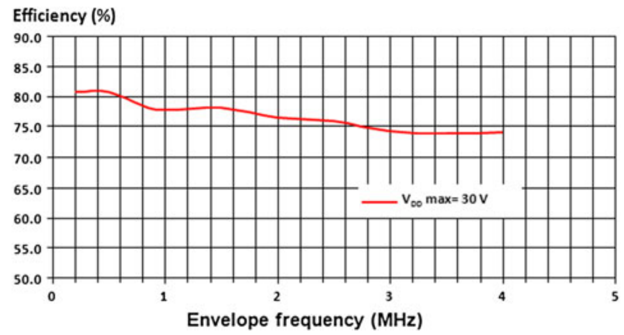

Fig. 16. Average efficiency versus envelope frequency for $V_{DDmax} = 30$ V.

VI. CONCLUSION

In this paper, we have presented a high-speed and high-power supply modulator based on the use of GaN HEMT power transistors. A novel switching cell architecture has been proposed and described. Using the proposed core switching cell, we have built a multilevel supply modulator demo board for ET applications. Experimental results have validated the technique for switching different supply voltages at high frequency. Improvement of this first prototype in terms of switching speed and enhanced efficiency will be achieved with an integrated design.

Work in progress will now consist in coupling of the proposed supply modulator to the drain bias port of an RF power amplifier driven by variable envelope RF signals. An important first aspect to be noticed is that power performances of the proposed supply modulator remain very insensitive to load variations.

ACKNOWLEDGEMENTS

The authors wish to address special acknowledgements to Dr. L. Bacqué who has first imagine the switching cell circuit during his Ph.D. thesis [11] at XLIM Laboratory in 2008, in collaboration with the CNES Toulouse (French National Space Research Center). Following this initial work, an in-depth analysis of the switching circuit and the implementation of the MET modulator have been performed and supported by the French FUI Project ALPAGA2, involving III-V Lab, AMCAD, Thalès TCS and XLIM UMR CNRS 7252 University of Limoges.

REFERENCES

[1] Kim, B. et al.: Push the envelope: design concepts for envelope-tracking power amplifiers. IEEE Microw. Mag., **14** (3) (2013), 68–81, IMS special issue May.

[2] Kimball, D.F. et al.: High-efficiency envelope-tracking W-CDMA base-station amplifier using GaN HFETs. IEEE Trans. Microw. Theory Tech., **54** (11) (2006), 3848–3856.

[3] Forestier, S.; Bouysse, P.; Quere, R.; Mallet, A.; Nebus, J.-M.; Lapierre, L.: Joint optimization of the power-added efficiency and

https://doi.org/10.1017/S1759078713001062 Published online by Cambridge University Press

the error-vector measurement of 20-GHz pHEMT amplifier through a new dynamic bias-control method. IEEE Trans. Microw. Theory Tech., **52** (4) (2004), 1132–1141.

[4] Hoyerby, M.C.W.; Andersen, M.A.E.: High-bandwidth, high-efficiency envelope tracking power supply for 40 W RF power amplifier using paralleled bandpass current sources, in IEEE 36th Power Electronics Specialists Conf., 2005 (PESC '05), 2005, 2804–2809.

[5] Bacque, L. et al.: High-current–high-speed dynamic bias control system applied to a 100-W wideband push–pull amplifier. IEEE Trans. Microw. Theory Tech., **56** (12) (2008), 2798–2807.

[6] Aitto-oja, T.: High efficiency envelope tracking supply voltage modulator for high power base station amplifier applications, in 2010 IEEE MTT-S Int. Microwave Symp. Digest (MTT), 23–28 May 2010, 668–671.

[7] Yan, J.J.; Hsia, C.; Kimball, D.F.; Asbeck, P.M.: GaN envelope tracking power amplifier with more than one Octave Carrier Bandwidth, in 2011 IEEE Compound Semiconductor Integrated Circuit Symp. (CSICS), 16–19 October 2011, 1–4.

[8] Hsia, C.; Kimball, D.F.; Asbeck, P.M.: Effect of maximum power supply voltage on envelope tracking power amplifiers using GaN HEMTs, in 2011 IEEE Topical Conf. Power Amplifiers for Wireless and Radio Applications (PAWR'11), 16–19 January 2011, 69–72.

[9] Kim, J.; Son, J.; Jee, S.; Kim, S.; Kim, B.: Optimization of Envelope Tracking Power Amplifier for Base-Station Applications. IEEE Trans. Microw. Theory Tech., **61** (4) (2013), 1620–1627.

[10] Kanbe, A. et al.: New architecture for envelope-tracking power amplifier for base station, in IEEE Asia Pacific Conf. Circuits and Systems, 2008 (APCCAS 2008), November 30 2008–December 3 2008, 296–299.

[11] Bacqué, L.: Optimisation du rendement d'amplificateurs de puissance sous contrainte de linéarité en présence de modulations numériques complexes, PhD Thesis no. 2008LIMO441, University of Limoges, France, 2008.

Patrick Augeau received the Electrical Engineering degree from ENSIL Limoges, France, in 2009. Since 2010, he is working toward his Ph.D. degree at the XLIM laboratory in Limoges. His main field of interest concerns the development of supply modulators for the implementation of envelope tracking on telecommunication power amplifiers.

Philippe Bouysse received his Ph.D. degree in Communication Engineering from the University of Limoges, France, in 1992. Since 1992, he has been with the University of Limoges, as a teacher and researcher with the XLIM Laboratory. His main research interests are the design and optimization of microwave power amplifiers. He is currently involved in designing supply modulators for envelope tracking implementation.

Audrey Martin received her Ph.D. degree from the Limoges University, France, in 2007. She is presently a teacher and researcher with XLIM Laboratory, University of Limoges. Her main research interests include active microwave and millimeter-wave circuit design, wideband power amplifiers and non-linear modeling techniques. She is also interested in the development of characterization and modeling of graphene devices.

Jean-Michel Nebus received his Ph.D. degree in electronics from the University of Limoges France in 1988. Then he has worked for 2 years as a Project Engineer with Alcatel Space Industries, Toulouse, France. He is currently a Professor with the XLIM Laboratory, University of Limoges. His main research interests are the optimization of linearity and efficiency of microwave power amplifiers.

Raymond Quéré (Fellow IEEE) received the Electrical Engineering degree from ENSEEIHT Toulouse, France in 1976 and the French "agrégation" in applied physics in 1978. He earned a Ph.D. degree (with honors) from University of Limoges in 1989 and was appointed full professor at the University of Limoges. Since 1998 he leads the non-linear high-frequency devices, circuits, and systems research department at XLIM-CNRS laboratory. His main field of interest is in the area of non-linear device and circuit modeling with a particular emphasis on non-linear phenomena such as stability in power amplifiers. He advises more than 30 Ph.D. students and he authors or co-authors more than 100 journal articles or communications in international conferences such as IMS/MTT, EuMW ... He was the co-author of the book "Nonlinear Stability of Nonlinear Microwave Circuits". In 2005, he was appointed as the general Chairman of the European Microwave Week in Paris.

Luc Lapierre was born in Clermont-Ferrand, France, in 1957. He received the Dipl-Ing degree from the Ecole Superieure d'Electricite (ESE), Paris, Gif sur Yvette, France, in 1980. In December 1981, he joined the French National Space Centre (CNES), Toulouse, France, where he was involved in microwave research activities mainly oriented on solid-state components. He also provides technical support in the development of microwave equipments for satellite payloads. He has been the Head of the Microwave Department, CNES, and is currently a Microwave Expert with the Microwave and Time Frequency Department, CNES.

https://doi.org/10.1017/S1759078713001062 Published online by Cambridge University Press

Olivier Jardel was born in Poitiers, France, in 1981. He received an engineering degree from the University of Aix-Marseille I, in 2004, and the Ph.D. degree from the University of Limoges in 2008, in the common laboratory MITIC between XLIM and III-V Lab. He is currently a research engineer at III-V Lab, working on the development of the AlInN/GaN HEMT technology, on transistor modeling and on the design of power amplifiers.

Stéphane PIOTROWICZ was born in France 1971. He received the Ph.D. degree in Electronics from the University of Lille in 1999. He Joined the Thales Research Center and worked on the design of Hybrid and MMIC power amplifiers on the InGaP/GaAs HBT technology for Radar and Space Applications. He currently works on the development of GaN technologies at III-V Lab (a joint lab of Alcatel-Lucent Bell Labs France, Thales Research and Technology & CEA Leti). He is in charge of the design and characterization team involved the realization of hybrid and MMIC circuits for T/R modules as power switches, power amplifiers and low noise amplifiers.

https://doi.org/10.1017/S1759078713001062 Published online by Cambridge University Press