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RESEARCH PAPER

High power density SiGe millimeter-wave power amplifiers

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This paper presents measured results for two-stage and three-stage high-voltage/high-power (HiVP) amplifiers implemented in a commercial 0.12 μm silicon germanium (SiGe) heterojunction bipolar transistor (HBT) bipolar Complementary Metal Oxide Semiconductor (BiCMOS) process at millimeter wave. The HiVP configuration provides a new tool for millimeter-wave silicon designers to achieve large output voltage swings, high output power density, customizable bias, and a way to minimize, if not eliminate, matching circuitry at millimeter-wave frequencies. The two-stage amplifier has achieved a $P_{SAT} = 5.41$ dBm with a power added efficiency (PAE) of 8.06% at center frequency 30 GHz. The three-stage amplifier has achieved a $P_{SAT} = 8.85$ dBm with a PAE of 11.35% with a total chip area of 0.068 mm² at center frequency 30 GHz. Simulation, layout, fabrication, and measurement results are presented in this paper.

Keywords: Circuit design and applications, Microwave measurements, Power amplifiers and linearizers, Radar applications, Si-based devices and IC technologies

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I. INTRODUCTION

While silicon-based technologies have become competitors in the millimeter-wave arena [1–5], the continued scaling of silicon processes, in order to increase f_T/f_{MAX}, has lowered bias voltages and therefore output voltage swings of silicon power amplifiers (PAs), from one process generation to the next [6]. Low RF output power has been a large contributing factor in stifling silicon-based technologies to provide commercial single-chip millimeter-wave solutions [7, 8]. In an attempt to counter the effects of lowered bias voltages, two approaches are commonly used to increase the radio frequency (RF) output power of silicon-based PAs: device paralleling and power combining [9].

While the paralleling of transistors increases the RF output current swing of the amplifier, and therefore, the RF output power, it lowers the output impedance of the amplifier and increases the quiescent current flow in Class A amplifiers, having an impact on power added efficiency (PAE). On chip power combiners, passive or active, can lead to large chip area, RF power loss, and poor power density. In this paper, a third approach to increase RF output power is discussed, implemented in silicon at millimeter wave, and its measurements presented. The approach, called the high-voltage/high-power (HiVP) configuration, increases the RF output voltage swing of the amplifier, increases the output impedance, and allows for a customizable bias for the designer, ensuring a configuration that can be used from one process generation to the next [10].

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II. CONCEPT

A) DC perspective

The schematics for a two-stage and three-stage silicon germanium (SiGe) heterojunction bipolar transistor (HBT) HiVP are shown in Figs 1(a) and 1(b), respectively. For clarity, the schematics are shown without input or output matching circuitry. From a DC perspective HBTs Q_{1-2} (for the two-stage device) and HBTs Q_{1-3} (for the three-stage device) are stacked in a cascode fashion, essentially in DC series. The total DC bias becomes $V_{CC} = N$ (the number of transistors in the stack) × V_{CE} (for an individual transistor). The bases of transistor's Q_{1-N} are biased from the single V_{CC} supply, through a corresponding resistor-ratioed current mirror stack formed by Q_{B1-BN} and $R_{1(A\&B)-N(A\&B)}$. The operation of the current mirror will be discussed later, but it is sufficient to say the devices in Q_{1-N} will provide the RF amplification and Q_{B1-BN} will provide DC bias.

B) RF perspective

What differentiates this configuration from the classic cascode configuration is the size of the base capacitors (C_{1-N}) in Figs 1(a) and 1(b). The base capacitors are not large enough to act

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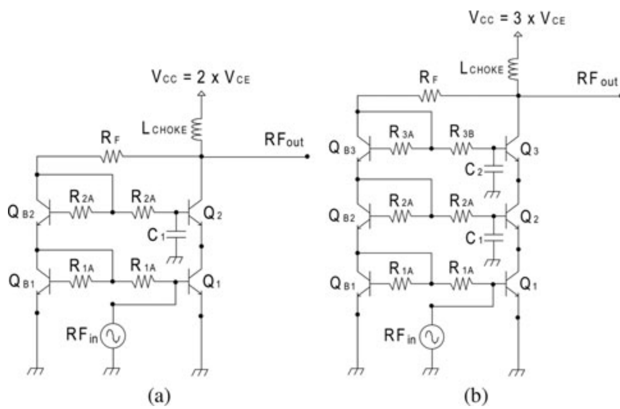

Fig. 1. (a, b) Two-stage SiGe HBT HiVP (a – left) and three-stage SiGe HBT HiVP (b – right).

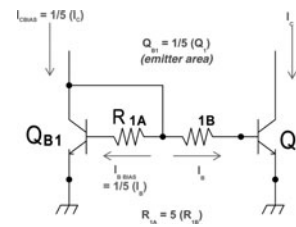

Fig. 2. Resistor-ratioed current mirror.

as a signal ground, essentially leaving each of the bases floating. Instead, they are sized to a first-order approximation using equation (1), where $C_1$is the base capacitor and C_{be} is the internal base–emitter capacitance of the HBT [9]. The role of the base capacitor is to adjust the emitter impedance of the transistor it is attached to. By adjusting the impedance seen at the transistor's emitter, it can be set to act as the optimal load to the collector of the transistor that precedes it. Using Fig. 1(a) as an example, C_1 is sized to ensure $Z_{emitter}$ of Q_2 is equal to optimal load for Q_1. Once this tuning is achieved in simulation, the RF signal exiting Q_1 will be optimally transferred to the emitter of Q_2, in effect transistors Q_{1-N}, will be in RF series as well as DC series:

$$Z_{emitter} \approx \left(\frac{1}{g_m}\right)\left(1 + \frac{C_{be}}{C_1}\right). \qquad (1)$$

The final component of the HBT HiVP configuration is the feedback resistor (R_F) shown in both Figs 1(a) and 1(b). The function of R_F is to provide a current reference for the resistor-ratioed current mirror. Under RF power, R_F ensures that the current reference to the mirror swings up and down with the collector voltage of the top transistor Q_N. This enables a maximum output voltage swing of twice V_{CC}. In addition, it prevents the breakdown (BV_{CBO}) of each transistor by ensuring that each transistor is constantly biased in saturation, as the RF output voltage of the amplifier swings up and down.

C) Resistor-ratioed current mirror

A current mirror allows for precise control over the base current that biases the SiGe HBTs in the main stack (Q_{1-N}) in Figs 1(a) and 1(b). A resistor-based voltage ladder will not work well for SiGe HBT devices as they are extremely sensitive to very small fluctuations in base–emitter voltage [10]. Any mismatch in resistor sizes to due fabrication error would result in transistors in the main stack having different bias points. In Figs 1(a) and 1(b), the transistors in the main stack (Q_{1-N}) are of identical emitter area to ensure the same DC current flow in the stack. The transistors in the bias stack (Q_{B1-BN}) also have identical emitter area to one another, but that area is set at a ratio of 1:5 to the emitter area of the transistors in the main stack. Each transistor in the stack is biased via a corresponding resistor-ratioed current mirror. Transistors Q_1 and Q_{B1} from Figs 1(a) and 1(b) are enlarged in Fig. 2. In Fig. 2, Q_{B1} has 1/5 the emitter area of Q_1. The 1:5 ratio is to some extent arbitrary; the smaller the ratio, the higher the PAE of the amplifier will become, but the limit will depend on transistor emitter area sizes available in the process design kit. Therefore careful consideration of design goals must be used in determining the ratio.

The resistors in the mirror must be in the same ratio as the transistor's emitter areas. In Fig. 2, resistor R_{1A} is five times larger than R_{1B}, ensuring that five times the current will be provided to transistor Q_1 as Q_{B1}. The ratio allows the use of a far smaller transistor than a traditional current mirror, decreasing both the area of the bias stack and the quiescent current for the bias stack, having the effect of increasing the amplifier's PAE. The ratio of resistors guards against potential fabrication errors, ensuring that an exact size is not necessary as long as the ratio is correct, thus lowering the area of the resistors needed, as tight tolerance resistors typically have large areas in most design kits.

III. IMPLEMENTATION

Originally implemented in GaAs MESFETs (MEtal Semiconductor Field Effect Transistor) at 3.5 GHz [10], and more recently in SiGe HBTs at 2.4 GHz [9], the HiVP configuration discussed in this paper has been implemented using SiGe HBTs at millimeter wave, with a center frequency of 30 GHz – a frequency of interest for the sponsors of this work. For both the two-stage and three-stage amplifiers, double-stripe-high-f_T SiGe HBTs with emitter area of 18 μm × 120 nm were used in the main transistor stacks, whereas single-stripe-high-f_T SiGe HBTs with emitter area of 3.46 μm × 120 nm were used in the bias stacks.

The DC, small signal, harmonic balance simulation techniques outlined earlier [9] were used to design the two- and three-stage stacks in this work. Figure 3(a) shows the dynamic-load-line simulation for a single SiGe HBT. Figures 3(b) and 3(c) show the dynamic-load-line simulations for the two-stage and three-stage amplifiers. Figure 3(a) shows that the RF output voltage swing for a single SiGe HBT with an optimal load is approximately 1.4 V. Figure 3(b) shows that the RF output voltage swing for the two-stage amplifier is approximately 2.2 V, while the output voltage swing for the three-stage amplifier in Fig. 3(b) is 4.5 V. The saturated output power of the amplifiers was measured at 5.41 and 8.85 dBm, respectively, which was a 2.2-fold increase in output power, due to the approximately two-fold increase in output voltage swing, achieved through the addition of one stage.

The optimal loads for the single HBT, the two-stage, and three-stage amplifier are $43.74 + j53$, $110 + j30$, and $120 +$

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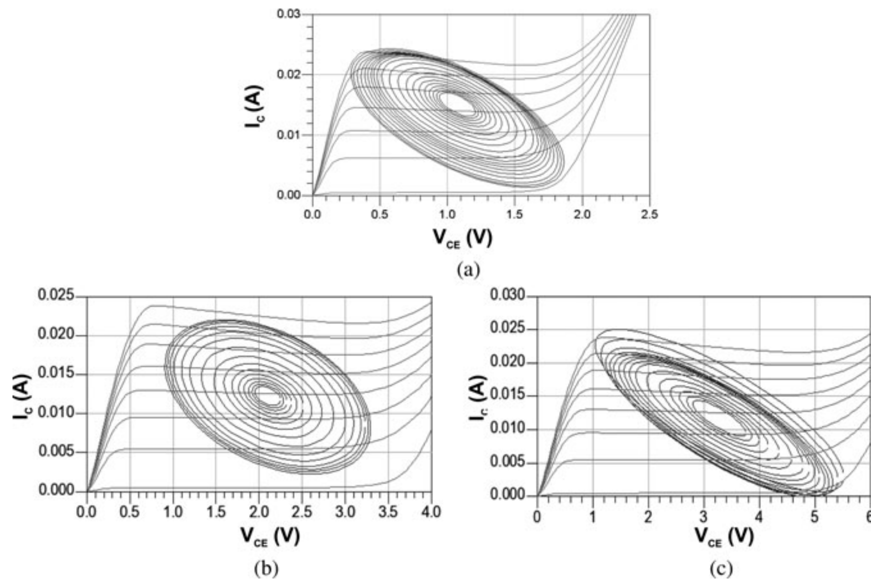

Fig. 3. (a–c) Dynamic load line simulations, one-stage (a – top), two-stage (b – bottom left), and three-stage (c – bottom right) SiGe HiVPs.

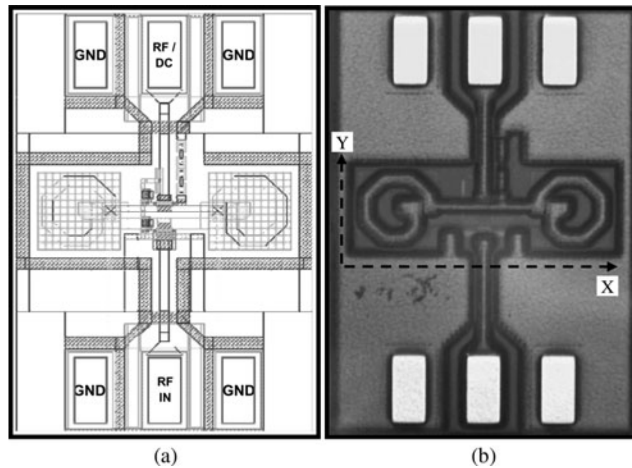

Fig. 4. (a, b) CAD layout (a – left) and microphotograph (b – right) of two-stage SiGe HiVP; $X = 400\ \mu m \times Y = 170\ \mu m$.

$j45\ \Omega$, respectively. As each stage is added the output impedance is increasing as expected.

The CAD layout and fabricated microphotograph of the two-stage SiGe HBT HiVP is shown in Figs 4(a) and 4(b), respectively. The values for the components in Figs 4(a) and 4(b) are listed in Table 1. The layout is the implementation of the schematic in Fig. 1(a), with a 0.1 nH inductor inserted between Q_1's collector and Q_2's emitter. The inductance was necessary to further adjust Q_2's emitter impedance, as Q_2's base capacitor could not provide enough tuning range to reach the optimal impedance required by Q_1's collector. This inductance was split into two 0.2 nH inductors in parallel in order to ensure symmetry. In future layouts, it is recommended that a small length of thick metal replaces the large area inductances. In this work, a parameterized inductor cell was used to avoid EM simulation to verify the accuracy of the process design kit provided by the foundry models.

The CAD layout and fabricated microphotograph of the three-stage SiGe HBT HiVP is shown in Figs 5(a) and 5(b), respectively. The values for the components in Figs 5(a) and 5(b) are listed in Table 2. No inductance was necessary between stages 1 and 2, as in the two-stage design, as the optimal load impedance was adequately met by stage 2 with only the base capacitor C_1. This led to the even

Table 1. Component values for two-stage SiGe HiVP.

Schematic label	Value or size	Layout specifics
Q_1/Q_2	Double-emitter SiGe HBT	120 nm × 18 μm, 1-finger
Q_{B1}/Q_{B2}	Single-emitter SiGe HBT	120 nm × 3.46 μm, 1-finger
C_1	25 fF (4 in series 107 fF)	8 × 13 μm
L_1	0.1nH (2 in parallel)	OD = 100 μm, $W = 14.4$ μm
R_{1A}/R_{2A}	28.5 kΩ	2 × 8.87 μm (4 in series)
R_{1B}/R_{2B}	5.5 kΩ	2 × 2.23 μm (4 in series)
R_F	11.32 Ω	15.68 × 5 μm
Probe pads	N/A	50 × 102 μm, NS backplane

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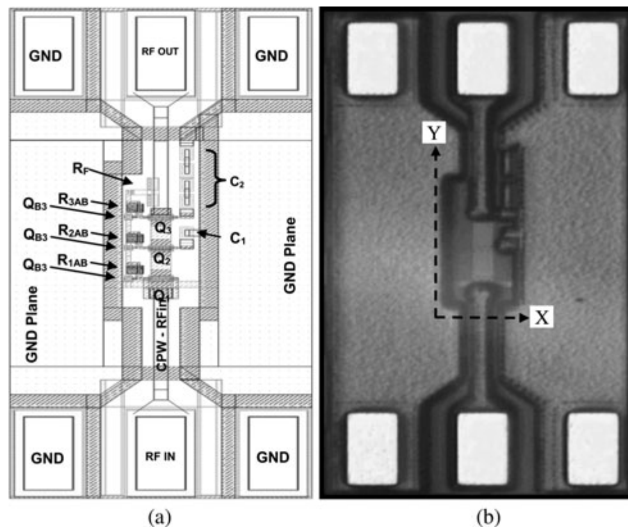

Fig. 5. (a, b) CAD layout (a – left) and microphotograph (b – right) of three-stage HiVP circuit, $X = 60$ μm × $Y = 200$ μm.

Table 2. Component values for three-stage SiGe HiVP.

Schematic label	Value or size	Layout specifics
$Q_1/Q_2/Q_3$	Double-emitter SiGe HBT	120 nm × 18 μm, 1-finger
$Q_{B1}/Q_{B2}/Q_{B3}$	Single-emitter SiGe HBT	120 nm × 3.46 μm, 1-finger
C_1	100 fF	8 × 11.4 μm
C_2	25 fF (4 107 fF in series)	8 × 12 μm
$R_{1A}/R_{2A}/R_{3A}$	28.5 kΩ	2 × 8.87 μm (4 in series)
$R_{1B}/R_{2B}/R_{3B}$	5.5 kΩ	2 × 2.23 μm (4 in series)
R_F	11.32 Ω	15.68 × 5 μm
Probe pads	N/A	50 × 102 μm, NS backplane

smaller layout area and also increased the power density of the circuit.

IV. MEASUREMENTS

For the two-stage device both the small and large signal measurements were made with $V_{CC} = 2.2$ V and $I_C = 12.8$ mA. For the three-stage device, all measurements were made with $V_{CC} = 3.28$ V and $I_C = 14.3$ mA. The simulated versus measured small signal measurements for the two-stage and three-stage SiGe HBT amplifiers with 50 Ω terminations are shown in Figs 6(a) and 6(b), respectively. It should be noted that no matching circuitry was integrated on-chip; a custom impedance was desired by the designer for eventual integration of these amplifiers into a power combining structure. At 30 GHz, the two-stage device small signal gain was measured at 7.96 dB, whereas the three-stage device measured 11.18 dB.

The large signal simulation and measurements at 30 GHz for the two-stage device are shown in Figs 7(a) and 7(b), respectively. The measurements were made using a load-pull measurement system, where the optimal source and load impedance were characterized and presented to the device for optimal output power. With an area of only 0.068 mm^2, at 30 GHz, the 1-dB compressed output power was measured at 3.37 dBm with a PAE of 6.14%, whereas saturated power was measured at 5.41 dBm with a PAE of 8.06%. It is expected that PAE would decrease slightly when the device is matched to 50 Ω due to losses in the matching circuit.

The large signal simulation and measurements at 30 GHz for the three-stage device are shown in Figs 8(a) and 8(b), respectively. The measurements' optimal source and load impedance were characterized and presented to the device for optimal output power. With an area of only 0.12 mm^2, at 30 GHz, the 1-dB compressed output power was measured at 3.32 dBm with a PAE of 5.3%, whereas saturated power was measured at 8.85 dBm with a PAE of 11.35%. It should be noted that while the 11.35% PAE was achieved at 8 dB of compression, the 8 dB is shared across the three stages of the HiVP stack resulting in 8 dB/3 stages = 2.6 dB per stage, a safe operating region for each of the underlying amplifiers.

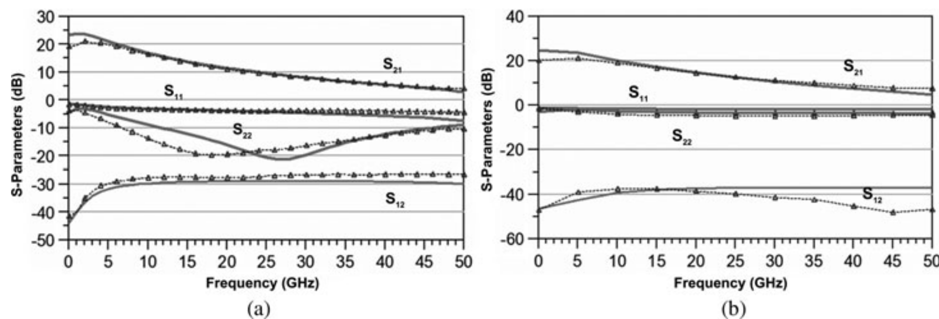

Fig. 6. (a, b) *S*-parameters for two-stage (a – left) and three-stage (b – right); red – sim., blue – meas.

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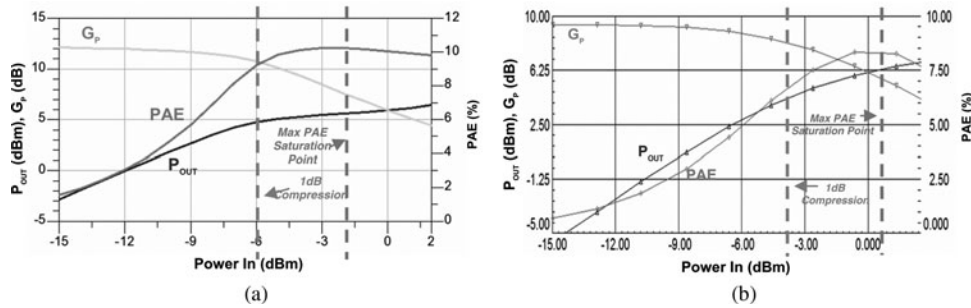

Fig. 7. (a, b) Power characteristics for two-stage device (a – left) simulation (b – right) measurements at 30 GHz.

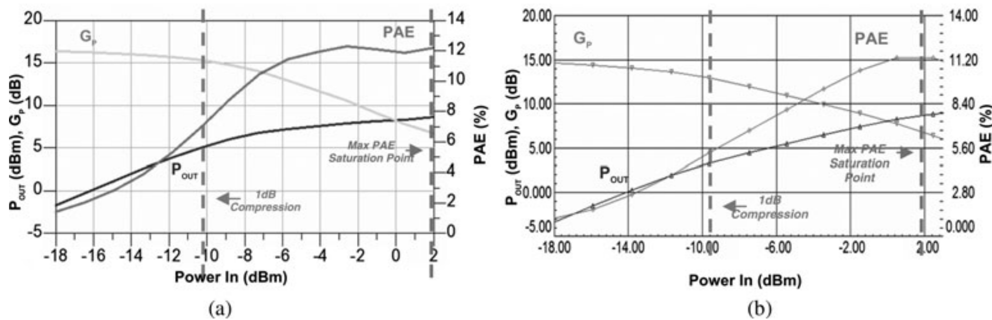

Fig. 8. (a, b) Power characteristics for three-stage device (a – left) simulation (b – right) measurements at 30 GHz.

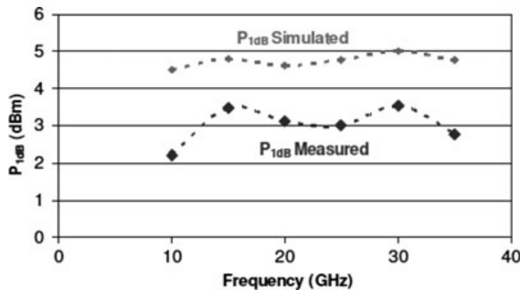

Fig. 9. $P - 1$ dB versus frequency for three-stage device (red) simulation (blue) measurements W/50 Ω terminations.

Figure 9 shows $P - 1$ dB versus frequency for the three-stage device. $P - 1$ dB was plotted for frequencies: 10–35 GHz in 10 GHz steps. The figure shows the simulated versus measured values of $P - 1$ dB with 50 Ω terminations at each frequency and not the idea load. As one might expect the simulated values (shown in red) are higher than measured values (shown in blue) as is typically the case for the large signal model of silicon-based processes. The purpose of this measurement is to show the bandwidth of the PA across a wide frequency range.

V. CONCLUSION

A two- and three-stage SiGe HBT HiVPs have been designed, fabricated, and measured in a 0.12 μm commercial SiGe bipolar complementary metal oxide semiconductor (BiCMOS) process. Although EM tools were used to optimize the layout, the foundry provided models have provided fairly accurate prediction of the final results obtained in measurement. The simulation techniques followed were the procedures outlined in [9]. Measured results of 11.18 dB of small signal gain – 8.85 dBm of saturated output power with a PAE of 11.35% – have been achieved in only 0.012 mm² of area using the SiGe HBT HiVP configuration. We found very good agreement between simulation and measurement in both small and large signal characterizations. The work presented in this paper represents an initial successful attempt at the use of the HiVP configuration at across a wide band of millimeter-wave frequencies. It is intended to provide verification of the architecture at high frequencies, and offers the silicon designer a simple alternative for increasing output power density, output impedance, and bias over conventional methods available in the literature.

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