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RESEARCH PAPER

80-GHz-band low-power sub-harmonic mixer IC with a bottom-LO-configuration in 130-nm SiGe BiCMOS

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In this paper, a W-band (80 GHz) sub-harmonic mixer (SHM) IC is designed, fabricated and measured in 130-nm SiGe BiCMOS technology. The presented SHM IC makes use of a common emitter common collector transistor pair structure with a bottom-LO-configuration to decrease the LO power requirement and a tail current source to flatten the conversion gain. On-chip Marchand balun is designed for W-band on-wafer measurements. The SHM IC presented in this paper has exhibited a conversion gain of 3.9 dB at 80 GHz RF signal with an LO power of only −7 dBm at 39.5 GHz. The mixer core consumes only 0.68 mA at a supply voltage of 3.3 V.

Keywords: W-band, 130-nm SiGe BiCMOS, Sub-harmonic mixer, CECCTP, Bottom-LO-configuratoin, Marchand Balun, Low power

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I. INTRODUCTION

Nowadays, W-band (around 80 GHz) is widely used all over the world for several applications, such as automotive radar [1, 2], high-speed networks [3], imaging, and gesture recognition [4]. In 2009, European Telecommunication Commission Institute (ETSI) has assigned a short range radar band from 77 to 81 GHz [1]. In 2012, the International Telecommunication Union (ITU) has recommended vehicular collision avoidance radars in the frequency band from 77 to 81 GHz [2] and fixed wireless systems operating in the 71–76 and 81–86 GHz range [3]. A 94 GHz pulsed-radar transceiver was reported for the applications of imaging and gesture recognition [4].

Mixer is a key component of the radiofrequency (RF) transceivers. For W-band receivers, sub-harmonic mixer (SHM) is an attractive solution since it mixes the RF signal with the second harmonic of LO (2^*f_{LO}) signal. With relatively low oscillation frequency, the oscillator has better phase noise performance, and the buffer of the oscillator can provide higher LO power with lower power consumption [5].

Since the passive SHMs have significant conversion loss, there are many topologies reported to implement active SHMs with conversion gain. Paper [5] reported an SHM topology with a compact input network, which transfers RF signals from single-ended to differential while keeping LO signals in phase at the base of the differential transistors. This topology has high LO–RF and 2LO–RF isolation between the LO and RF ports. However, it is challenging to realize the RF and LO input matching at the same time. Thus, this topology requires high LO pumping power.

Gilbert-cell SHMs with three-level stacked-LO switching core [6–9] are widely used, which use the current switching mechanism to generate 2^*f_{LO} signal for mixing. Other Gilbert-cell leveled-LO SHM topologies were reported including both bottom-LO configuration [10–12] and top-LO configuration [13–15], which use the nonlinearities of transistors to generate 2^*f_{LO} signal for mixing. The design trade-offs of the Gilbert-cell SHMs between stacked-LO and leveled-LO configurations were reported in [16]. It is reported that Gilbert-cell stacked-LO SHM has lower LO power requirement but lower operational frequency than the Gilbert-cell leveled-LO SHMs. This trade-off is mainly caused by the different operational principles. The transistor switching characteristic used by stacked-LO SHM is sensitive to signal frequency. The transistor nonlinearities used by leveled-LO SHMs is sensitive to signal power. In addition, all these Gilbert-cell SHM topologies require a precise quadrature LO signal and have complicated circuit layouts.

The common emitter common collector transistor pair (CECCTP) SHMs with top-LO-configuration were also reported in [17, 18]. Owing to differential LO signal input and simple circuit layout, CECCTP structure is considerable for millimeter-wave SHM IC. In the conventional top-LO-configured CECCTP SHM, however, the bottom RF stage suppresses the generation of 2^*f_{LO} signal and results in a high requirement of LO power. Hence, we propose an improved bottom-LO-configured CECCTP SHM IC with a tail current source for W-band applications [19]. The

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improved SHM topology has following features: (1) the required LO power is only −7 dBm, (2) the conversion gain is flattened and not sensitive to LO power, (3) the DC power consumption is only 2.2 mW.

130-nm SiGe BiCMOS technology with a cut-off frequency of over 200 GHz is applied to design and fabricate the SHM IC. For comparison, a conventional top-LO-configured SHM IC is also designed and fabricated. Integrated Marchand balun is designed for W-band on-wafer measurements. In this paper, the working principles of the bottom-LO-configured SHM (with and without a tail current source) and the conventional top-LO-configured one are described and compared in Section II. The circuit design and simulated performance of both the improved and conventional SHM ICs are presented in Section III. Section IV demonstrates the measurement results and is followed by a conclusion.

II. OPERATION PRINCIPLES

A) Conventional top-LO-configured CECCTP SHM

Figure 1(a) illustrates the core circuit of the conventional top-LO-configured CECCTP SHM. Load and bias circuits are not drawn for simplicity. HBT Q1 serves as a transconductance amplifier for RF input stage. HBTs Q2 and Q3 form a CECCTP stage to generate second harmonic of the LO signal (2^*f_{LO}). The frequency mixing principle of this SHM is very similar to the dual-gate mixer analyzed in paper [20]. The generated 2^*f_{LO} signal modulates the collector voltage of Q1 and switches Q1 between the saturation and forward active region over 2^*f_{LO} cycle. Since the bias current and transconductance of Q1 are modulated by 2^*f_{LO} signal, the RF signal is mixed with the 2^*f_{LO} signal and the IF signal ($f_{IF} = f_{RF} - 2^*f_{LO}$) is generated. It is noted that the 2^*f_{LO} power significantly influences the Q1 modulation and the conversion gain of SHM.

In order to maximize the generation of 2^*f_{LO} signal, Q2 and Q3 are biased to work in switching mode [21], which means that when one transistor is turned on, the other one is turned off. Figure 1(b) shows the simplified model of the LO frequency-doubling stage. For each half cycle, Q2 or Q3 works like a common emitter amplifier with a degeneration resistor R_1. Hence, the magnitude of the collector current is decreased and the generation of 2^*f_{LO} in the output current (I_{out}) is suppressed.

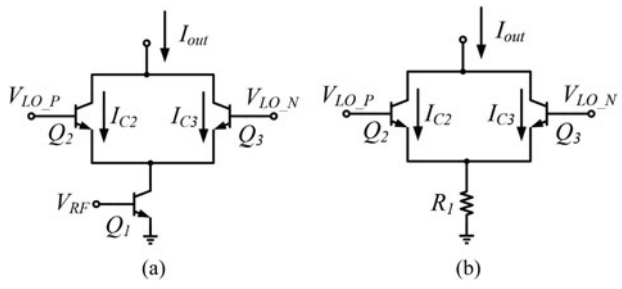

Fig. 1. (a) Simplified schematic of the conventional top-LO-configured CECCTP SHM. (b) Modeling of the LO frequency-doubling stage.

B) Bottom-LO-configured CECCTP SHM with a tail current source

1) SCHEMATIC OF THE BOTTOM-LO-CONFIGURED SHMS

Figure 2(a) shows the simplified schematic of the core of the bottom-LO-configured CECCTP SHM. Since the common emitter point of Q2 and Q3 is connected to ground, the CECCTP effectively enlarges the generation of 2^*f_{LO} for mixing. Since this is a voltage-biased structure and the base-to-emitter bias voltage of Q2 and Q3 are constant, DC and 2^*f_{LO} component of I_{out} are very sensitive to LO power. Hence, a tail current source is employed to stabilize the DC bias current, as shown in Fig. 2(b). Large shunt capacitor (C_{TAIL}) provides an AC ground. This is a current-biased structure, and the potential of node A is floated. Thus, the base-to-emitter bias voltage (V_{be_bias}) of Q2 and Q3 could be adaptively changed to keep DC component of I_{out} constant and to flatten the 2^*f_{LO} generation.

2) COMPARISON OF THE SHMS WITH TOP AND BOTTOM LO CONFIGURATIONS

Figure 3 shows the simulated load-lines of the HBT Q1 (solid line) in the top-LO-configured SHM in Fig. 1(a) and that of the HBT Q1 (dotted line) in the bottom-LO-configured

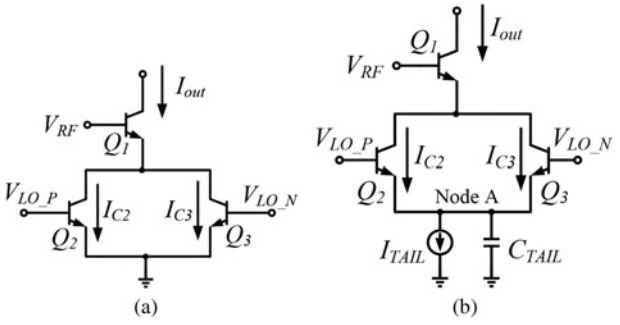

Fig. 2. Simplified schematic of the (a) bottom-LO-configured CECCTP SHM, (b) bottom-LO-configured CECCTP SHM with tail current source.

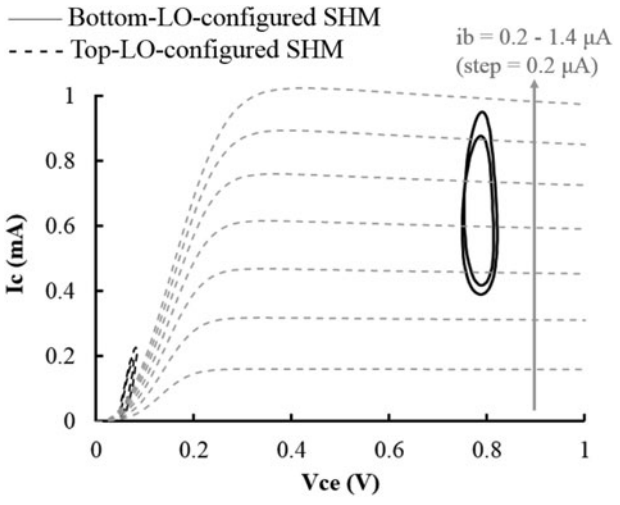

Fig. 3. Simulated load-lines of the HBT Q1 (RF stage) in the SHMs with top and bottom LO configurations.

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SHM in Fig. 2(b), respectively. Since RF input is small signal and LO input is large signal, both SHMs are applied with no RF power and an LO power of −7 dBm at 39.5 GHz to simulate the load-lines of HBT Q1. In the top-LO-configured SHM, the 2^*f_{LO} modulates the collector-to-emitter voltage (V_{ce}) and collector current (I_c) of Q1. The RF stage operates between the saturation and slightly forward active region and generates the f_{IF} signal. In the bottom-LO-configured SHM, the 2^*f_{LO} modulates the base-to-emitter voltage (V_{be}) and collector current (I_c) of Q1. The RF stage operates in the forward active region and generates the f_{IF} signal. When the LO power is low, the bottom-LO-configured SHM generates higher 2^*f_{LO} current swing than the top-LO-configured one, as shown in Fig. 3.

3) EFFECTIVENESS OF THE TAIL CURRENT SOURCE IN THE BOTTOM-LO-CONFIGURED SHM

In order to quantitatively analyze the difference of the 2^*f_{LO} generation between the circuits in Figs. 2(a) and (b), the collector current (I_c) of HBT is modeled as a train of rectified cosine pulses. Figure 4 shows the calculated time-domain waveforms of the collector current and base voltage in the CECCTP stage. I_{max} is the peak current of I_c. I_{C2} and I_{C3} refer to the collector current of Q2 and Q3, respectively. V_{be2} and V_{be3} refer to the base-to-emitter voltage of Q2 and Q3, respectively. V_{be_max} and V_{be_min} refer to the HBT base-to-emitter voltage swing, V_{be_on} is the threshold voltage of HBT, t_o is the width of the current pulses, and T is the period of the fundamental frequency.

I_{out} can be represented using a Fourier-series expansion:

$$\begin{aligned} I_{out}(t) &= I_{C2} + I_{C3} \\ &= I_0 + I_1\cos(\omega_1 t) + \cdots + I_n\cos(\omega_n t), \end{aligned} \tag{1}$$

where I_n is the nth-harmonic current component. The DC component I_0 in I_{out} is:

$$I_0 = I_{max}\left|\frac{2\theta_t}{\pi^2}\right| \tag{2}$$

and the second harmonic (I_2) in I_{out} is:

$$I_2 = I_{max}\left|\frac{\theta_t\cos(\theta_t)}{\pi^2/4 - {\theta_t}^2}\right|, \tag{3}$$

where θ_t is the conduction angle. When t increases from 0 to $t_0/2$, V_{be2} decreases from V_{be_max} to V_{be_on}, as shown in Fig. 4:

$$(V_{be\_max} - V_{be\_bias}) \times \cos\left(\frac{2\pi}{T} \times \frac{t_0}{2}\right) = V_{be\_on} - V_{be\_bias}. \tag{4}$$

Hence, θ_t can be expressed as a function of V_{be_bias}, input power of LO signal (P_{LO}) and the input impedance of CECCTP frequency-doubling stage (R_{LO}):

$$\begin{aligned} \theta_t = \frac{2\pi}{T} &= 2\cos^{-1}\left(\frac{V_{be\_on} - V_{be\_bias}}{V_{be\_max} - V_{be\_bias}}\right) \\ &= 2\cos^{-1}\left(\frac{V_{be\_on} - V_{be\_bias}}{\sqrt{2P_{LO} \times R_{LO}}}\right). \end{aligned} \tag{5}$$

For simplicity, the transconductance performance of HBT is assumed to be constant when input power changes. Thus, current swing I_{max} is proportional to the voltage swing $V_{be\_max} - V_{be\_on}$:

$$\begin{aligned} I_{max} &= g_m(V_{be\_max} - V_{be\_on}) \\ &= g_m\left(1 - \cos\frac{\theta_t}{2}\right)\sqrt{2P_{LO} \times R_{LO}}. \end{aligned} \tag{6}$$

Since V_{be_bias} is constant in Fig. 2(a), θ_t drastically increases when P_{LO} increases, as shown in equation (5). From equations (3) and (6), I_2 can be expressed as:

$$I_2 = g_m\sqrt{2P_{LO} \times R_{LO}}\left(1 - \cos\frac{\theta_t}{2}\right) \times \left|\frac{\cos(\theta_t)}{\pi^2/4 - {\theta_t}^2}\right|. \tag{7}$$

Since I_0 is constant ($I_0 = I_{TAIL}$) and V_{be_bias} is floated in Fig. 2(b), V_{be_bias} decreases and θ_t slightly decreases when P_{LO} increases, as shown in equation (2). From equations (2) and (3), I_2 can be expressed as:

$$I_2 = I_{TAIL}\frac{\pi^2}{2} \times \left|\frac{\cos(\theta_t)}{\pi^2/4 - {\theta_t}^2}\right|. \tag{8}$$

The I_2 in equation (7) has additional polynomials about θ_t and P_{LO}, compared with the I_2 in equation (8). Hence, a tail current source could make I_2 (2^*f_{LO} in I_{out}) insensitive to θ_t, and meanwhile could make I_2 insensitive to P_{LO}. It is expected that the SHM with the tail current source in Fig. 2(b) generates 2^*f_{LO} more smoothly than the SHM in Fig. 2(a).

Figure 5 shows the simulated dependence of 2^*f_{LO} (I_2) in I_{out} on the LO input power in the conventional top-LO-configured SHM (gray solid line), the bottom-LO-configured SHM without I_{TAIL} (black dashed line) and the improved bottom-LO-configured SHM with I_{TAIL} (black solid line).

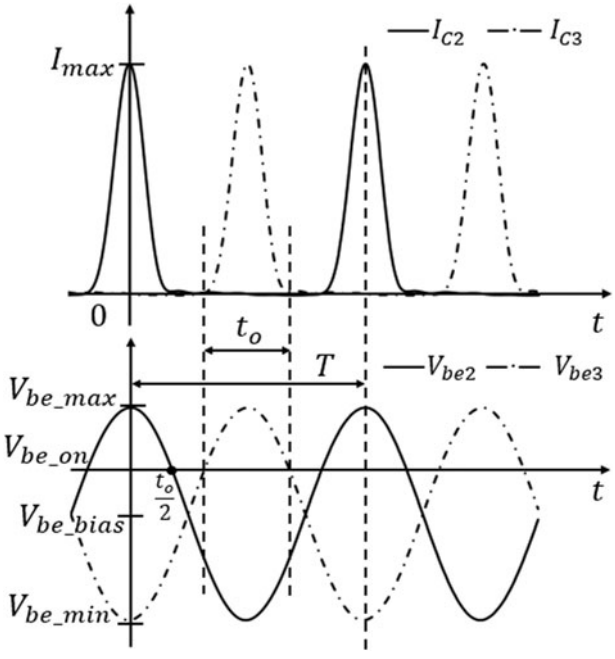

Fig. 4. Collector current and base voltage time-domain waveforms in the CECCTP frequency-doubling stage.

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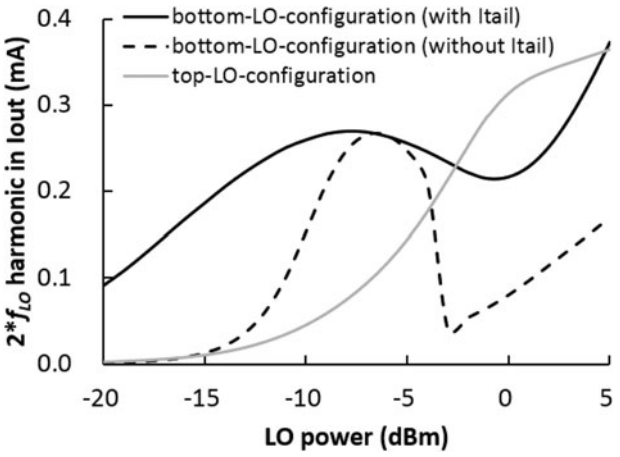

Fig. 5. Magnitude of the 2^*f_{LO} of I_{out}.

Differential LO signal at 39.5 GHz is applied to the CECCTP frequency doubling stage. The improved SHM in Fig. 2(b) effectively enlarges and flattens the 2^*f_{LO} in I_{out} with low LO input power range.

III. CIRCUIT DESIGN

Figure 6 shows the schematic of the conventional top-LO-configured CECCTP SHM IC. HBTs Q1, Q2, and Q3 form the SHM core. The supply voltage for the conventional SHM core is 2.5 V. For on-wafer measurements, integrated Marchand balun is designed at the LO input port to transfer the differential balanced 50 Ω port to a single-ended unbalanced 50 Ω port. Since the center frequencies of LO and RF signals are 39.5 and 80 GHz, respectively, spiral inductors are utilized for the LO matching circuit and a microstrip line is used for the RF matching circuit.

Figure 7 shows the schematic of the bottom-LO-configured SHM IC with a tail current source presented in this paper. HBTs Q1, Q2, Q3, Q4, and Q5 form the SHM core, where Q4 and Q5 serve as the tail current mirror. The supply voltage for the SHM core is 3.3 V. Both SHMs employ the same emitter follower as the IF buffer amplifier with a supply voltage of 1.8 V.

Figures 8(a) and 8(b) illustrate the top and side views of the Marchand balun IC design, respectively. As shown in Fig. 8(a), a pair of coupled spiral transmission lines are employed for magnetic coupling and port transformation. As shown in

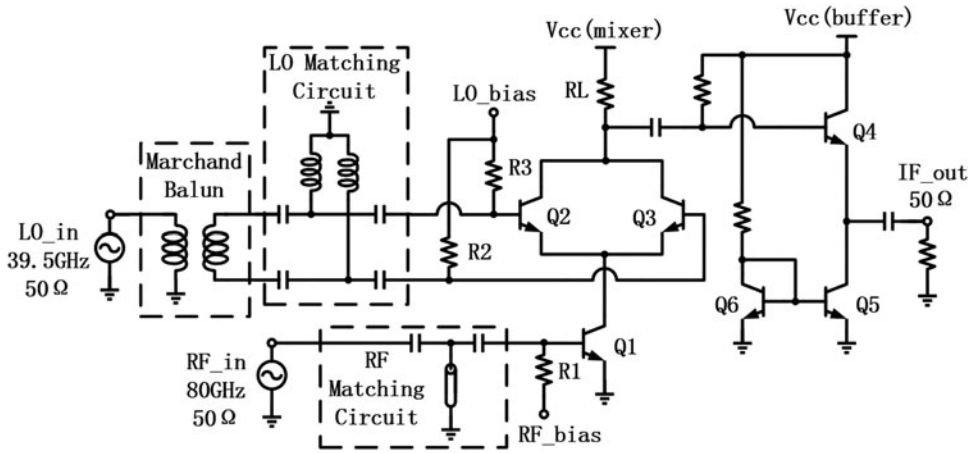

Fig. 6. Schematic of the conventional top-LO-configured CECCTP SHM IC.

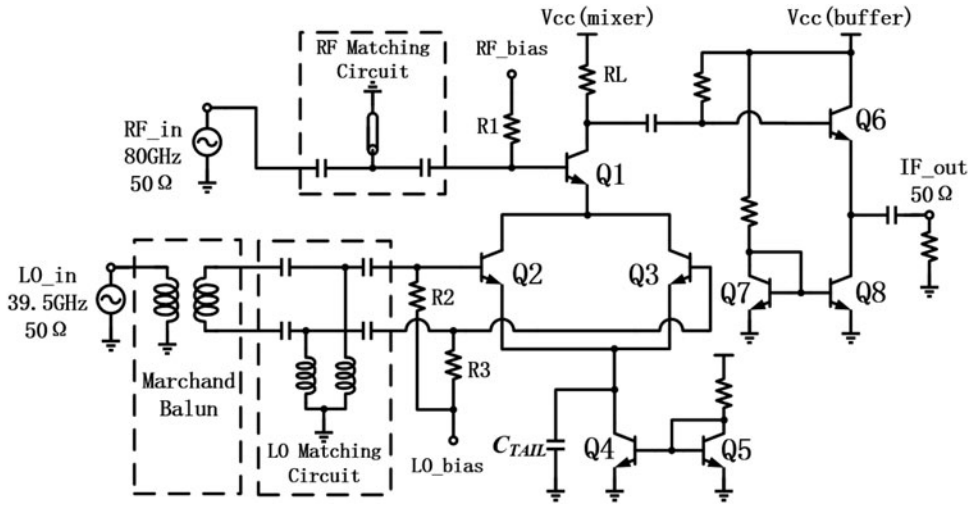

Fig. 7. Schematic of the improved bottom-LO-configured CECCTP SHM IC with tail current source.

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Fig. 8(b), the microstrip line consists of a signal line using the top metal (M6) and a ground plane using the bottom metal (M1). The M1 and M6 are separated by a 10-μm thick dielectric material. The ground plane includes some square slots to meet the design rule. Since the line width, line space and balun size have large influence on the balun performance, the Marchand balun is simulated and analyzed by electro-magnetic solver, Momentum. Consequently, the line width and space are 6 and 3 μm, respectively, as depicted in Fig. 8(b). The balun size is 270×120 μm^2 as shown in Fig. 8(a).

Figure 9 shows the simulated dependence of the conversion power gain of both SHM ICs on the LO power. The frequencies of RF, LO, and IF signals are 80, 39.5, and 1 GHz, respectively. The RF power is fixed to −40 dBm, and LO power (P_{LO}) is swept from −20 to 10 dBm. The improved SHM in Fig. 7 has a conversion power gain of 6.9 dB (including the buffer gain) at $P_{LO} = -7$ dBm. The core circuit of the improved SHM (without the buffer) consumes a DC current of 0.64 mA at a supply voltage of 3.3 V. The conventional SHM in Fig. 6 requires $P_{LO} = -1.5$ dBm to have similar conversion power gain of 6.7 dB (including the buffer gain). The core of the conventional SHM (without the buffer) consumes a DC current of 0.27 mA at a supply voltage of 2.5 V. The dependence of the conversion gain on the LO power is similar to that of 2^*f_{LO} in I_{out} shown in Fig. 5. In the top-LO-configured SHM, since the RF stage is the emitter degeneration for LO stage and the generation of 2^*f_{LO} is critically suppressed, the conversion gain is lower than that of the bottom-LO-configured SHM with P_{LO} lower than −2 dBm. In the bottom-LO-configured SHM, since the LO stage becomes the emitter degeneration for RF stage and the transconductance of RF stage is limited, the conversion gain is lower

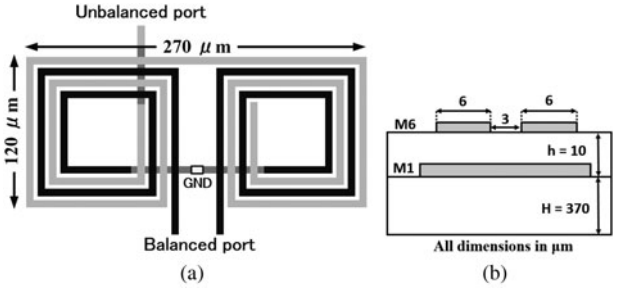

Fig. 8. (a) Top view and (b) side view of the Marchand balun IC.

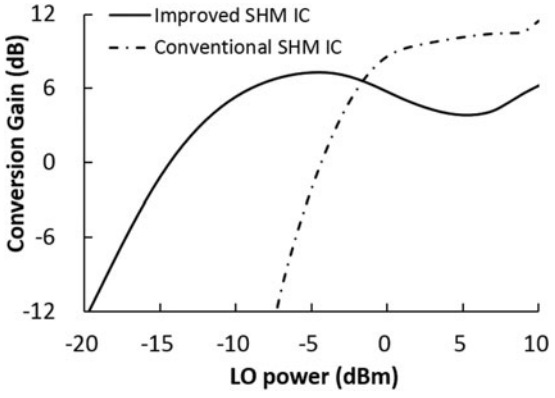

Fig. 9. Simulated dependence of the conversion gain on LO power.

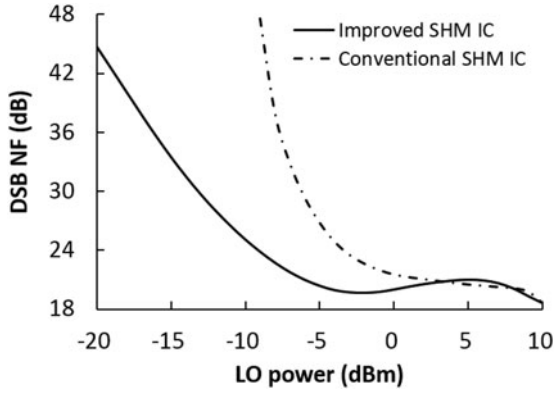

Fig. 10. Simulated dependence of the DSB NF on LO power.

than that of the top-LO-configured SHM with P_{LO} higher than −2 dBm. As shown in Fig. 9, the conversion gain of the improved SHM is higher and less sensitive to the variation of P_{LO} than that of the conventional one under P_{LO} less than −2 dBm.

Figure 10 shows the simulated double side band noise figure (DSB NF) of both SHM ICs with sweeping the LO power from −20 to 10 dBm. The frequencies of RF, LO, and IF signals are 80, 39.5 and 1 GHz, respectively. When P_{LO} is lower than 0 dBm, the DSB NF of the improved SHM is much lower than that of the conventional SHM.

The small signal noise analysis in GoldenGate is applied to simulate the noise level and the noise contribution of all the devices in the conventional and improved SHMs. Table 1 summarizes the simulated main noise contributors. The conventional and improved SHMs have the same conditions for simulation: $f_{RF} = 80$ GHz, $f_{LO} = 39.5$ GHz, $f_{IF} = 1$ GHz, and $P_{RF} = -40$ dBm. Since the optimal P_{LO} is different between the two SHMs, $P_{LO} = -1.5$ dBm is injected to the conventional SHM, while $P_{LO} = -7$ dBm is injected to the improved SHM, respectively. In the conventional SHM, the RF stage (HBT Q1) is the biggest noise contributor with 86.8% noise

Table 1. Summary and comparison of the noise contribution in the conventional and improved SHM ICs.

	Conventional SHM ($P_{LO} = -1.5$ dBm)		Improved SHM ($P_{LO} = -7$ dBm)	
Device	**Noise (10^{-18} V²/Hz)**	**Contribution (%)**	**Noise (10^{-18} V²/Hz)**	**Contribution (%)**
Noise from input DSB	1.7	–	2.0	–
Total added noise	294.1	100	292.6	100
Q1 (RF stage)	253.8	86.8	14.8	5.1
Q2 (LO stage)	0.6	0.2	98.5	33.7
Q3 (LO stage)	0.6	0.2	94.6	32.3
Q4 (tail current)	–	–	9.4	3.2
Q5 (tail current)	–	–	9.2	3.2
LO port (50 Ω)	<0.3	<0.1	11.1	3.8
LO Balun	<0.3	<0.1	24.4	8.3
RL (load)	4.4	1.5	6.2	2.1
R1 (RF bias)	26.2	8.9	2.1	0.7
R2 (LO bias)	<0.3	<0.1	5.4	1.9
R3 (LO bias)	<0.3	<0.1	4.8	1.6

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contribution. In the improved SHM, the LO stage (HBTs Q2 and Q3) becomes the biggest noise contributor with 66% noise contribution, while the RF stage has only 5.1% noise contribution.

The difference of the noise contribution is mainly caused by the difference of the operational principle. In the conventional SHM, the HBT Q1 (RF stage) enters the saturation region and increases the noise power. In addition, the noise of RF stage is amplified by the LO stage. Thus, the RF stage in the conventional SHM is the biggest noise contributor.

In the improved SHM, the LO stage generates the noise at the emitter of the HBT Q1 (RF stage). The noise from LO stage is amplified and converted to the noise at IF output by Q1. Thus, the LO stage in the improved SHM is the biggest noise contributor.

Since the noise coming from the tail current source (Q4 and Q5) is shunted by the C_{TAIL}, the tail current source has only 6.4% noise contribution. Figure 11 shows the dependence of conversion gain and DSB NF on the C_{TAIL} of the improved SHM. The conditions for the simulation are the same as those for the noise contribution simulation. As shown in Fig. 11, a large C_{TAIL} for AC ground is necessary to increase the conversion gain and decrease the DSB NF. Consequently, C_{TAIL} is chosen to 10 pF in the improved SHM circuit. The C_{TAIL} for AC ground decreases the common-mode rejection of the tail current source and might be a source of instability for a common-mode signal. It is confirmed that the SHM IC is stable from the transient simulation with sweeping LO power.

Figure 12 shows the simulated port-to-port isolation, including the 2LO–RF, LO–RF at the RF port, and the RF–IF, 2LO–IF, LO–IF at the IF port of the (a) conventional and (b) improved SHM ICs. The isolations are simulated as a function of LO frequency (f_{LO}). The f_{LO} is swept from 37.5 to 41.5 GHz and the f_{RF} is correspondingly changed from 76 to 84 GHz to keep the f_{IF} fixed to 1 GHz. Both two SHMs are applied with the RF power of −40 dBm. The conventional and improved SHMs are applied with the LO power of −1.5 and −7 dBm, respectively. Both SHMs have excellent LO–RF isolation as a result of the CECCTP structure of the LO stage and the balance of the balun.

Figure 13 shows the simulated input–output response of the conventional and improved SHM ICs. The frequency conditions for the simulation are: $f_{RF} = 80$ GHz, $f_{LO} = 39.5$ GHz, and $f_{IF} = 1$ GHz. The LO power of −1.5 and −7 dBm are injected to the conventional and improved SHMs, respectively. The IP1 dB and OP1 dB of the conventional SHM are −27.0 and −21.5 dBm. The IP1 dB and OP1 dB of the improved SHM are −23.0 and −17.0 dBm. In the conventional SHM, since the RF stage enters the saturation region

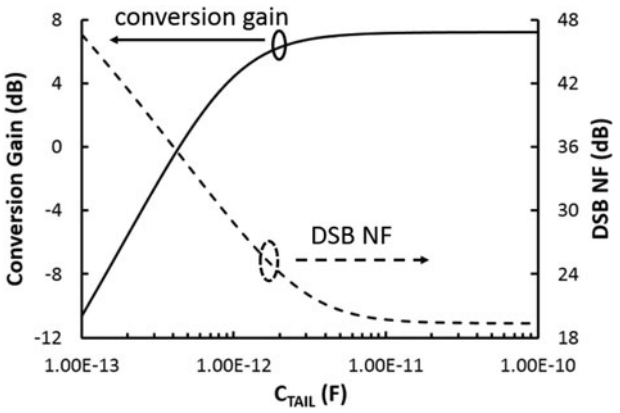

Fig. 11. Simulated conversion gain and DSB NF of the improved SHM versus C_{TAIL}.

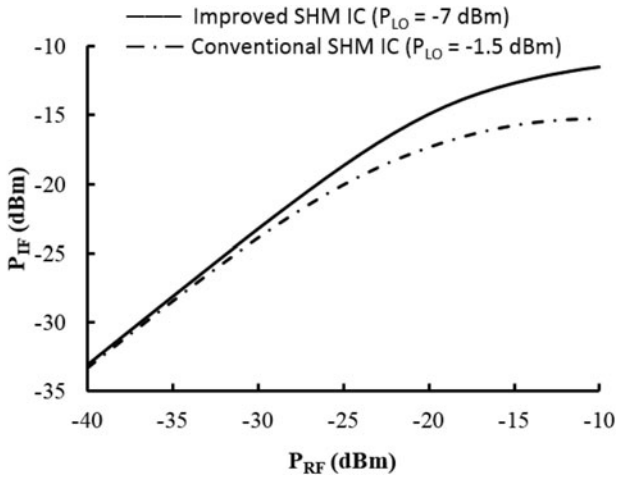

Fig. 13. Simulated IF output power versus RF input power.

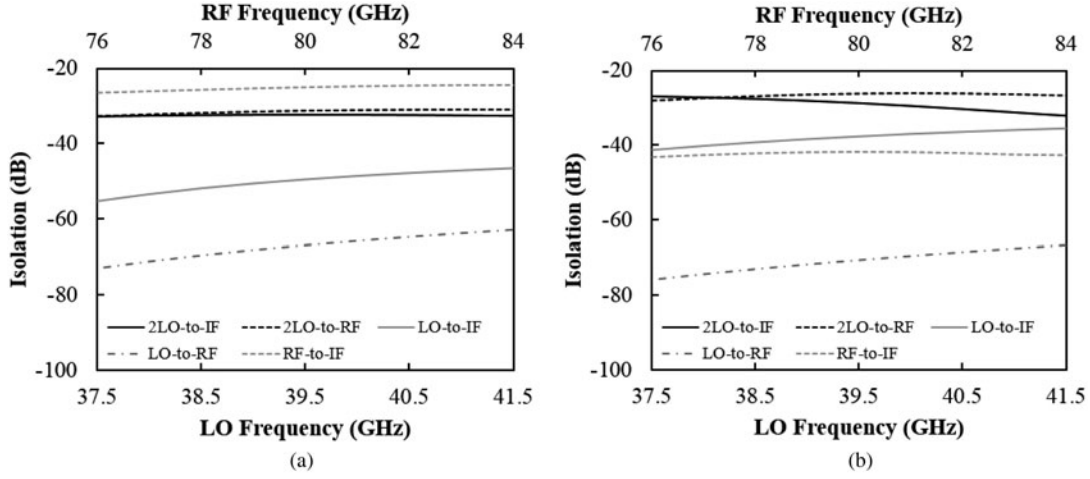

Fig. 12. Simulated isolation of the (a) conventional SHM and (b) improved SHM versus LO and RF frequency ($f_{IF} = 1$ GHz).

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as shown in Fig. 3, the voltage swing of the IF signal is suppressed. Thus, the IP1 dB of conventional SHM is lower than that of the improved one.

Figure 14 shows the simulated conversion gain of the conventional and improved SHMs as a function of the RF frequency. The f_{LO} is swept from 37.5 to 41.5 GHz and the f_{RF} is correspondingly changed from 76 to 84 GHz to keep the f_{IF} fixed to 1 GHz. The conventional and improved SHMs are applied with an LO power of −1.5 and −7 dBm, respectively.

IV. MEASUREMENT RESULTS

A) Measured results of the Marchand balun

To confirm the performance of the Marchand balun, a balun IC is individually fabricated in 130-nm SiGe BiCMOS technology. Figure 15(a) shows the die photograph of the balun IC and the core size is only 270×120 μm². Figure 15(b) shows the measured insertion loss performance. From 26 to 66 GHz, the balun IC exhibits measured insertion loss of <3 dB. Figure 15(c) illustrates the measured imbalance performance. From 20 to 66 GHz, the amplitude imbalance is <0.9 dB and the phase imbalance is <2.5°.

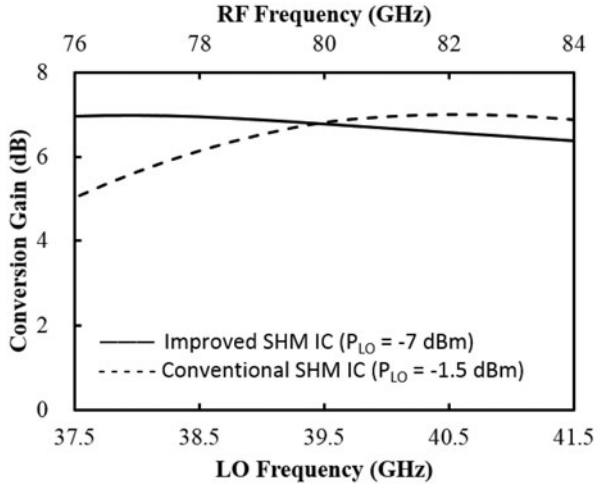

Fig. 14. Simulated conversion gain versus RF frequency.

B) Measured results of the SHM ICs

Figure 16 shows the die photograph of the bottom-LO-configured CECCTP SHM IC with a tail current source presented in this paper, which has a core size of 550 by 460 μm. In addition, the conventional top-LO-configured CECCTP SHM IC is fabricated for comparison.

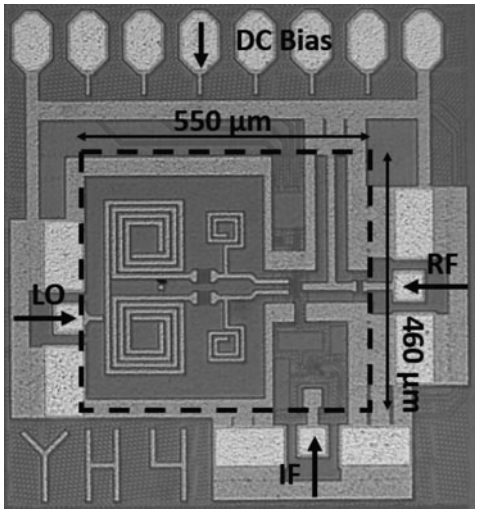

Fig. 16. Die photograph of the improved bottom-LO-configured SHM IC with tail current source.

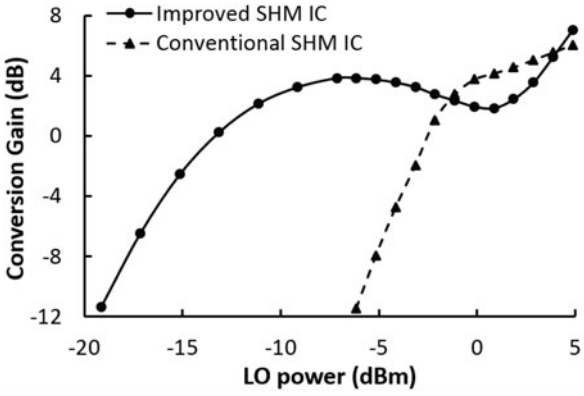

Fig. 17. Measured dependence of the conversion gain on the LO power (conditions: f_{RF} = 80 GHz, f_{LO} = 39.5 GHz, f_{IF} = 1 GHz).

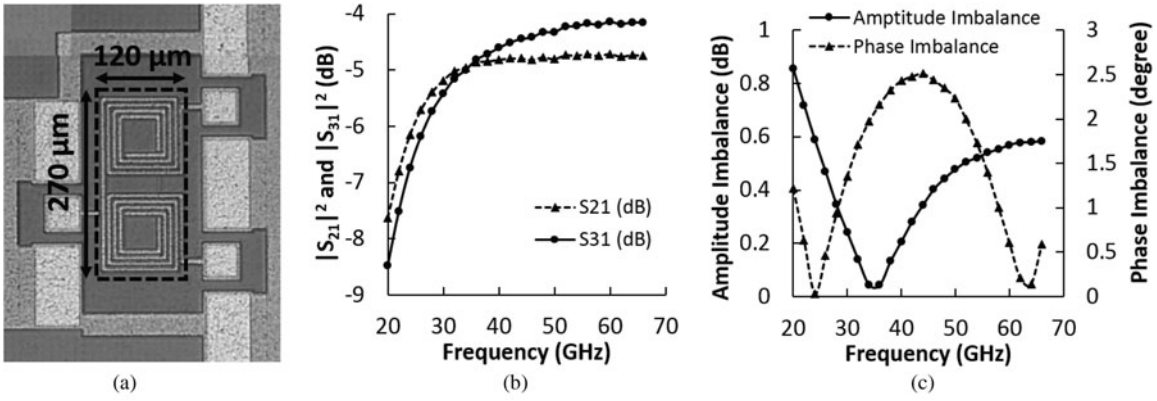

Fig. 15. (a) Die photograph of the Marchand balun IC, (b) measured insertion loss, (c) measured amplitude and phase imbalance.

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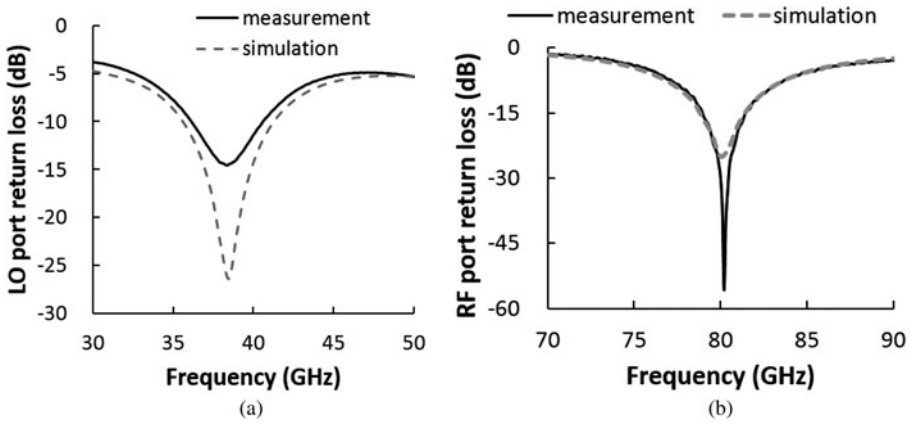

Fig. 18. Measured and simulated input return loss of the (a) LO port and (b) RF port of the improved SHM IC.

Figure 17 shows the measured dependence of the conversion power gain of the improved and conventional SHM ICs on the LO power. The measurement was carried-out on-wafer with single-ended 50-Ω system. At an RF frequency of 80 GHz and an LO frequency of 39.5 GHz (IF output frequency is 1 GHz), the improved SHM IC achieves a conversion power gain of 3.9 dB and a DC power consumption of 2.2 mW at an LO power of only −7 dBm. Considering the insertion loss of the balun as shown in Fig. 15(b), the actual input power is around −9 dBm. The conventional top-LO-configured one has a conversion power gain of 1.9 dB with a power consumption of 1.1 mW at an LO power of −1.5 dBm.

Figure 18 shows the simulated and measured input return loss at: (a) LO port and (b) RF port of the improved SHM IC with −7 dBm LO input power injected. The return loss of the LO port is better than 10 dB from 36.1 to 40.6 GHz. The return loss of the RF port is better than 10 dB from 78 to 82.7 GHz. The measured return losses well agree with the simulation.

Figure 19 depicts the simulated and measured IF frequency responses of the conversion gain of the improved SHM IC. RF frequency is fixed to 80 GHz and RF power is fixed to −37 dBm. LO input power is fixed to −7 dBm and LO frequency is swept from 39.95 to 39.25 GHz. Thus, IF frequency changes from 100 MHz to 1.5 GHz. When IF frequency is below 200 MHz, the conversion gain decreases with IF frequency decreasing because the capacitors are not large enough for DC block and AC ground. When the IF frequency is above 500 MHz, the conversion gain decreases with IF frequency increasing as a result of the frequency response of the buffer amplifier.

Figure 20 shows the simulated and measured input–output responses of the improved SHM IC with an LO power of −7 dBm at 39.5 GHz. The frequencies of RF and IF signals are 80 and 1 GHz, respectively. The measured IP1 dB and OP1 dB are −27 and −25 dBm, respectively.

Table 2 summarizes the measured performance of the fabricated CECCTP SHM ICs with previously published W-band SHM ICs. W-band SHM ICs utilizing the passive subharmonically pumped (SHP) diode topology require high LO power and suffer from the conversion loss. Compared with the active SHMs in [5, 15, 26], the LO-bottom-configured SHM IC presented in this paper has exhibited higher conversion gain with lower LO power and ultra-low power consumption.

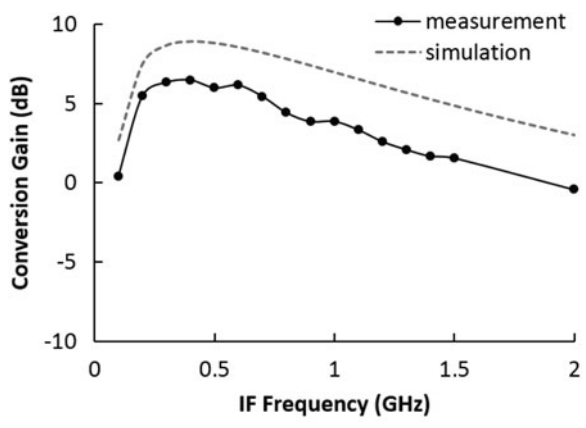

Fig. 19. Measured and simulated conversion gain versus IF frequency of the improved SHM IC (conditions: $f_{RF} = 80$ GHz, $f_{LO} = (f_{RF} - f_{IF})/2$, $P_{LO} = -7$ dBm).

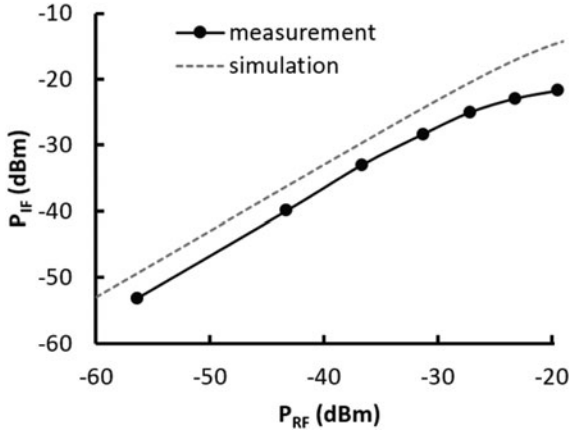

Fig. 20. Measured and simulated IF power versus RF power of the improved SHM IC (conditions: $f_{RF} = 80$ GHz, $f_{LO} = 39.5$ GHz, $f_{IF} = 1$ GHz, and $P_{LO} = -7$ dBm).

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Table 2. Summary and comparison of the W-band SHM ICs.

Ref	Process	f_{RF} (GHz)	P_{LO} (dBm)	Conversion gain (dB)	DC power (mW)	Chip size (um × um)	Topologies
[5]	0.8 μm SiGe BiCMOS	77	10	0.7*	22	0.9 × 0.86	Balanced SHM
[15]	90 nm CMOS	70	10	−1.5	58	0.61 × 0.58	Top-LO-leveled Gilbert-cell SHM
[22]	0.l μm InP HEMT	94	2	−9.5	0	2.35 × 1.1	Dual-FET resistive SHM
[23]	0.15 μm GaAs pHEMT	80	10	−10	0	1.5 × 2.0	SHP‡ diode mixer
[24]	0.15 μm GaAs pHEMT	77	7	−11	0	2.5 × 1	Anti-parallel Schottky diode pair SHM
[25]	0.15 μm GaAs pHEMT	89	11	−4.7	0	1 × 2	SHP HEMT gate mixer
[26]	1 um InP DHBT	83	6	1	N.A.	1.37 × 1.41	Active single HBT doubler & mixer
[27]	UMS BES Schottky diode	90	0	−13	N.A.	1.4 × 1.4	SHP diode mixer
[28]	Quasi-monolithic (GaAs Schottky diode)	90	10	−8	0	2.2 × 4.0	Anti-parallel Schottky diode pair SHM
This work	0.13 μm SiGe BiCMOS	80	−7†	3.9	2.2	0.55 × 0.46	Improved bottom-LO-configured SHM with tail current source
		80	−1.5†	1.9	1.1	0.55 × 0.46	Conventional top-LO-configured SHM

*Includes 11 dB gain of the IF buffer amplifier.
†Includes 2 dB insertion loss of the balun.
‡SHP, sub-harmonically pumped.

V. CONCLUSION

A bottom-LO-configured CECCTP SHM IC with a tail current source for W-band applications has been designed, fabricated, and tested using 130-nm SiGe BiCMOS technology. The SHM IC exhibits a conversion gain of 3.9 dB at 80 GHz with an LO power of only −7 dBm at 39.5 GHz. The DC power consumption of the SHM IC is only 2.2 mW. It is confirmed that the bottom-LO-configuration decreases the requirement of LO power and the tail current source makes the conversion gain insensitive to the variation of LO power. Therefore, the improved SHM topology significantly facilitates the design of oscillator and is suitable for W-band transceiver IC.

ACKNOWLEDGEMENT

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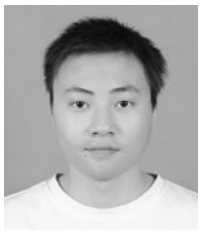

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