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Doherty power amplifier output networks with maximized bandwidth

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Abstract

A method is presented to optimize the combining network and the post-matching network of a Doherty power amplifier (DPA) for maximizing the bandwidth. For widely applicable results, RF power transistors are approximated in the large-signal regime using a simple analytical model with a few parameters. A definition of bandwidth of DPA is given, which involves gain and efficiency at full-power and 6 dB backoff. Different combining network topologies are compared in terms of this bandwidth definition. The element values are optimized using two factors, one to scale the combining node impedance and the other to scale the impedance seen by the transistors. For each optimized topology, explicit formulas are given resulting in the element values in terms of the optimized values and a few transistor parameters. The method presented also leads to a proper selection of the post-matching network.

Research Paper

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1. Introduction

Modern wireless communication systems use high peak to average power ratio (PAPR) signals to utilize spectrum efficiently with high data rates [1]. Such signals cause power amplifiers to operate with a reduced efficiency [2]. Doherty power amplifier (DPA), first proposed by Doherty [3] and well discussed in [4] provides an efficient amplification for signals having high PAPR.

There has been a lot of work on increasing the efficiency of the DPA or increasing the frequency range where the DPA is efficient. Efficiency optimizations can be achieved in narrowband applications, but in broadband applications, it is not trivial to achieve similar performance. Using more efficient amplifier modes such as class-E or class-F enables efficient operation controlling harmonic terminations in backoff of narrowband applications [5, 6]. In [7] tuned load and class-F are compared at the output of the DPA using benefits of GaN-HEMT transistors. There are also asymmetrical DPA approaches [8] where the backoff peaking is set to 8.0–9.9 dB.

When it comes to building a wideband DPA, there are several limitation factors which are summarized and categorized in [9]. The most notable ones are the device output capacitance and the frequency response limitation of λ/4 impedance inverters. In [10], a DPA is built over the frequency range of 1.7–2.3 GHz, focusing more on the device output capacitance and not considering λ/4 impedance inverter's limitation. Parasitic compensation techniques are used to achieve 49% [11] and 87% [12] fractional bandwidths (FBW). Digitally controlled dual-RF input DPAs are also another approach to increase the efficiency bandwidth compared to single input DPAs [13]. In [14], a 100% FBW digital DPA was presented based on Doherty-outphasing continuum and in [15], a 50% FBW digital three-way DPA with backoff reconfigurability is presented.

Frequency analysis of the DPA is extensively investigated in [16] exploiting the bottleneck on the limitation of impedance inverter's frequency response. By modifying the impedance transformation ratio of transmission lines, the impedance seen by the carrier amplifier has less variation over the frequency and the efficiency bandwidth is increased up to an octave [17]. The impedance inverter's limitation is more dominant if the device output capacitance is small, such as in GaN devices, with which FBW = 25% is achieved by a modified load modulation network [18]. Adoption of broadband post matching networks instead of quarter-wave inverters are proposed to achieve FBW of 43% [19], 53% [20], and 70.7% [21].

The use of a two-section matching circuit at the peaking amplifier enhances the efficiency bandwidth [22]. It is also possible to achieve wide bandwidth with LDMOS transistor using two section transmission line matching where [23] presents 52% FBW with 280W output power. In [24] a closed-form design technique is presented on how to implement input, output splitting/combining networks and demonstrating 83% FBW. Biasing transistors with a constant current source rather than a voltage source results in FBW of 93.3% [25].

In this paper, we determine the topology and element values of optimized output network of a DPA, for the purpose of maximizing the bandwidth. Instead of using specific and complex vendor models of transistors, we use a simple generic and robust transistor model to make the

results more general. In section "Theory", we introduce our analytical transistor model that is used in approximating the behavior of any RF power amplifier including DPA. We divide the output network into two parts: a combining network and a post-matching network. We present different combining network topologies in section "Output network" and introduce two factors for the purpose of bandwidth optimization. Section "Optimized combining networks" introduces the definition of bandwidth of the DPA dependent both on gain and efficiency at full-power and 6 dB backoff. There, we provide explicit formulas for the bandwidth maximized values of combining network element values that are dependent on the optimized factors and the transistor parameters. A post-matching network not causing a bandwidth reduction can be selected subsequently. In section "Example designs", we give examples to demonstrate the use of the method, where all element values are calculated using the presented formulas. The resultant output networks are also analyzed using a harmonic balance simulator using vendor models of transistors to show that the results are close enough. The values can be used as a good starting point for further optimization using harmonic balance with more accurate models of transistors. Section "Experimental results" presents experimental results verifying the validity of the method.

2. Theory

2.1 Large-signal intrinsic RF transistor model

The drain current of the RF transistor is assumed to depend linearly on the gate voltage, v_{GS}, minus the threshold voltage, V_T, through the transconductance of G_m. We note that this is a good approximation for the popular GaN transistors. We write the instantaneous intrinsic drain current, i_D, in terms of the drain to source voltage, v_{DS}, as

$$i_D = \begin{cases} G_m(v_{GS} - V_T) f(v_{DS}) & \text{if} v_{GS} \geq V_T \\ 0 & \text{otherwise} \end{cases} \quad (1)$$

with

$$f(v_{DS}) = 1 - \frac{1}{2}\left(1 - \frac{v_{DS}}{V_{DD}}\right)^{N_e} - \frac{1}{2}\left(1 - \frac{v_{DS}}{V_{DD}}\right)^{N_e+1} \quad (2)$$

where $f()$ is continuous function for all v_{DS} values and N_e is an even integer showing the order of knee function approximation. The resultant $I-V$ characteristics of our model is shown in Fig. 1 for N_e=14.

This function is an improved version of that introduced recently [26]. Unlike the model there, our transistor characteristics are never in the fourth quadrant and hence it always remains a passive device. Therefore, our model is usable for transistors under any class of operation experiencing any complex or negative real-part loads. This is especially important for DPA analysis since the individual transistors of a DPA may experience very high-Q or even negative real-part loads under certain conditions. It is found that harmonic balance simulation of DPA using vendor models of transistors causes convergence problems under certain combining network combinations making an optimization very difficult.

The knee voltage, V_K, is defined as the point where the the slope of $f(v_{DS})$ with respect to v_{DS}/V_{DD} is unity. For a given V_K and V_{DD}, the most appropriate even integer, N_e, can be determined from the solution of

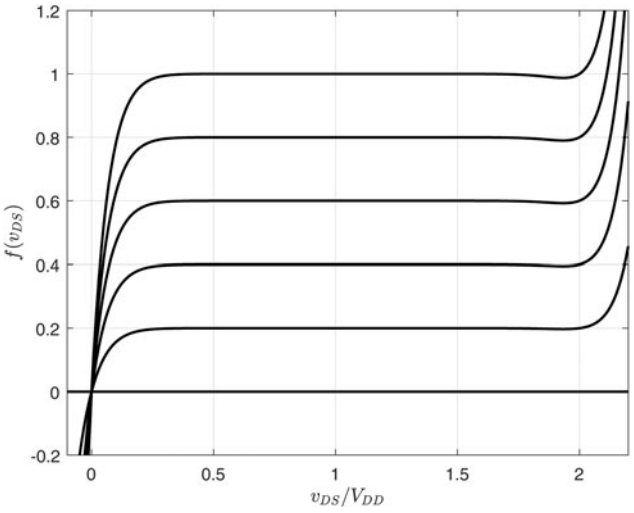

Fig. 1. *I-V* characteristics of our model with N_e = 14.

$$N_e\left(1 - \frac{V_K}{V_{DD}}\right)^{N_e-1} + (N_e+1)\left(1 - \frac{V_K}{V_{DD}}\right)^{N_e} = 2 \quad (3)$$

2.2 Analysis of a simple RF power amplifier using the model

The analysis method can be explained using an RF power amplifier shown in Fig. 2. The transistor is assumed to have a voltage-independent drain capacitance of C and a series package inductance of L_s. The amplifier operates with a supply voltage of V_{DD}.

The transistor input is excited with a sinusoidal signal at ω shifted with a bias voltage V_B. To simplify the analysis, we assume that all harmonic voltages are shorted at the intrinsic transistor drain. This is a good approximation if the package inductance L_s is small and the inductance, L, forms a resonant circuit at fundamental frequency shorting the harmonics. Hence the drain voltage is assumed to be purely sinusoidal, and we can write v_{DS} as:

$$v_{DS}(\theta) = V_{DD} + V_1 \cos(\theta + \phi) \quad (4)$$

An input voltage of $v_{GS} = V_B + V_{in}\cos\theta$ results in a drain current of

$$i_D = A(\theta)\left[1 - \frac{1}{2}\left(\frac{V_1}{V_{DD}}\right)^{N_e} \cos^{N_e}(\theta+\phi) + \frac{1}{2}\left(\frac{V_1}{V_{DD}}\right)^{N_e+1} \cos^{N_e+1}(\theta+\phi)\right] \quad (5)$$

with

$$A(\theta) = \begin{cases} G_m(V_{in}\cos\theta + V_B - V_T) & \text{if } \cos\theta > -\frac{V_B - V_T}{V_{in}} \\ 0 & \text{otherwise} \end{cases} \quad (6)$$

Following the approach of [26], we expand (5) as the product of an infinite series with a finite series. Hence one can obtain the DC current, I_0, and the fundamental current, $\mathbf{I}_1$ (in the phasor form), both as a finite series. Note that I_0 and $\mathbf{I}_1$ depend on N_e,

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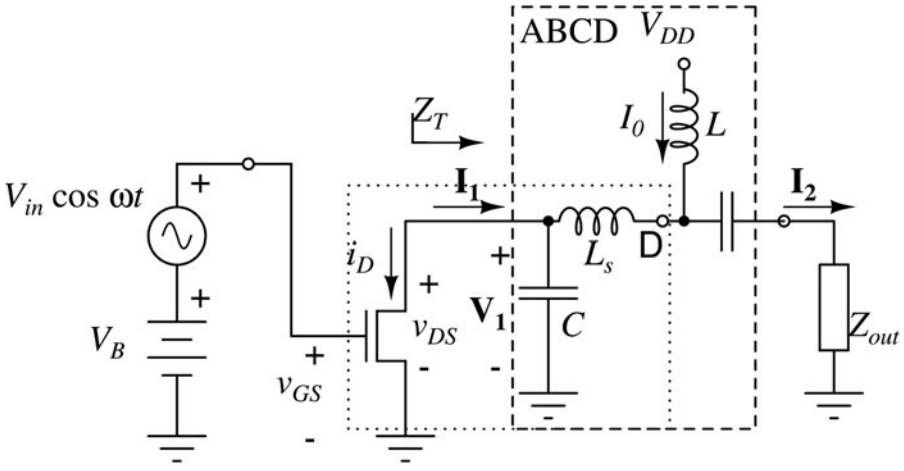

Fig. 2. Schematic of an RF power amplifier.

V_{in}, $V_B - V_T$, and the phasor $\mathbf{V}_1 = V_1 e^{j\phi}$, in a nonlinear manner through the functions f_1 and f_2 defined as

$$\begin{aligned} I_0 &= f_1(N, V_{in}, V_B - V_T, \mathbf{V_1}) \\ &= A_0 k_0 + \frac{1}{2}\sum_{n=1}^{N_e+1} A_n k_{n,R} \\ \mathbf{I_1} &= f_2(N, V_{in}, V_B - V_T, \mathbf{V_1}) \\ &= A_1 k_0 + \frac{1}{2} A_0 k_{1,R} + \frac{1}{2}\sum_{n=1}^{N_e+1}\big[(A_{n-1} + A_{n+1})k_{n,R} \end{aligned} \tag{7}$$

$$+ j(A_{n-1} - A_{n+1})k_{n,Q})\big] \tag{8}$$

where A_n, $k_{n,R}$, and $k_{n,Q}$ are defined in Appendix A. We should also satisfy $\mathbf{V_1} = Z_T \mathbf{I_1}$ or

$$\mathbf{V_1} = Z_T f_2(N, V_{in}, V_B - V_T, \mathbf{V_1}) \tag{9}$$

where $Z_T = \mathbf{V_1}/\mathbf{I_1}$ is the drain impedance seen by the transistor. This value is easily found as a function of ω in terms of Z_{out} and ABDC parameters of the network composed of C, L_s, and L.

$$Z_T = \frac{AZ_{out} + B}{CZ_{out} + D} \tag{10}$$

With a given ω, N, V_{DD}, V_{in}, and $V_B - V_T$, we solve[1] the nonlinear equation of (9) to find $\mathbf{V_1}$. Once the complex valued quantity, $\mathbf{V_1}$, is found, we can determine I_0 from (7), and the output RF power, P_{out}, using

$$P_{out} = \frac{1}{2}\mathcal{R}e\{Z_{out}\}|\mathbf{I_2}|^2 \text{ with } \mathbf{I_2} = \frac{\mathbf{V_1}}{\mathrm{AZ_{out}} + \mathrm{B}} \tag{11}$$

The efficiency is determined from

$$\eta = \frac{P_{out}}{I_0 V_{DD}} \tag{12}$$

[1]We use *fsolve* function of MATLAB. All MATLAB codes used in this paper are available as Supplementary material.

2.3 RF power amplifier examples

As the active device we choose Cree CGH40010 GaN transistor to build a power amplifier with $V_{DD} = 28$ V. We model the transistor using the parameters $G_m = 0.66$ A/V, $V_T = -3.3$ V, $C = 1.84$ pF and $L_s = 0.26$ nH, and $N_e = 14$. Here, G_m and V_T are determined from the transistor's I-V characteristics. C and L_s are estimated from the vendor specified optimal load impedance. N_e is found from the knee voltage using (3).

We first bias the transistor in Class-B ($V_B = V_T$) and choose $L = \infty$. Figure 3 shows the calculated power and efficiency load-pull contours using our model at 2.5 GHz as Z_{out} is varied. The full-power load-pull contours are generated with an input drive level to reach the rated power at the corresponding optimum load. At the same load, we reduce the input power to reach a 6 dB lower output power to define the 6 dB back-off (BO) level. Then the load-pull contours are regenerated at this BO level.

We repeated the load-pull simulation (Fig. 4) for the same amplifier with transistor biased as Class-C. It is excited with twice the input RF voltage to obtain the same output power with a properly selected gate bias voltage.

The maximum power is achieved nearly at the same impedance value as the Class-B amplifier. As BO is increased the optimal values move toward higher impedances more rapidly compared to Class-B amplifier.

To verify the accuracy of our model, we present comparison of our results for Class-B and Class-C amplifiers with harmonic balance simulation[2] at 2.5 GHz using vendor supplied nonlinear model in Table 1. The results of our model are reasonably close to the results of more accurate vendor model.

Table 2 lists our model's optimal load impedance, Z_{opt}, defined at the drain pin (D in Fig. 2) of the transistor package for different frequencies. With a suitable value of shunt inductance (L of Fig. 2), it is possible to move the center of load-pull contours to the real axis to find the optimal load resistance, R_{opt}, which is also defined at the drain pin of the transistor. At low frequencies, R_{opt} is equal to the optimal load resistance (26.6 Ω) of the intrinsic transistor, since the effects of the drain capacitance, C and the package inductance, L_s, are negligible.

Note that this simple model of the transistor can be scaled by a factor ξ to wider gate width transistors of the same family: For a

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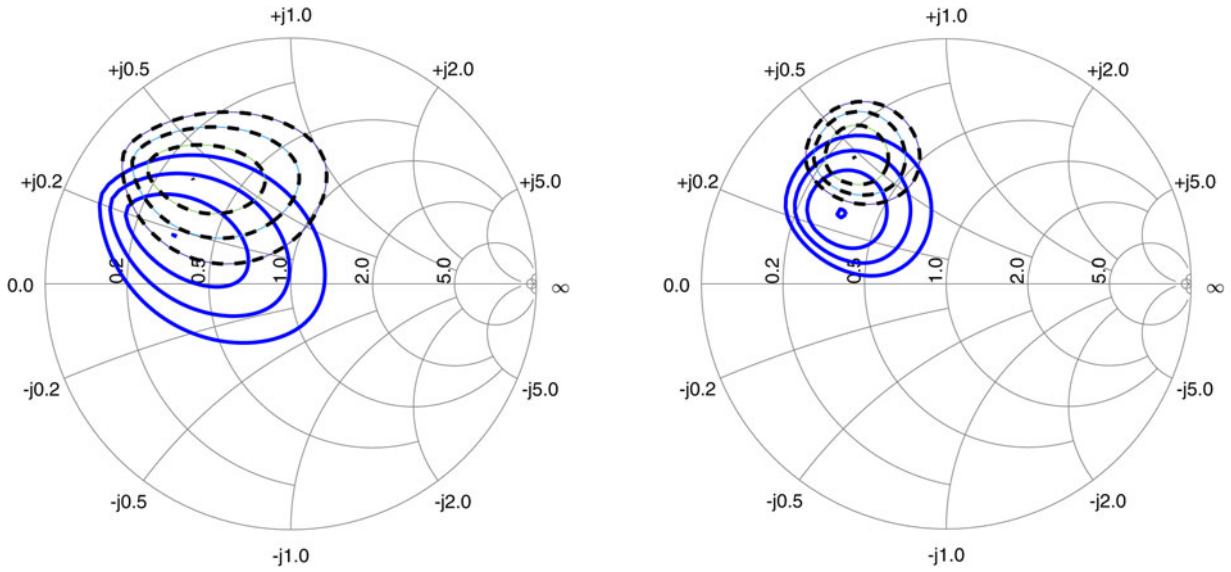

Fig. 3. Power (left, in 1 dB steps) and efficiency (right, in 5% steps) load-pull contours of Class-B transistor at 2.5 GHz on 50 Ω Smith charts at two-input levels: full-power (solid) and 6 dB BO (dashed).

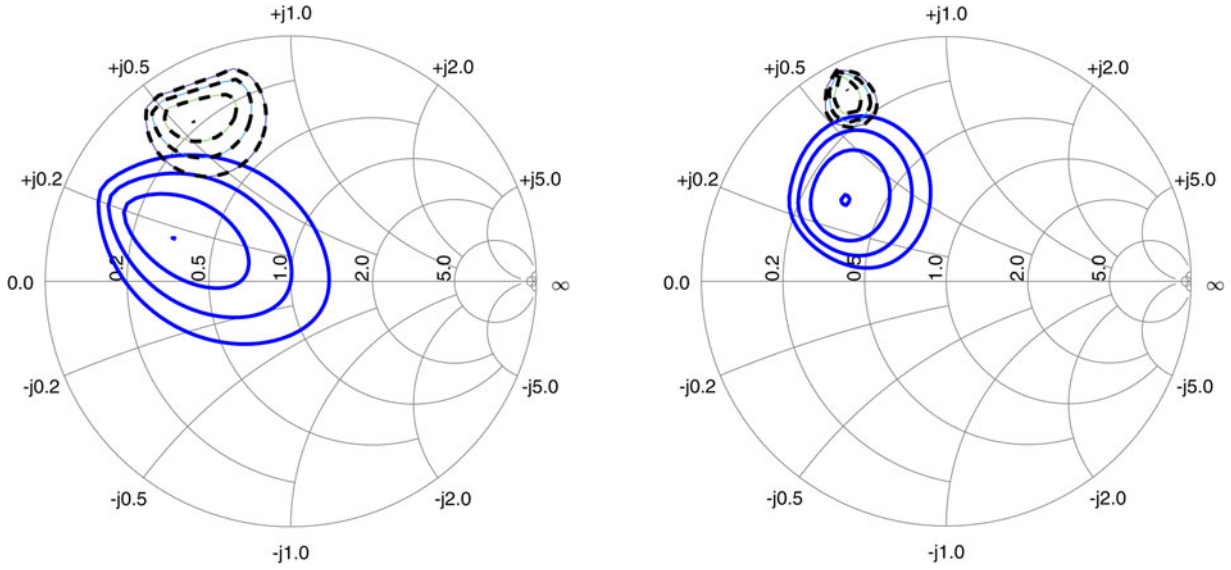

Fig. 4. Figure 3 repeated for Class C transistor at full-power (solid) and at 5 dB BO (dashed) rather than at 6 dB BO.

transistor with ξ times gate width[3], the parameters above become ξG_m, ξC, L_s/ξ, L/ξ, R_{opt}/ξ, Z_{out}/ξ, while V_T and η remain unchanged. Hence the load pull contours of Figs 3 and 4 are applicable if the reference impedance of the Smith chart is set to $(50/\xi)$ ~Ω. For example, for CGH40025 and CGH40045 power transistors, we need to set $\xi = 2.5$ and 4.5, respectively.

2.4 Analysis of Doherty power amplifier

We consider the generic DPA shown in Fig. 5 composed of carrier and peaking amplifiers, using the Class-B and Class-C amplifiers identical to those described in the previous section.

The desired combining node impedance of Z_L is obtained using a post-matching network of sufficient bandwidth. The carrier transistor is biased as Class-B ($V_{Bc} = V_T$), while the peaking transistor is biased as Class-C with V_{Bp}. The combining network with two branches should provide the desired impedances to the transistor drains. When both transistors are driven at full-power, the impedances presented to both drains should nearly[4] be equal to R_{opt}. At 6 dB BO, the peaking transistor is off. Its output capacitance, C, should be tuned out at the center frequency to prevent loading to the combining node. At the same BO level, the combining network should present a load of $2R_{opt}$ to the carrier transistor drain, to achieve the desired high efficiency. For an

[3]The number of drain bond wires and the drain capacitance is nearly proportional to the gate width.

[4]The optimal load values for a Class-C transistor is slightly different for the same full-power. For simplicity, we will assume them to be equal to that of Class-B amplifier.

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Table 1. Comparison of harmonic balance and our model for Class-B and Class-C amplifiers at full-power (FP) and 6 dB output BO

	Harm. balance			Our model		
	Z_{out} (Ω)	P_{out} (dBm)	η	Z_{out} (Ω)	P_{out} (dBm)	η
CGH40010 Class-B at 2.5 GHz (V_{Bc} = −3.3 V)						
Maximum power						
FP	16 + j12	40.8	66	16.9 + j8.9	40.6	67
BO	16 + j19	36.8	61	15.9 + j20.2	37.6	68
Maximum efficiency						
FP	16 + j18	40.2	71	17.3 + j14	40.1	72
BO	14 + j22	36.1	64	13.6 + j23.4	37.2	72
CGH40010 Class-C at 2.5 GHz (V_{Bp} = −5.6 V)						
Maximum power						
FP	14 + j13	41	72	16.8 + j7.9	40.6	76
Maximum efficiency						
FP	16 + j19	40.4	80	16.9 + j15.3	39.7	81

Table 2. Optimal load impedance (Z_{opt}), and load resistance (R_{opt}, used with a shunt tuning inductor, L) for CGH40010 GaN transistor at full-power

f_0 (GHz)	Z_{opt} (Ω)	L (nH)	R_{opt} (Ω)
≪ 1.0	26.6	≫15	26.6
1.0	24.5+j5.75	15	25.9
1.5	21.8+j6.52	6.0	24.5
2.0	18.9+j8.47	3.3	23.0
2.5	16.9+j8.87	2.05	21.1
3.0	14.3+j7.86	1.35	18.7
3.5	12.3+j6.95	0.935	16.4

efficiency peak at 6 dB BO, we set $\beta = 2\alpha$, where α and β are the input power divider ratios as indicated in Fig. 5. For a lossless divider we have $\alpha^2 + \beta^2 = 1$ and hence $\alpha = 1/\sqrt{5}$, $\beta = 2/\sqrt{5}$. We introduce a proper phase shift at the input of the carrier amplifier to equalize the phases at the combining node.

Referring to Fig. 5, the output loads of transistors including their parasitic capacitances and matching networks can be represented as a function of ω with ABCD parameters having complex entries. The combining node is terminated with the impedance Z_L having a voltage phasor of $\mathbf{V_L}$ at ω.

Let the carrier and peaking transistors' voltage and current phasors at ω be denoted by $\mathbf{V}_c$, $\mathbf{I}_c$, $\mathbf{V}_p$, and $\mathbf{I}_p$, respectively. From ABCD matrices shown in Fig. 5, we have:

$$\mathbf{V_c} = A_c\mathbf{V_L} + B_c\mathbf{I_{Lc}} \tag{13}$$

$$\mathbf{I_c} = C_c\mathbf{V_L} + D_c\mathbf{I_{Lc}} \tag{14}$$

$$\mathbf{V_p} = A_p\mathbf{V_L} + B_p\mathbf{I_{Lp}} \tag{15}$$

$$\mathbf{I_p} = C_p\mathbf{V_L} + D_p\mathbf{I_{Lp}} \tag{16}$$

The voltage at the combining node is given by

$$\mathbf{V_L} = (\mathbf{I_{Lc}} + \mathbf{I_{Lp}})Z_L \tag{17}$$

Substituting equation (17) in equations (14), (16) and solving for $\mathbf{I}_{Lc}$ and $\mathbf{I}_{Lp}$, we rewrite equation (17) as

$$\mathbf{V_L} = Z_L\frac{D_p\mathbf{I_c} + D_c\mathbf{I_p}}{D_cD_p + (C_cD_p + C_pD_c)Z_L} \tag{18}$$

Substituting $\mathbf{I_{Lc}}$, $\mathbf{I_{Lp}}$ and equation (18) into equations (13) and (15), we get

$$\begin{aligned}\mathbf{V_c} &= \frac{B_cD_p + (A_cD_p + B_cC_p)Z_L}{D_cD_p + (C_cD_p + C_pD_c)Z_L}\mathbf{I_c} \\ &\quad + \frac{(A_cD_c - B_cC_c)Z_L}{D_cD_p + (C_cD_p + C_pD_c)Z_L}\mathbf{I_p} \triangleq Z_c\mathbf{I_c} \qquad (19)\\ \mathbf{V_p} &= \frac{B_pD_c + (A_pD_c + B_pC_c)Z_L}{D_cD_p + (C_cD_p + C_pD_c)Z_L}\mathbf{I_p}\end{aligned}$$

$$+ \frac{(A_pD_p - B_pC_p)Z_L}{D_cD_p + (C_cD_p + C_pD_c)Z_L}\mathbf{I_c} \triangleq Z_p\mathbf{I_p} \tag{20}$$

where Z_c and Z_p are defined as the impedances seen by each transistor.

As in the case of stand-alone amplifier, we can write $\mathbf{I}_c$ and $\mathbf{I}_p$ as the fundamental component of clipped cosine waves:

$$\mathbf{I_c} = f_2(N, \alpha V_{in}, V_{Bc} - V_T, \mathbf{V_c}) \tag{21}$$

$$\mathbf{I_p} = f_2(N, \beta V_{in}, V_{Bp} - V_T, \mathbf{V_p}) \tag{22}$$

Substituting equations 21 and 22 into equations 19 and 20, we get two nonlinear equations with two unknowns: $\mathbf{V}_c$ and $\mathbf{V}_p$. These equations can be solved simultaneously to find the unknown values. We can then proceed to find the supply currents of carrier (I_{0c}) and peaking (I_{0p}) amplifiers from

$$I_{0c} = f_1(N, \alpha V_{in}, V_{Bc} - V_T, \mathbf{V_c}) \tag{23}$$

$$I_{0p} = f_1(N, \beta V_{in}, V_{Bp} - V_T, \mathbf{V_p}) \tag{24}$$

The phasor at the combining node, $\mathbf{V}_L$, is found using equations (18), (21), and (22). Hence the output power is written as

$$P_{out} = \frac{1}{2}\mathcal{R}e\left\{\frac{|\mathbf{V_L}|^2}{Z_L}\right\} \tag{25}$$

and the efficiency can be found from

$$\eta = \frac{P_{out}}{V_{DD}(I_{0c} + I_{0p})} \tag{26}$$

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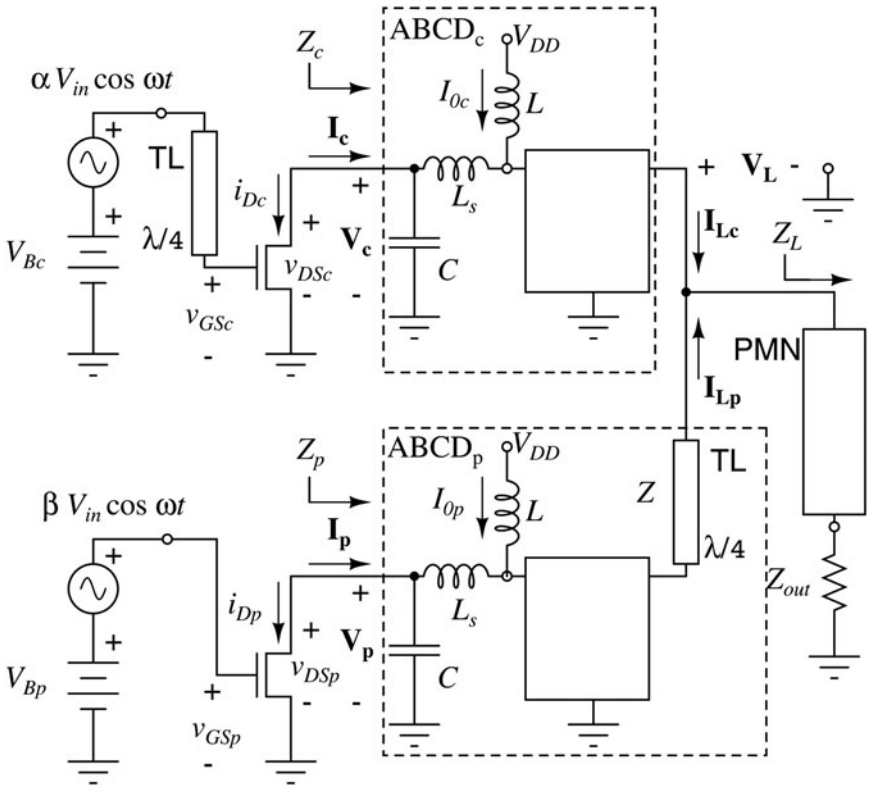

Fig. 5. Schematic of the generic DPA.

3. Output network

The output network plays a crucial role in the performance of the DPA [16]. We divide the output network into two parts: A combining network (CN) which combines the outputs of both amplifiers and a post-matching network (PMN), which transforms the combining node impedance to the load impedance. In this section, we present different CN and PMN topologies.

3.1 Combining network (CN)

We introduce two factors for the purpose of bandwidth optimization. Using the first factor, ζ, we set the combining node impedance at center frequency, ω_0, as

$$Z_L(\omega_0) = \zeta \frac{R_{opt}}{2} \tag{27}$$

Using the second factor, κ, we set Z_c and Z_p at full-drive as

$$Z_c(\omega_0) = Z_p(\omega_0) = \kappa R_{opt} \tag{28}$$

and at 6 dB BO (Z_{cBO}) as

$$Z_{cBO}(\omega_0) = 2\kappa R_{opt} \tag{29}$$

At the center frequency and full-power, the impedance transformation circuits at the output of both transistors should transform $Z_c(\omega_0) = Z_p(\omega_0) = \kappa R_{opt}$ to $2Z_L$ so that when they are connected in parallel at the combining node it becomes Z_L. This corresponds to a transformation ratio of ζ/κ. At 6 dB BO, the carrier amplifier's impedance transformation circuit should transform $Z_{cBO}(\omega_0) = 2\kappa R_{opt}$ to Z_L, corresponding to a transformation ratio of $\zeta/4\kappa$.

With a selection of $\kappa < 1$, the small-signal gain and maximum power are reduced at the center frequency, while increasing the performance at band edges, contributing to the bandwidth enhancement. However, we will keep $0.84 < \kappa < 1.2$ to prevent a gain reduction of more than 1.5 dB and to preserve the linearity within acceptable limits.

3.1.1 Conventional CN

The conventional combining network is shown in Fig. 6.

The output capacitance, C, of each transistor is tuned out at the center frequency with a suitable shunt inductance, L, as given in Table 2, acting also like the drain bias RFC. If L turns out to be too small for practical realization, it can be replaced by a high impedance (Z_H) transmission line with a length x (in λ_0 units) of

$$x = \frac{1}{2\pi} \tan^{-1}\left(\frac{\omega_0 L}{Z_H}\right) \tag{30}$$

with a slight degradation in bandwidth performance.

Since the peaking transistor is connected directly to the combining node, it is not possible to optimize ζ and κ independently. To maintain the equal contribution of power at full-drive we must set

$$\zeta = \kappa \text{ and } Z = \zeta R_{opt} \tag{31}$$

Obviously, the delay compensation at the input side depicted in Fig. 5 must be swapped between transistors for proper operation.

3.1.2 CN type I

The CN [22, 24] shown in Fig. 7 achieves the desired characteristics using three quarter-wave transmission lines, which allows

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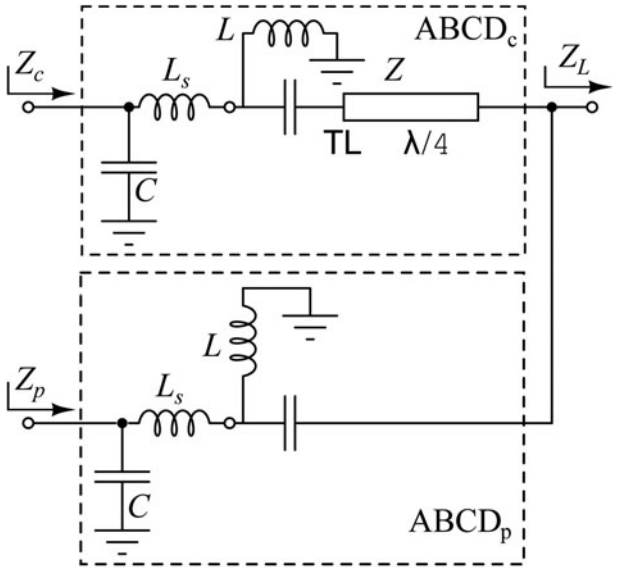

Fig. 6. Conventional combining network.

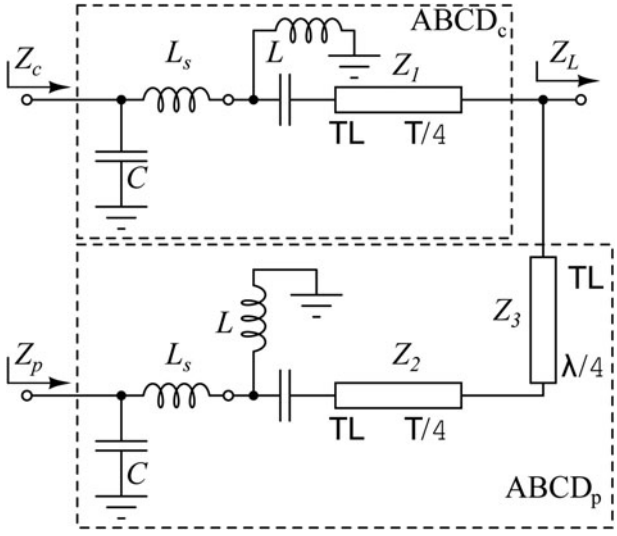

Fig. 7. CN I.

easy implementation, especially at high frequencies. Z_1 should transform $2Z_L = \zeta R_{opt}$ to κR_{opt} at full power and $Z_L = \zeta R_{opt}/2$ to $2\kappa R_{opt}$ at 6 dB BO. Similarly, Z_2 and Z_3 should transform ζR_{opt} to κR_{opt} at the full-drive level. When the peaking transistor is off, no loading is presented at the combining node at the center frequency since there is a shunt inductance, L, to tune-out the drain capacitance, C, at that frequency. Since C is tuned out only at the center frequency, its loading at other frequencies is one of the bandwidth limiting factors.

The transmission line impedances are given by

$$Z_1 = \sqrt{\kappa\zeta} R_{opt} \tag{32}$$

$$Z_2 = \kappa^{3/4}\zeta^{1/4} R_{opt} \quad Z_3 = \kappa^{1/4}\zeta^{3/4} R_{opt} \tag{33}$$

Note that both Z_2 and Z_3 contribute to transformation for a wider band operation.

3.1.3 CN type II

A wide-band combining network using lumped elements [19, 27] is shown in Fig. 8. The inverters connected to the drain of the transistors have the possibility of absorbing the drain capacitance, C, and the package inductance, L_s, as part of the inverter, resulting in a higher bandwidth.

For the carrier amplifier, we need an inverter that transforms ζR_{opt} to κR_{opt} under full-power. The same inverter will transform $\zeta R_{opt}/2$ to $2\kappa R_{opt}$ with 6 dB BO.

The peaking amplifier needs an identical inverter. Since the drain capacitor of the transistor is already present, depending on the value of the inverter ratio, adding a shunt capacitance or inductance on the drain side may be necessary. The component values can be calculated as:

$$C_1 = \frac{1}{\omega_0 R_{opt}\sqrt{\zeta\kappa}} \quad L_1 = \frac{R_{opt}\sqrt{\zeta\kappa}}{\omega_0} - L_s \tag{34}$$

$$C_5 = \frac{1}{\omega_0 R_{opt}\zeta} \quad L_5 = \frac{R_{opt}\zeta}{\omega_0} \tag{35}$$

where L_s is the series package inductance at the drain.

$$C_2 = \begin{cases} C_1 - C & \text{if } C_1 > C \\ 0 & \text{otherwise} \end{cases} \tag{36}$$

$$L_2 = \begin{cases} 1/[(C - C_1)\omega_0^2] & \text{if} C_1 < C \\ \infty & \text{otherwise} \end{cases} \tag{37}$$

For a good bandwidth performance, it is important to choose ζ and κ so that C_1 is nearly equal to the drain capacitance, C, if possible. In that case, there is no need for C_2 while a large value of L_2 can be kept to bias the device.

3.1.4 CN type III

The inductor, L_1, of the inverter of CN type II, can be replaced by a transmission line [12], making the circuits easily realizable at microwave frequencies (see Fig. 9). It can be approximated using a transmission line of impedance Z_H and length x_3 (in λ_0 units) as seen in Fig. 9.

We choose Z_H to be 40% higher than the higher impedance value to shorten its length, but not too high to avoid fabrication problems. The two unknown values, x_3 and C_3, can be found by equating the input impedance of the inverter to the required impedance at the center frequency.

The required values are determined by solving a number of cases and fitting a polynomial to the results. For an inverter that inverts $R_0 = \zeta R_{opt}$ to rR_0 with $r = \kappa/\zeta < 1$, we have

$$\omega_0 C_3 = \frac{-171.67r^3 + 466.58r^2 - 505.32r + 279.58}{100R_0}$$
$$x_3 = \frac{25.15p^3 - 67.43p^2 + 141.99p + 26.97}{1000} \tag{38}$$

$$\text{with } Z_H = 1.4R_0 \tag{39}$$

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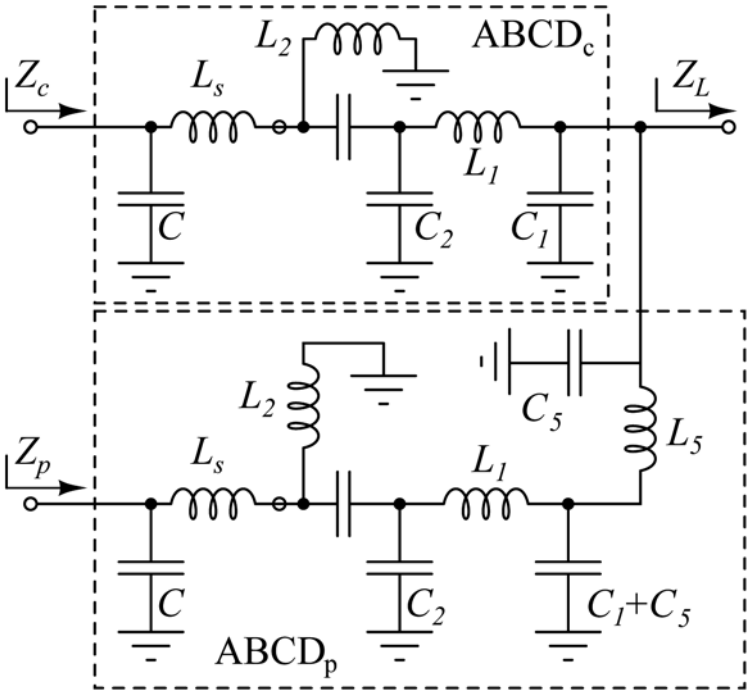

Fig. 8. CN type II.

where

$$p = \left(\sqrt{r} - \frac{\omega_0 L_s}{R_0}\right)^2 \tag{40}$$

If Z_H value of equation (39) is too high for implementation, equations (63) and (64) of Appendix B can be used for a smaller Z_H. If the required shunt capacitance is smaller than the drain capacitance of the transistor, a shunt inductance (L_3) can be added, which can also act like the DC power feed for the transistor. The remaining component values can be determined from

$$C_4 = \begin{cases} C_3 - C & \text{if} C_3 > C \\ 0 & \text{otherwise} \end{cases} \tag{41}$$

$$L_3 = \begin{cases} 1/[(C - C_3)\omega_0^2] & \text{if} C_3 < C \\ \infty & \text{otherwise} \end{cases} \tag{42}$$

$$Z_5 = \zeta R_{opt} \tag{43}$$

3.2 PMN

A PMN providing the desired combining node impedance can be chosen depending on the bandwidth requirement and the ratio of Z_{out} to Z_L. A number of possibilities are shown in Fig. 10.

In (a), a single quarter-wave transmission line is used to transform Z_L to Z_{out} with

$$Z_A = \sqrt{Z_L Z_{out}} \tag{44}$$

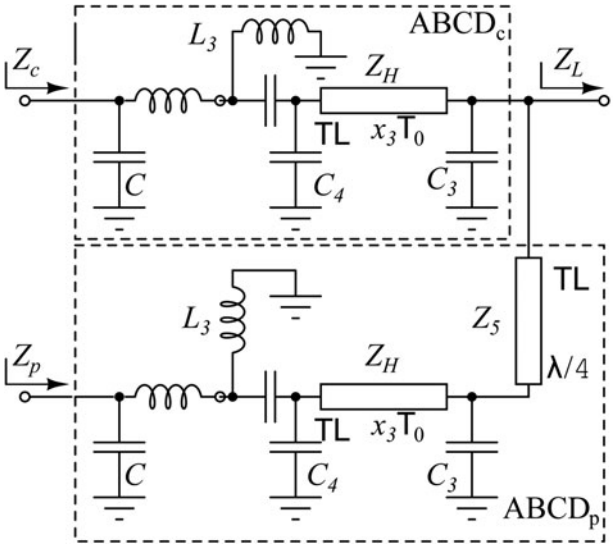

Fig. 9. CN III.

If $\zeta R_{optc}/2$ is close to Z_{out}, one section is enough even in a wide band. For a larger transformation ratio, two λ/4 transmission lines may be used as shown in (b) with values

$$Z_B = Z_L^{3/4} Z_{out}^{1/4} \text{ and } Z_C = Z_L^{1/4} Z_{out}^{3/4} \tag{45}$$

The impedance transformation can also be achieved with a small size lumped element inverter shown in (c). In this case, we should choose

$$L_a = \frac{\sqrt{Z_L Z_{out}}}{\omega_0} \text{ and } C_a = \frac{1}{\omega_0^2 L_a} \tag{46}$$

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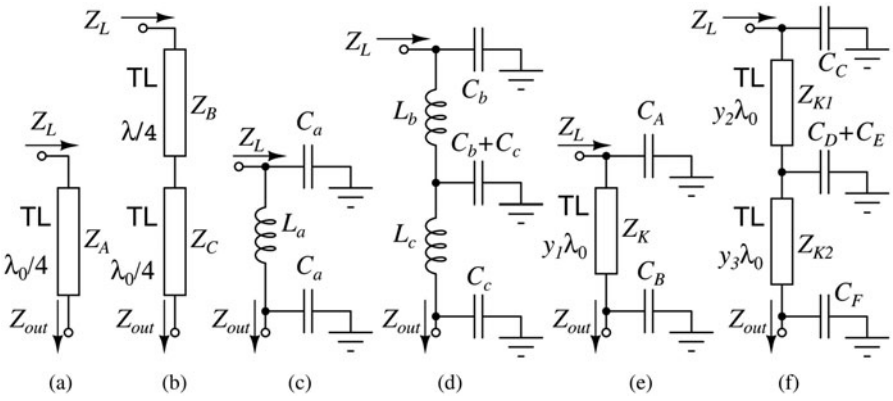

Fig. 10. Different PMNs.

For a wider bandwidth or when the transformation ratio is high, two inverters can be used as shown in (d) with

$$L_b = \frac{Z_L^{3/4} Z_{out}^{1/4}}{\omega_0} \text{ and } C_b = \frac{1}{\omega_0^2 L_a} \tag{47}$$

$$L_c = \frac{Z_L^{1/4} Z_{out}^{3/4}}{\omega_0} \text{ and } C_c = \frac{1}{\omega_0^2 L_a} \tag{48}$$

When a lumped inductance is not desirable or practical, PMN shown in (e) can be utilized: a high impedance (Z_K) transmission line and two shunt capacitors, C_A and C_B. Since we do not need an inverter, the shunt capacitances do not have to be equal in value, hence providing higher bandwidth. The electrical length, y_1, of the transmission line (in λ_0 units) can be found from the solution of the nonlinear equation

$$\frac{Z_A}{Z_K} - \frac{2\pi y_1}{\cos^2(2\pi y_1)} = 0 \tag{49}$$

We equate the real part of Z_{L1} to $Z_L(\omega_0)$ and the imaginary part of Z_{L1} to 0, both at ω_0. We find C_A and C_B, by solving the resulting nonlinear equations numerically. For an impedance transformer that transforms rR_0 to R_0 with $0.4 < r < 1$ we have

$$\omega_0 C_A = \frac{27.06r^3 - 76.17r^2 + 83.14r - 11.76}{100R_0} \tag{50}$$

$$\omega_0 C_B = \frac{-181.59r^3 + 503.13r^2 - 568.26r + 268.09}{100R_0}$$
$$y_1 = \frac{25.37r^3 - 78.17r^2 + 108.17r + 29.24}{1000} \tag{51}$$

$$\text{and } Z_K = 1.4R_0 \tag{52}$$

Since the combining networks are of low-pass type, the band center is smaller than ω_0.

For a wider band or when the transformation ratio from Z_L to Z_{out} is high, one may repeat the transformation operation in two steps and use two sections of the circuit of (e) as shown in (f).

Table 3. Bandwidth performance of different PMNs

PMN	Z_{out}/Z_L	1.5	1.7	2	3	5
(a)	f_1/f_0	0.3	0.53	0.67	0.80	0.87
	f_2/f_0	1.7	1.47	1.33	1.2	1.13
(b)	f_1/f_0	0.25	0.4	0.5	0.63	0.70
	f_2/f_0	1.8	1.6	1.5	1.37	1.3
(c)	f_1/f_0	0.77	0.79	0.81	0.86	0.90
	f_2/f_0	1.13	1.13	1.12	1.11	1.08
(d)	f_1/f_0	0.71	0.72	0.73	0.75	0.78
	f_2/f_0	1.18	1.18	1.17	1.17	1.16
(e)	f_1/f_0	0.34	0.57	0.69	0.83	0.95
	f_2/f_0	1.37	1.30	1.22	1.16	1.14
(f)	f_1/f_0	0.39	0.51	0.62	0.75	0.83
	f_2/f_0	2.05	1.97	1.91	1.73	1.58

The performances of different PMNs as a function of transformation ratio, Z_{out}/Z_L, are given in Table 3 for the condition that the transformed impedance has a return loss higher than 15 dB. Note that the networks can also be used with the inverted transformation ratio.

An inspection of the table indicates that lumped element networks (PMN types (c) or (d)) can be used only when the transformation ratio and/or the bandwidth is small. For wider bandwidths or when the transformation ratio is high, for example, with high power transistors with large ξ values, PMN type (b) gives the best performance. PMN types (e) and (f) give a good performance despite their smaller size. The center frequency of the PMN may have to be shifted, since the band limits are not always symmetrical.

4. Optimized combining networks

For the purpose of optimization, we define the bandwidth of a DPA in which all of the following constraints are satisfied:

- The efficiency at 6 dB output BO is higher than 50%
- The efficiency at full-power is higher than 60%
- The power at 6 dB output BO is at most 1.5 dB less than the normal value.
- The power at full-power is at most 1.5 dB less than the normal value.

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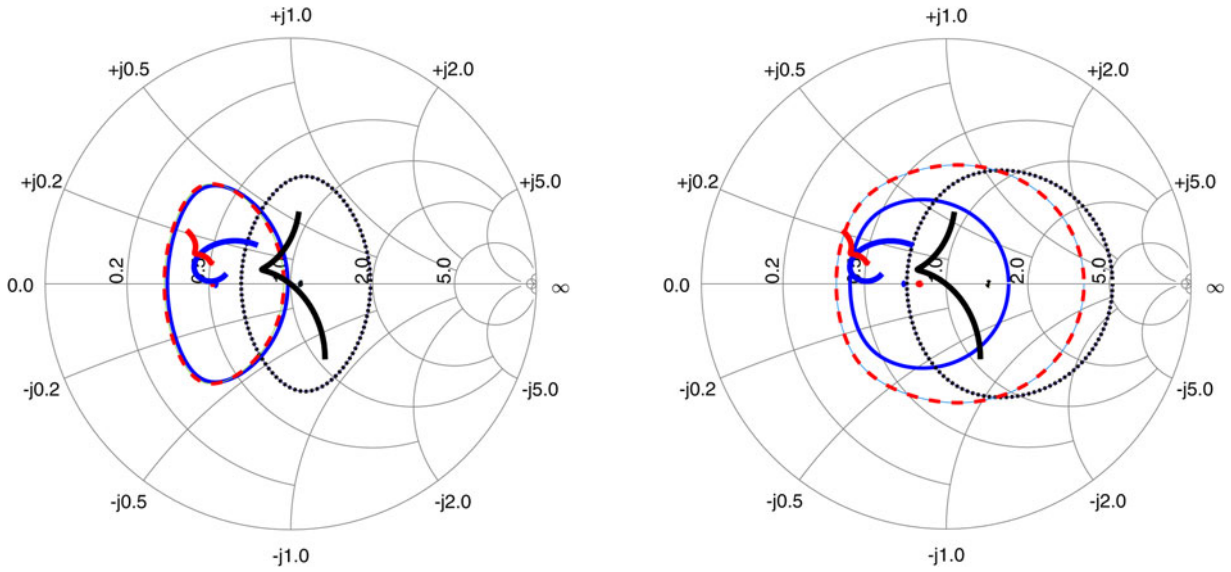

Fig. 11. Limiting power (left) and efficiency (right) contours on Smith charts, for carrier amplifier at full-power (solid) and 6 dB backoff (dotted), and for peaking amplifier at full-power (dashed). Impedances seen by the amplifiers as a function of frequency ($0.79f_0$ to $1.20f_0$) are also shown.

Table 4. Normalized band limits of DPA with optimized ζ and κ for CGH400XX family transistors at different frequencies

CN	f_0 (GHz)	ζ	κ	f_1/f_0	f_2/f_0	$\frac{Z_{out}}{\xi Z_L}$
Conv.	1.0	1.2	1.2	0.793	1.200	3.21
	1.5	1.2	1.2	0.834	1.185	3.40
	2.0	1.2	1.2	0.852	1.165	3.62
	2.5	1.2	1.2	0.865	1.147	3.95
	3.0	1.2	1.2	0.878	1.134	4.45
	3.5	1.2	1.2	0.885	1.121	5.08
I	1.0	4.8	0.84	0.685	1.315	0.80
	1.5	4.8	0.84	0.720	1.295	0.85
	2.0	4.8	0.84	0.745	1.265	0.91
	2.5	4.8	0.84	0.776	1.231	0.98
	3.0	4.8	0.84	0.785	1.210	1.11
	3.5	4.8	0.84	0.798	1.188	1.27
II	1.0	2.6	0.94	0.605	1.195	1.44
	1.5	2.8	0.93	0.597	1.190	1.34
	2.0	2.9	0.91	0.593	1.187	1.30
	2.5	3.1	0.87	0.64	1.18	1.21
	3.0	3.3	0.84	0.67	1.170	1.14
	3.5	3.5	0.84	0.695	1.150	1.07
III	1.0	2.1	1.14	0.560	1.21	1.79
	1.5	2.2	1.02	0.555	1.220	1.71
	2.0	2.2	0.99	0.565	1.230	1.71
	2.5	2.2	0.91	0.626	1.230	1.71
	3.0	2.2	0.84	0.66	1.213	1.71
	3.5	2.4	0.84	0.68	1.162	1.56

The input matching network and PMN is assumed to be properly chosen not causing a band limitation.

Table 5. Normalized band limits of DPA with optimized ζ and κ for a transistor with L_s=0 and different combining networks

CN	Q	ζ	κ	f_1/f_0	f_2/f_0	$\frac{Z_{out}}{\xi Z_L}$
Conv.	0.3	1.2	1.2	0.805	1.210	3.75
	0.5	1.2	1.2	0.840	1.175	3.75
	0.7	1.2	1.2	0.858	1.145	3.75
	1.0	1.2	1.2	0.886	1.123	3.75
	1.5	1.2	1.2	0.912	1.094	3.75
	2.0	1.2	1.2	0.929	1.075	3.75
I	0.3	5.0	0.84	0.684	1.342	0.75
	0.5	5.0	0.84	0.733	1.297	0.75
	0.7	5.0	0.84	0.768	1.261	0.75
	1.0	5.0	0.84	0.807	1.218	0.75
	1.5	5.0	0.84	0.855	1.165	0.75
	2.0	5.4	0.84	0.890	1.125	0.75
II	0.3	2.9	0.98	0.520	1.200	1.30
	0.5	2.9	0.98	0.520	1.200	1.30
	0.7	3.0	0.93	0.570	1.200	1.25
	1.0	3.2	0.89	0.685	1.200	1.17
	1.5	3.5	0.87	0.790	1.160	1.07
	2.0	4.5	0.86	0.860	1.130	0.84
III	0.15	3.0	0.94	0.530	1.267	1.25
	0.3	3.0	0.94	0.530	1.267	1.25
	0.5	3.1	0.94	0.530	1.267	1.25
	0.7	3.1	0.85	0.615	1.240	1.21
	1.0	3.6	0.84	0.725	1.230	1.04
	1.5	4.0	0.84	0.815	1.177	0.94
	2.0	4.2	0.84	0.865	1.140	0.89

The input matching network and PMN are assumed not to cause a band limitation.

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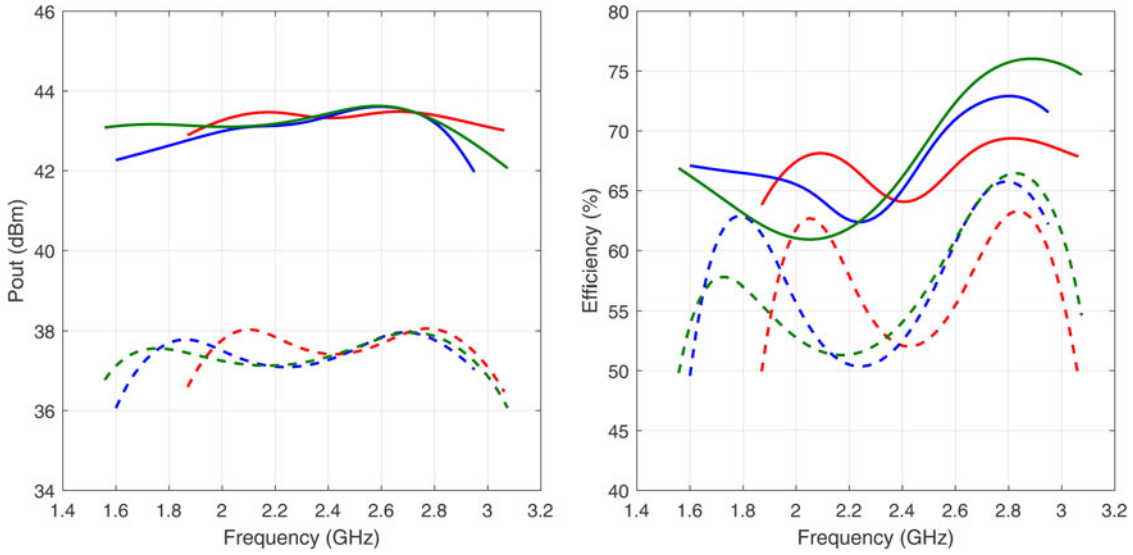

Fig. 12. Comparison of power outputs (left) and efficiencies (right) of CN types I (red), II (blue), and III (green), all using transistors with $Q = 0.77$. Solid lines represent full power and dashed lines represent 6 dB BO.

Here, "full-power" is defined as the dB gain compression point at the center frequency with the optimal load. We should also consider linearity of the DPA and keep it within acceptable limits. The 1.5 dB value above is chosen as a compromise between linearity and bandwidth. A higher value will result in a higher bandwidth with more nonlinearity.

For bandwidth optimization of the conventional CN, the combining node impedance, $Z_L = \zeta R_{opt}/2$ should be as high as possible to minimize the quality factor of drain capacitance tuning network. We can increase ζ only up to 1.2, since $\zeta = \kappa > 1.2$ results in an unacceptable level of nonlinearity.

For other types of CN, we can increase ζ to higher values, while keeping κ less than unity for a large band.

As an example, we consider CN type I and PMN type (a) with $\zeta = 4.8$, $\kappa = 0.84$ at $f_0 = 3.5$ GHz. We show the power and efficiency contours defined by the constraints above on the Smith charts of Fig. 11 for both carrier and peaking amplifiers. In the same charts, we also show the impedances experienced by the carrier (Z_c) and peaking (Z_p) amplifiers as a function of frequency at two drive levels, which should stay inside the relevant contours.

These Smith charts can be used to observe the variation of impedances as the values of ζ and κ are varied. The values are then optimized to reach the widest bandwidth. Those factors should be chosen to keep the impedance values within the power and efficiency contours for as wide frequency range as possible. We note that decreasing the value of κ moves the impedance curves toward the left, reducing the power and efficiency at the center frequency while boosting power and efficiency at the band edges. On the other hand, a higher ζ improves the bandwidth at the backoff level resulting in a reduction of the bandwidth at full-power.

Table 4 gives the optimized results for CGH400XX series transistors at different center frequencies assuming that PMN matches Z_L to Z_{out} perfectly at all frequencies. The values of ζ and κ as well as the normalized band limits are given in the same table for different types of combining networks.[5] This table is applicable for transistors scaled with factor ξ, since an increase in the transistor gate width simply causes a reduction of the combining node impedance to Z_L/ξ.

Table 6. Component values for the CN type I and PMN type (a) with $f_0 = 3.5$ GHz

Comp.	Eq.	Value	Comp.	Eq.	Value
Z_1	32	32.9 Ω	Z_2	33	21.3 Ω
Z_3	33	50.9 Ω	Z_A	44	44.3 Ω

The effect of series drain inductance, L_s, is negligible at lower frequencies or in MMIC circuits where the transistors are integrated with the rest of the combining circuit. In such cases, it is possible to list more general results in terms of drain quality factor, Q, rather than frequency. With the definition

$$Q = \omega_0 C R_{opt} \tag{53}$$

we provide such results in Table 5. Since all values in the table are normalized, they are applicable for the design of a DPA at any frequency band with any transistor, if C and R_{opt} of transistor are known.

Inspection of Tables 4 and 5 indicates that widest bandwidth is obtained with CN type II or III since C and L_s can be absorbed as part of the combining network. In Fig. 12 we present a comparison of different CN types for CGH400XX transistors with $f_0 = 2.5$ GHz, showing the power and efficiency at full-power and 6-dB BO. CN type III gives the widest bandwidth, while type II is slightly worse. CN type I may still be preferred for its ease of implementation even though it has the smallest bandwidth.

Tables are given for our specific bandwidth definition given above. If the limiting values in that definition are relaxed, it is possible to obtain DPAs with a wider bandwidth but with a lower performance.

[5]Using the provided MATLAB code, it is possible to determine the optimal ζ and κ values and the corresponding band limits for other technologies, when the transistor is approximated by three parameters.

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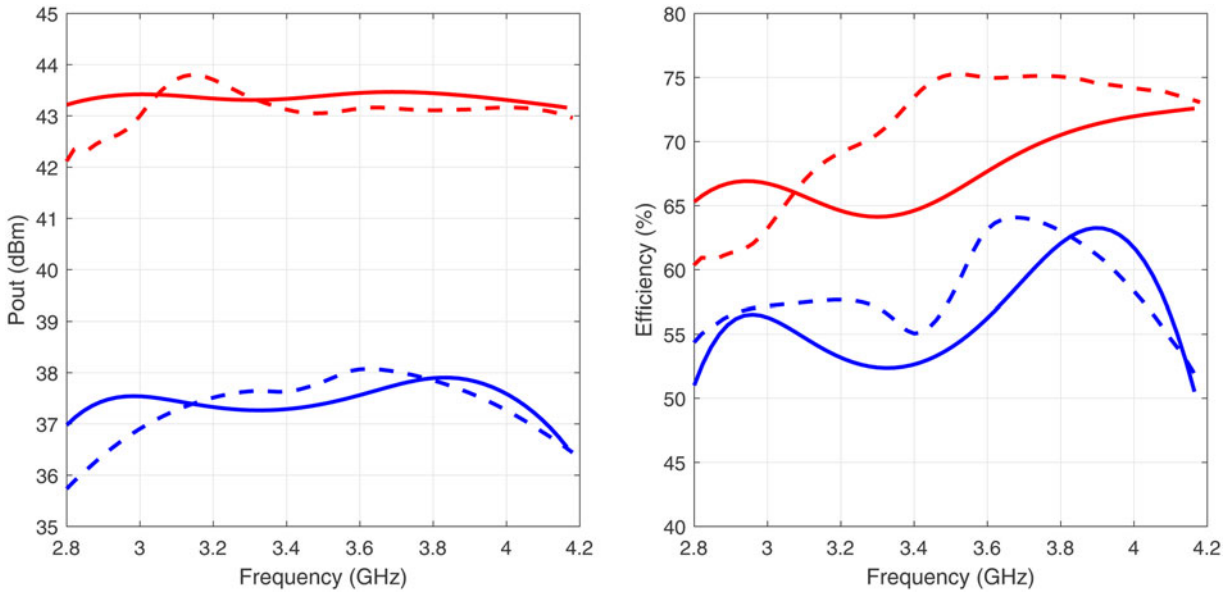

Fig. 13. Power output (left) and efficiency (right) of the the first example as a function of frequency for full-power (red) and for 6 dB BO (blue). Harmonic balance simulations (dashed) are also drawn.

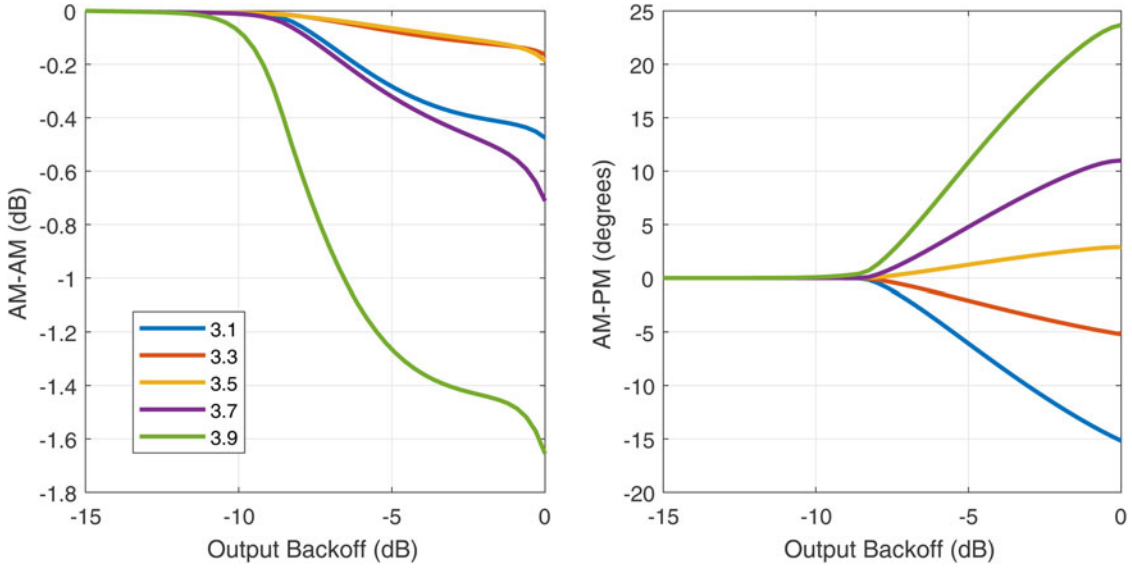

Fig. 14. AM-AM (left) and AM-PM (right) characteristics of the first example at 3.1, 3.3, 3.5, 3.7, and 3.9 GHz.

5. Example designs

To demonstrate the use of our method, we give a number of example DPA designs.

5.1 Example I

As the first example, we use a CN type I with CGH40010 (ξ=1) at $f_0 = 3.5$ GHz. At this frequency we have $R_{opt} = 16.4\,\Omega$ and $L = 0.935$ nH from Table 2. From Table 4, we set $\zeta = 4.8$ and $\kappa = 0.84$ to get a band from $f_1 = 2.8$ GHz to $f_2 = 4.16$ GHz. With $Z_{out}/Z_L = 1.27$, it is sufficient to use PMN type (a), (c), or (e) without limiting the bandwidth. The values of components in the output network as calculated from relevant equations are given in Table 6 for PMN type (a).

Table 7. Component values of the second example of CN type II and PMN type (b) at $f_0 = 2.5$ GHz

Comp.	Eq.	Value	Comp.	Eq.	Value
L_1	34	0.99 nH	L_2	37	4.52 nH
C_1	35	3.70 pF	C_2	35	0
L_5	43	2.10 nH	C_5	44	1.93 pF
Z_B	45	21.8 Ω	Z_C	45	37.9 Ω

Note that the inductance L can be replaced with a high impedance transmission line of length determined by equation (30). The results from both our model and harmonic balance simulation

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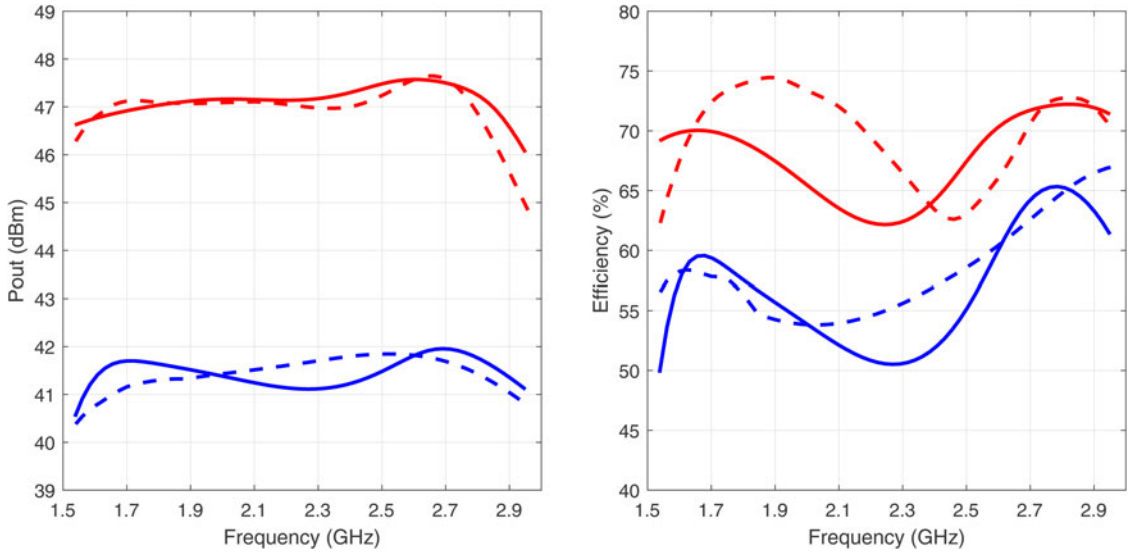

Fig. 15. Power output (left) and efficiency (right) of the second example as a function of frequency for full-power (red) and for 6 dB BO (blue). Harmonic balance simulations are also shown (dashed).

using vendor supplied nonlinear model of the transistors are shown in Fig. 13. Since we ignore the bandwidth limitation of the input matching networks, for a fair comparison we connect voltage sources with zero source impedance as the input driving sources in the harmonic balance simulations. Similarity between the curves is a verification for our simple model.

In Fig. 14 we present the calculated AM-AM and AM-PM distortions of this example at different frequencies. The phase distortion becomes significant when the peaking transistor begins to conduct. As it is previously shown [28–31], frequency-dependent AM/PM nonlinearity is an undesired attribute of Doherty amplifiers, which may be reduced by analog or digital predistortion methods or by modifying the input power split ratio.

If we had used the transistor CGH40045 with $\xi = 4.5$, L, Z_1, Z_2, and Z_3 would have been scaled down by 4.5 and $Z_{out}/Z_L = 1.27$ $\xi = 5.71$ would have required PMN type (b) or (f). For such a large transistor, however, the assumption of input side matching network not limiting the bandwidth may be optimistic.

5.2 Example II

As the second example, we use CN type II with CGH40025 ($\xi = 2.5$) for $f_0 = 2.5$ GHz. We use $R_{opt} = 26.6/\xi = 10.6\,\Omega$ from Table 2 since the effect of L_s is eliminated with CN type II. From Table 4, we set $\zeta = 3.1$ and $\kappa = 0.87$ and get a band from $f_1 = 1.60$ GHz to $f_2 = 2.95$ GHz. With $Z_{out}/Z_L = 1.30$ $\xi = 3.03$, we should use PMN type (b) or type (f) not to reduce bandwidth. The component values are given in Table 7 for PMN type (b).

We plot the results in Fig. 15 along with harmonic balance simulation of the same circuit.

5.3 Example III

At the last example, we use a small center frequency ($f_0 = 0.5$ GHz) to demonstrate the use of Table 5. At this frequency the effect of L_s is negligible. With $R_{opt} = 26.6\,\Omega$ and $C = 1.84$ pF, we have $Q = 0.15$. We use CN type III. From the table we set ζ=3.0 and $\kappa = 0.97$ to get a band from $f_1 = 0.26$ to $f_2 = 0.61$ GHz. With $Z_{out}/Z_L = 1.25$ a PMN type (e) is sufficient. The component values are given in Table 8.

Table 8. Component values of the example III at $f_0 = 0.50$ GHz

Comp.	Eq.	Value	Comp.	Eq.	Value
x_3	62	0.098	Z_H	62	79.8 Ω
C_3	61	5.75 pF	C_4	41	3.91 pF
Z_5	43	79.8 Ω			
y_1	52	0.078	Z_K	52	70 Ω
C_A	50	1.26 pF	C_B	51	2.69 pF

6. Experimental results

For the purpose of comparing our results with experimental results, we relax the efficiency limits in our bandwidth definition to take care of losses in the output combining network: 46% for 6 dB BO and 56% for full-power.

6.1 DPA with type I combining network

We built a DPA using type I CN with $\zeta = 4.8$ and $\kappa = 0.84$ centered at 1.0 GHz. The schematic of the amplifier using two CGH40010 transistors is given in Fig. 16. Since $Z_{out}/Z_L = 0.80$, a simple PMN of a tapered line of 0.35 λ at 1.0 GHz is sufficient. Optimized element values along with calculated values are given in Table 9.

The DPA is implemented on Rogers 4003C[6] substrate with 0.508 mm thickness. The photo of the implementation can be seen in Fig. 17. The performance of the amplifier is depicted in Fig. 18 where the efficiency is better than 56% at full power and 46% at 6 dB BO. We achieved a bandwidth from 0.67 to 1.35 GHz, while the predicted bandwidth from Table 4 is 0.69–1.30 GHz, verifying our method.

[6]Rogers Corp, www.rogerscorp.com

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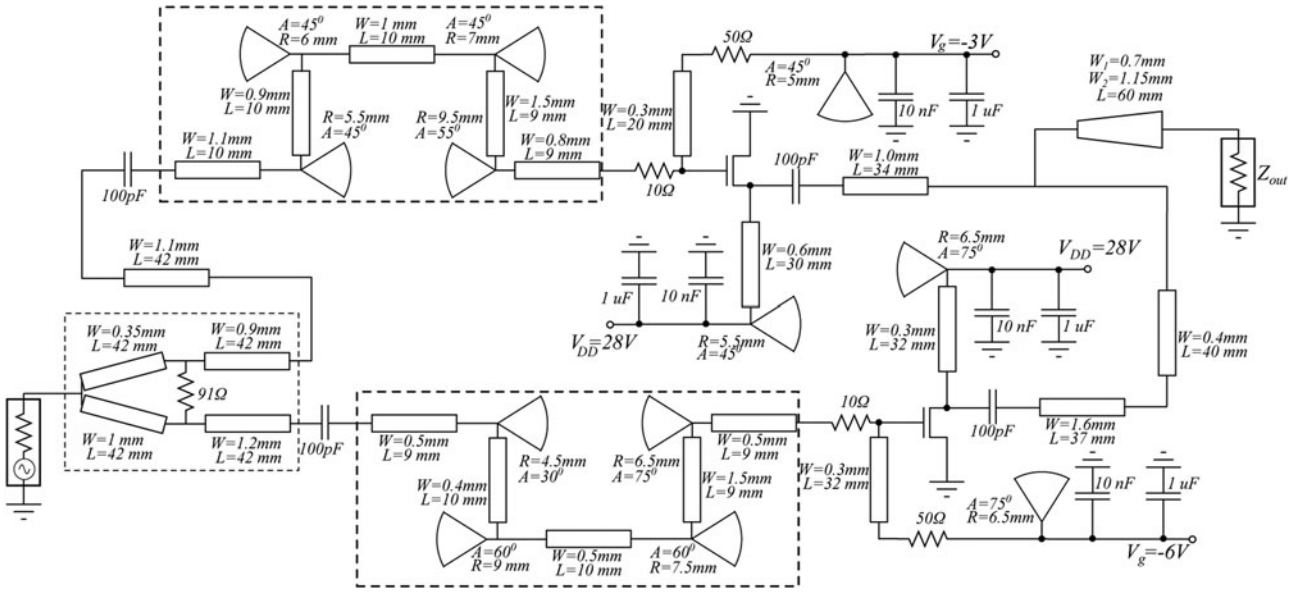

Fig. 16. The circuit schematic of fabricated wideband Doherty power amplifier.

Table 9. Component values for CN type I and OMN type (a) at $f_0 = 1.0$ GHz

Comp.	Eq.	Calculated value	HB Optimized value
Z_1	32	50.2 Ω	53.9 Ω
Z_2	33	33.6 Ω	40.1 Ω
Z_3	33	80.4 Ω	85.1 Ω
Z_L	44	62.2 Ω	65.6 Ω

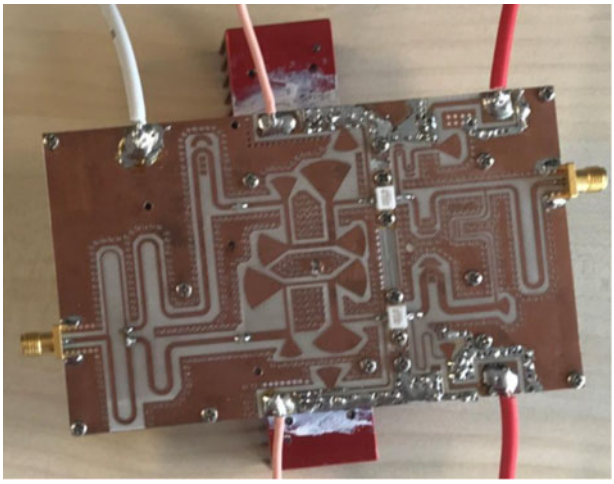

Fig. 17. Photograph of the fabricated wideband DPA. The dimensions are 20 × 10 cm.

6.2 Examples from previous works

We chose three experimental studies from literature whose limiting values are within or close to those in our bandwidth definition. Table 10 lists those studies for the estimated ζ and κ values to the best of our understanding as well as the predicted and measured band limits. Comparison of ζ and κ values to those in the Table 4 indicates that they are close to optimum values. The measured band limits are also consistent with our expectations. It is possible to find other examples in the literature with a wider bandwidth, but they have lower performance for efficiency within the band.

7. Conclusion

In this paper, we presented a method to design the output combining network of a wideband DPA maximizing the bandwidth of operation. We used a simple analytical model of the RF transistor with a few parameters (V_T, G_m, N_e, C, and L_s), and showed that the results are very similar to those obtained from harmonic balance simulation with a much more complex model of transistor.

We first presented a bandwidth definition for the DPA with strict limits on efficiency and power output performance. To optimize the bandwidth performance, we introduced two factors, ζ and κ. They are the multiplying factors for the impedance at the combining node and the impedance seen by transistors, both defined at the center frequency. For the given three parameters of a transistor and the type of the combining network, an optimal pair of ζ and κ can be determined. We presented a table that lists those values as a function of frequency. We also gave explicit formulas for all element values of the combining network. We showed that the higher power transistors of the same family can be used by a proper scaling of the combining network element values. We also presented a method to choose the post-matching network in order not to degrade the bandwidth performance.

If the package inductance, L_s, of the transistor is negligible, then it is possible to list the optimal values only in terms of transistor output quality factor, Q, making this second table more general for applications in lower frequencies or in MMICs.

The tables can be used to determine the potential bandwidth performance of a DPA using transistors with a quality factor, Q. Alternatively, they can be used in choosing a proper transistor for a DPA with a given bandwidth goal. We gave example designs to demonstrate the use of both tables to find all element values.

Among the three different CN topologies studied, type II gives a good bandwidth performance in applications where the

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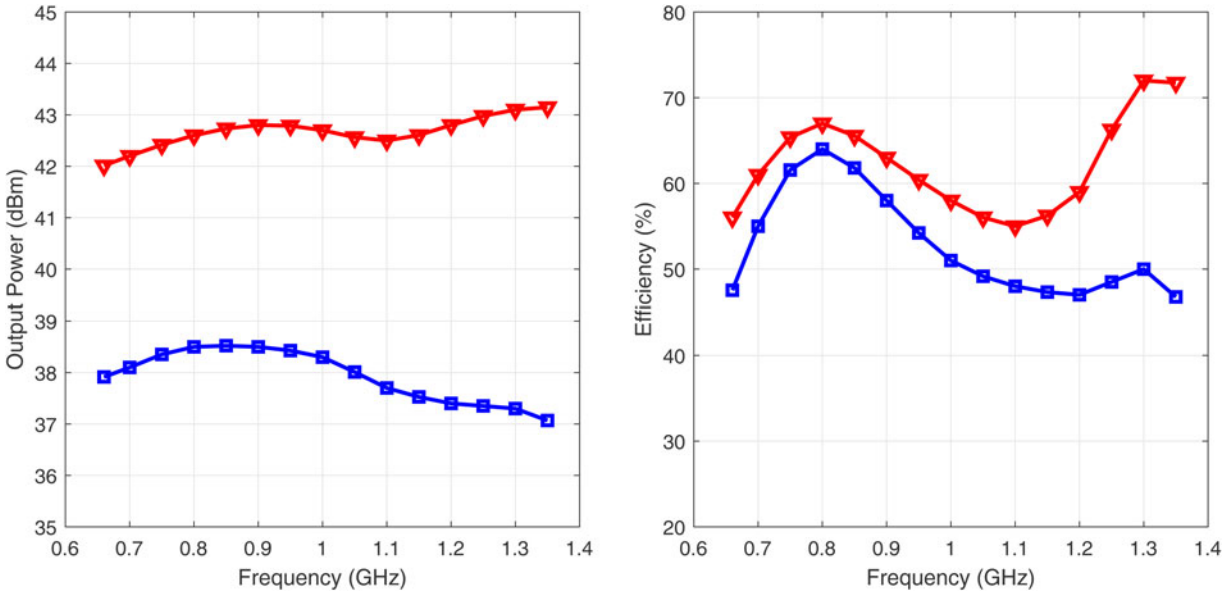

Fig. 18. Measurements of fabricated DPA: power output (left) and efficiency (right) as a function of frequency for full-power (red) and for 6 dB BO (blue).

Table 9. Summary of this work (T.W.) and three studies from the literature at full-power (FP) and at 6 dB BO

	T.W.	[22]	[27]	[20]
CN	I	I	II	III
OMN	(a)	N/A	N/A	(b)
ζ	4.8	4	2	2.1
κ	0.84	1	1.2	1.1
f_0 (GHz)	1.0	2.35	2.5	2.3
Q	0.29	0.66	0.7	0.64
f_1/f_0 (theo)	0.69	0.78	0.83	0.60
f_2/f_0 (theo)	1.30	1.22	1.14	1.18
f_1/f_0 (mea)	0.67	0.9	0.8	0.69
f_2/f_0 (mea)	1.35	1.13	1.08	1.17
η_{BO}(%)	46–64	39–67	48–63	46–63
P_{BO} (dBm)	37–38.5	35–39	34–35.5	37–38.5
η_{FP}(%)	56–71	57–84	46-60	56–75
P_{FP} (dBm)	42–43.1	41–45	40-41	43.8-45.2

distributed components are not preferred because of their size. CN type III can be implemented easily at higher frequencies and with a slightly better performance compared to type II. CN type I should be preferred for its robustness if a wide bandwidth is not required and the size is not a problem.

A higher power version of the DPA with the same bandwidth can be implemented by scaling of the transistors and the combining network element values, provided that a sufficiently wideband post-matching network is utilized to take care of the reduced combining node impedance.

Obviously, for the complete DPA design input matching, stabilization and input unequal dividing network must be added. Due to the bandwidth limitation of the input side, the resulting bandwidth of the DPA will be somewhat smaller than predicted here.

Even though our transistor model is extremely simple, the results obtained from our model are very close to harmonic balance simulations using the complex nonlinear models of transistors. Hence our method is very useful if there is no available nonlinear model of the transistors in a MMIC application. One can easily extract R_{opt}, C, and L_s from the measured load-pull data of the transistor. Those parameters are sufficient to design the output combining networks.

If the transistor has a vendor supplied model, the proposed circuit topology and calculated values from our method can be used as a good starting point of further optimization in a harmonic balance simulator.

Supplementary material. The supplementary material for this article can be found at https://doi.org/10.1017/S1759078722000381

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8.Appendix A.

We can expand equation (5) in a cosine series as

$$i_D = \left(A_0 + \sum_{n=1}^{\infty} A_n \cos(n\theta)\right) \cdot \left(k_0 + \sum_{n=1}^{N_e+1} [k_{n,R}\cos(n\theta) + k_{n,Q}\sin(n\theta)]\right) \tag{54}$$

where

$$A_0 = \frac{G_m(V_B - V_T)}{\pi}\left(\alpha_2 - \frac{\sin\alpha_2}{\cos\alpha_2}\right) \tag{55}$$

$$A_n = \frac{2G_m(V_B - V_T)}{\pi}\left[\frac{\sin(n\alpha_2)}{n} - \frac{1}{\cos\alpha_2}\left(\frac{\sin((n-1)\alpha_2)}{2(n-1)} + \frac{\sin((n+1)\alpha_2)}{2(n+1)}\right)\right] \tag{56}$$

$$\alpha_2 = \cos^{-1}\left(\frac{-(V_B - V_T)}{V_{in}}\right) \tag{57}$$

and with $\mathbf{V_1} = V_1 e^{j\Phi}$ [26]

$$k_0 = 1 - \frac{1}{2}\left(\frac{V_1}{2V_{DD}}\right)^{N_e}\binom{N_e}{N_e/2} \tag{58}$$

$$\begin{aligned} k_{2n,R} &= -\left(\frac{V_1}{2V_{DD}}\right)^{N_e}\binom{N_e}{N_e/2 - n}\cos(2n\phi) \\ k_{2n-1,R} &= \left(\frac{V_1}{2V_{DD}}\right)^{N_e+1}\binom{N_e+1}{N_e/2+1-n} \end{aligned} \tag{59}$$

$$\cos((2n-1)\phi) \tag{60}$$

$$\begin{aligned} k_{2n,Q} &= \left(\frac{V_1}{2V_{DD}}\right)^{N_e}\binom{N_e}{N_e/2 - n}\sin(2n\phi) \\ k_{2n-1,Q} &= -\left(\frac{V_1}{2V_{DD}}\right)^{N_e+1}\binom{N_e+1}{N_e/2+1-n} \end{aligned} \tag{61}$$

$$\sin((2n-1)\phi) \tag{62}$$

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9.Appendix B.

If Z_H value found in equation (39) is too high for implementation, one can use the following formulas giving a longer transmission line with a lower Z_H value. For an inverter that inverts rR_0 to R_0 with $r < 1$, we have

$$\omega_0 C_i = \frac{-337.13r^3 + 725.94r^2 - 674.74r + 297.9}{100R_0}$$
$$x_i = \frac{300.95p^3 - 497.42p^2 + 427.76p - 1.718}{1000} \quad (63)$$

$$\text{with} Z_H = R_0 \quad (64)$$

where p is given by equation (40).

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