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A millimeter-wave fundamental and subharmonic hybrid CMOS mixer for dual-band applications

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Abstract

This paper proposes and presents a millimeter-wave (MMW) fundamental and subharmonic hybrid mixer in a 65-nm CMOS technology. Based on a hybrid structure with two switching quads and a quasi-diplexer, the proposed circuit can function either as a fundamental mixer (FM) or a subharmonic mixer (SHM) for dual-band applications. An application of the MMW hybrid mixer in a concurrent dual-band receiver is also discussed, which indicates that the proposed mixer can operate at two different MMW frequency bands concurrently as long as the frequency conversion schemes are carefully designed. Measured results show that the 3-dB RF bandwidth of the MMW hybrid mixer ranges from 16 to 35 GHz for the FM mode and 30 to 53 GHz for the SHM mode, respectively.

Introduction

With the development of wireless communication, sensing, and radar systems, demands for low-cost circuits and transceivers that can support multi-band and multi-mode operation are increasing rapidly [1–8]. As a key component of dual-band transceivers, dual-band mixers deserve in-depth study.

Several dual-band fundamental mixers (FMs) with dual-band impedance matching networks have been developed under 6 GHz [9–11]. However, it is difficult to implement local oscillators (LOs) with low phase noise and wide turning range at millimeter-wave (MMW) frequencies. By either mixing the input signal with the fundamental or higher-order harmonic component of the LO, dual-band performance can also be achieved [12, 13]. The mixers, which can be reconfigured between fundamental and subharmonic modes by changing the LO waveforms [14] or the bias conditions [15], have also been proposed for dual-band operation. In addition, an MMW dual-band switchable star mixer was also proposed by changing the effective length of the Marchand baluns [16]. However, these mixers can operate only in one band at a time, which are not suitable for concurrent dual-band applications [17–20].

In this paper, a fundamental and subharmonic hybrid CMOS mixer is proposed for MMW dual-band applications. Based on a hybrid structure with two switching quads and a quasi-diplexer, this circuit can function either as an FM or a subharmonic mixer (SHM). In addition, the hybrid mixer can operate at two MMW bands concurrently as long as the frequency conversion schemes are carefully designed.

Circuit design and analysis

Figure 1 shows the schematic of the proposed MMW CMOS hybrid mixer. It consists of two switching quads (M_1–M_8), equipped with 20-μm width transistors biased at $V_{GS} = 0.4$ V. The selection of device size and bias voltage was made to obtain a maximum conversion gain (CG) following the procedure presented in [21]. Herein, the voltage V_S (as shown in Fig. 1) is set to 0 V for simplicity, which can be set to other values to bias the baseband amplifiers in future work. Because there are no DC current paths for the transistors, the drain–source voltage (V_{DS}) of the transistors is 0 V. Different from conventional SHMs [21, 22], an additional "quasi-diplexer" formed by C_{B1}, C_{B2}, C_{F1}, C_{F2}, L_{F1}, and L_{F2} is inserted between the switching quads to establish a hybrid structure with two down-conversion paths (as shown in Fig. 1) for dual-band applications. The quasi-diplexer has a low-pass characteristic in path 1 and a high-pass characteristic in path 2. The values of C_{F1}, C_{F2}, L_{F1}, and L_{F2} are chosen to make the cutoff frequency of the low-pass filter (LPF) higher than the IF frequency (f_{IF}), whereas the values of C_{B1} and C_{B2} need to be small enough to block the IF signal in path 2. Three Marchand baluns are used to generate differential RF and LO signals [15, 23]. A 90° coupler and an inductor (L_C) are jointly used to provide an optimum LO phase distribution for the switching quads.

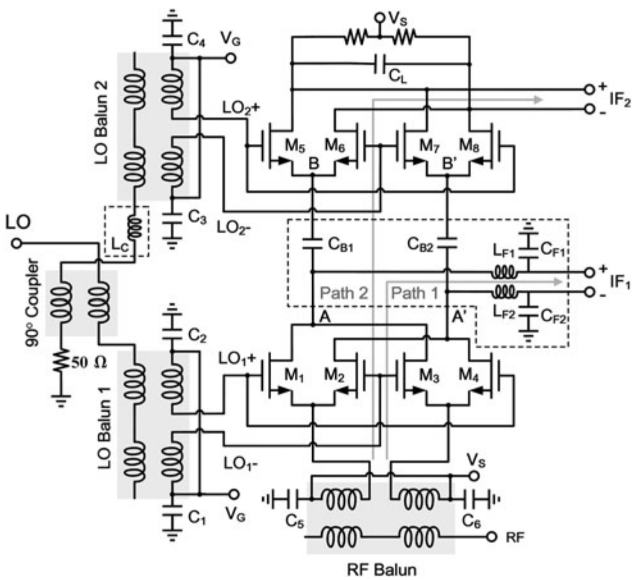

Fig. 1. Schematic of the proposed MMW CMOS hybrid mixer.

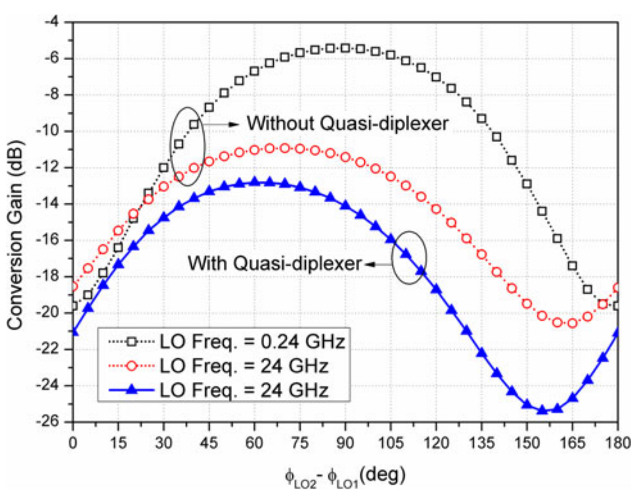

Fig. 2. Impact of the parasitic effects of the transistors and the existence of the quasi-diplexer on the simulated CG performance.

Assuming the two switching quads are driven by two phase-shifted square-wave LOs with a 50% duty cycle and the transistors are operating as ideal switches, the voltage across AA′ (as shown in Fig. 1) can be expressed as [24]:

$$\begin{aligned} v_{AA'}(t) &= V_{RF}\cos(2\pi f_{RF}t)\frac{4}{\pi}\sum_{n=0}^{\infty}\frac{1}{2n+1}\sin[2\pi(2n+1)f_{LO}t] \\ &= \frac{2}{\pi}V_{RF}\sum_{n=0}^{\infty}\frac{1}{2n+1}\sin[2\pi f_{RF}t - 2\pi(2n+1)f_{LO}t] \\ &\quad + \frac{2}{\pi}V_{RF}\sum_{n=0}^{\infty}\frac{1}{2n+1}\sin[2\pi f_{RF}t + 2\pi(2n+1)f_{LO}t] \end{aligned} \tag{1}$$

where f_{LO} is the LO frequency, V_{RF} and f_{RF} are the voltage amplitude and frequency of the RF signal, respectively.

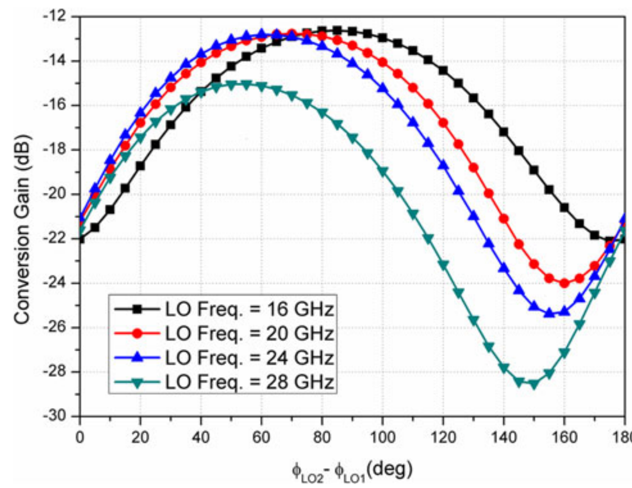

Fig. 3. Simulated CGs with respect to LO phase shift for different LO frequencies.

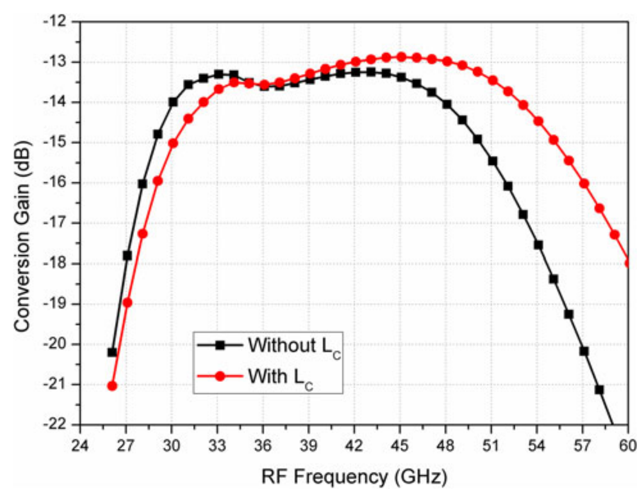

Fig. 4. Simulated CGs of the SHM with and without the inductor L_C.

Subharmonic mixing mode

For $f_{RF} = 2f_{LO} \pm f_{IF}$, where f_{IF} is the IF frequency, the lowest frequency in (1) is $f_{LO} - f_{IF}$. Because f_{LO} is much higher than f_{IF} in MMW applications, all the frequency components in (1) will be blocked by the LPF in path 1, because the cutoff frequency of the LPF is much lower than $f_{LO} - f_{IF}$. Therefore, they can only be passed to BB′ (as shown in Fig. 1) for the second stage of mixing and the subharmonic mixing is obtained in path 2.

Theoretically, the best CG performance is achieved when the LO_1 and LO_2 are in quadrature [21, 22]. In practical, however, the optimum LO phase shift will drift away from 90° due to the parasitic effects of the transistors at MMW frequencies [24] and the existence of the quasi-diplexer. Figure 2 illustrates the impact of the parasitic effects of the transistors and the existence of the quasi-diplexer on the simulated CG performance. For the SHM without the quasi-diplexer, the optimum LO phase shift drifts from 90 to 70° when the LO frequency moves from 0.24 to 24 GHz, due to the parasitic effects of the transistors [24]. Meanwhile, the maximum CG is decreased significantly because the modulating currents in the mixer find a path to ground through the substrate resistance and the parasitic source–bulk

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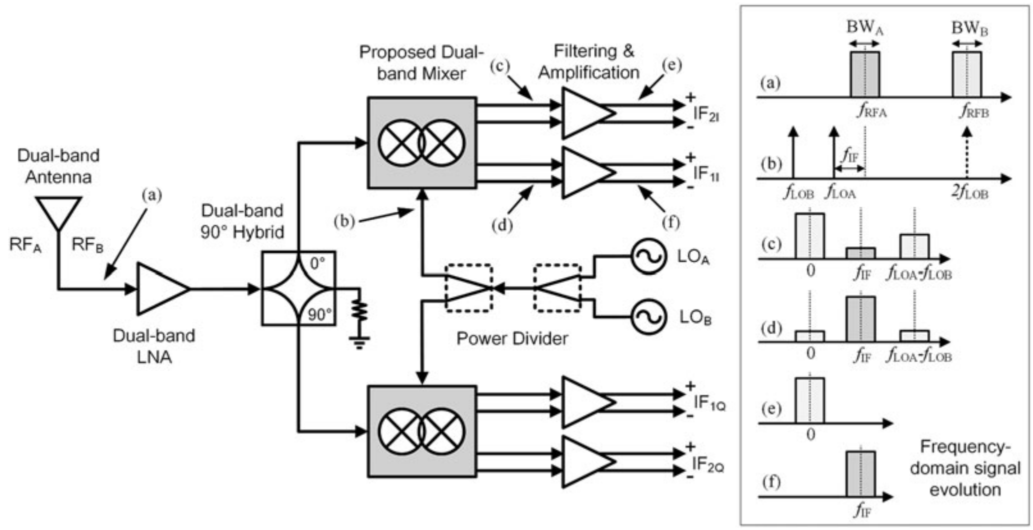

Fig. 5. An architecture for concurrent dual-band receiver.

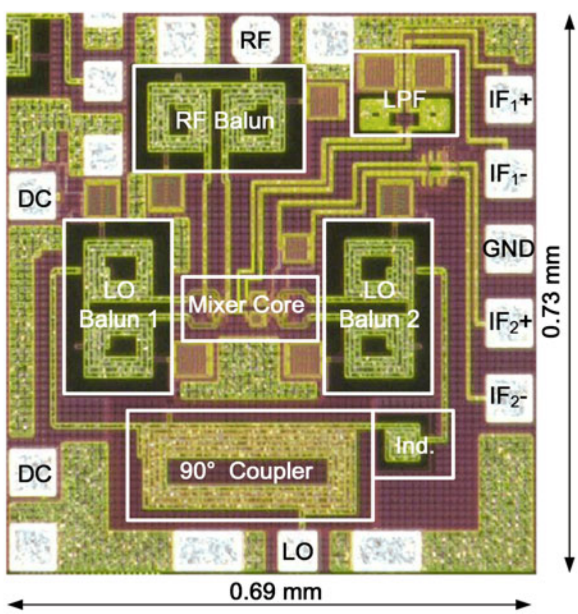

Fig. 6. Photo of chip of the proposed MMW hybrid CMOS mixer.

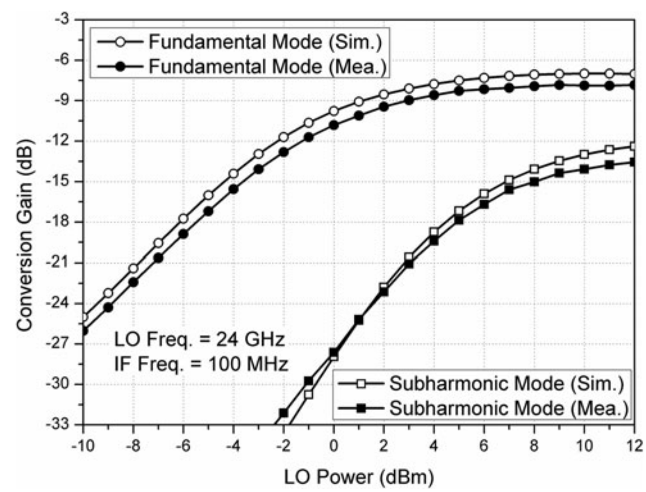

Fig. 7. Measured and simulated CGs versus LO power for both subharmonic and fundamental modes.

and drain–bulk capacitances at higher frequencies [21]. By adding the quasi-diplexer, the optimum LO phase shift further drifts from 70 to 60° at 24-GHz LO frequency, because the quasi-diplexer introduces additional phase delays for the frequency components in (1). In addition, the maximum CG is further decreased by 1.9 dB due to the insertion loss of the quasi-diplexer. Figure 3 shows the simulated CGs of the proposed SHM with respect to LO phase shift for different LO frequencies. As can be observed, the optimum LO phase shift is 85, 70, 60, and 55° for the LO frequency of 16, 20, 24, and 28 GHz, respectively. In this study, the LO phase shift of 60° is chosen, so that the CG is close to the peak value for the LO frequency of 20, 24, and 28 GHz, respectively, whereas the CG is only 0.8 dB lower than its peak value for the LO frequency of 16 GHz.

To achieve 60° of LO phase shift, a 350-pH inductor L_C is inserted between the 90° coupler and the LO balun 2. Figure 4 compares the simulated CGs of the SHM with and without L_C. By introducing the inductor L_C, the CG of the SHM is improved significantly at high LO frequencies but a little degraded at low LO frequencies. In future work, the optimum LO phase distribution can be implemented by investigating a novel coupler with arbitrary phase shift.

Fundamental mixing mode

For $f_{RF} = f_{LO} \pm f_{IF}$, the lowest two frequencies in (1) are f_{IF} and $2f_{LO} - f_{IF}$. Because the IF signal is blocked by the capacitors C_{B1} and C_{B2} in path 2, it can only be passed to the IF_1 port through path 1. Meanwhile, because the cutoff frequency of the LPF is much lower than $2f_{LO} - f_{IF}$, all the frequency components in (1) except for the IF signal will be filtered by the LPF. Therefore, only the IF signal is passed through path 1 and the fundamental mixing is obtained in path 1.

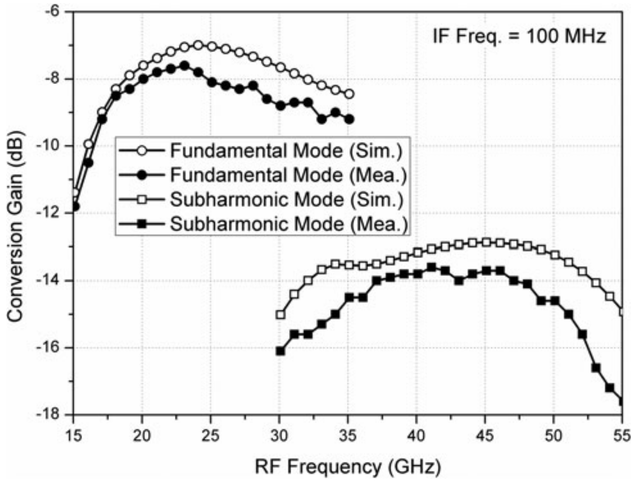

Fig. 8. Measured and simulated CGs versus RF frequency for both subharmonic and fundamental modes.

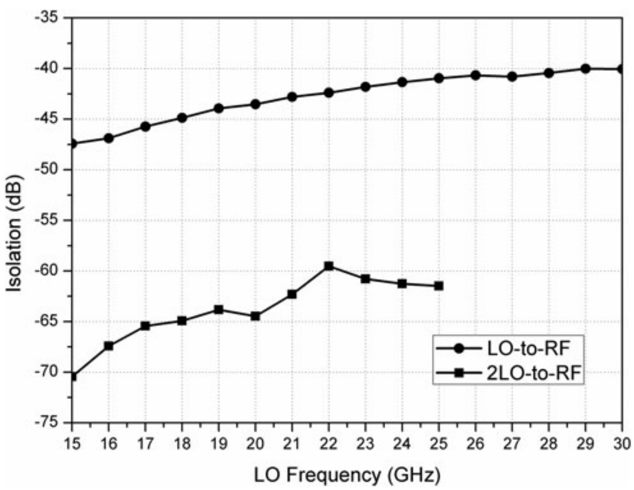

Fig. 9. Measured LO-to-RF and 2LO-to-RF isolations.

Concurrent mixing mode

By carefully assigning the LO frequencies, the proposed hybrid mixer can also function as a concurrent dual-band mixer. For instance, Fig. 5 shows an application of the hybrid mixer in a concurrent dual-band receiver that is capable of simultaneous operation at two different frequencies (f_{RFA} and f_{RFB}) by imposing the following conditions: (1) $f_{LOA} = f_{RFA} - f_{IF}$, (2) $f_{LOB} = f_{RFB}/2$, (3) $f_{IF} > (BW_A + BW_B)/2$, and (4) $|f_{LOA} - f_{LOB}| > f_{IF} + (BW_A + BW_B)/2$. The frequency domain signal evolution in the concurrent dual-band receiver is also illustrated in Fig. 5. The proposed concurrent dual-band receiver can be viewed as a low-IF receiver for the signal of RF_A and a subharmonic direct-conversion receiver for the signal of RF_B. Therefore, both the receiver architectures have the advantage of low DC offsets [22, 25]. In addition, the flicker noise issues in low- and zero-IF CMOS receivers can also be mitigated by using passive mixers [26–29].

Experimental results

The proposed MMW hybrid mixer is fabricated using a standard TSMC 65-nm CMOS process. The photo of the chip is shown in Fig. 6 with a chip size of $0.69 \times 0.73\ \text{mm}^2$, including all pads and dummy metal. The mixer was measured via on on-wafer probing.

The measured and simulated CGs versus LO power level ($f_{LO} = 24$ GHz, $f_{IF} = 100$ MHz) for both SHM and FM modes of the mixer are shown in Fig. 7. It is observed that an LO power of 10 dBm is required for the SHM. Figure 8 shows the measured and simulated CGs versus RF frequency for both modes of the mixer. The maximum CG of the mixer is −13.7 and −7.6 dB for the SHM and FM modes, respectively, the 3-dB RF bandwidth is from 30 to 53 GHz and 16 to 35 GHz for the SHM and FM modes, respectively. The measured CGs of this mixer are considerably lower than that in [15], due to the following reasons: (1) the lack of IF buffers, which provide about 7-dB power gain in [15]; (2) the transconductance (g_m) of the transistors is lower than that in [15] due to $V_{DS} = 0$ V; (3) the quasi-diplexer also introduces 1.9-dB additional insertion loss, as shown in Fig. 2. The measured 3-dB IF bandwidth is 1.2 and 1.5 GHz for the SHM and FM modes, respectively. The measured LO-to-RF and 2LO-to-RF isolations are better than 40 and 58 dB, respectively, as shown in Fig. 9. The measured input 1 dB power compression point (IP_{1dB}) of the mixer is 4 and 6 dBm for the SHM and FM modes, respectively. A performance summary and comparison to other dual-band MMW mixers are shown in Table 1.

Table 1. Comparison of MMW dual-band mixers

Ref.	[16]	[15]	[30]	This work
Tech.	0.1-µm GaAs	65-nm CMOS	90-nm CMOS	65-nm CMOS
CG (dB)	−7 to −10 (43–63 GHz) −10.5 to −13 (55–85 GHz)	−0.1 ± 1.5 (17–43 GHz) −4.8 ± 1.5 (34–56 GHz)	−12 to −15 (6.5–20 GHz) −12 to −15 (12–33 GHz)	−7.6 to −10.6 (16–35 GHz) −13.7 to −16.7 (30–53 GHz)
P_{LO} (dBm)	>15	−3	12.6	10
P_{DC} (mW)	0	7	0	0
Dual-band concurrently?	No	No	No	Yes
IP_{1dB} (dBm)	N/A	−7.6 to −6.1	−3	4–6
Chip size (mm^2)	1.43	0.5	1	0.5

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Conclusion

In this paper, a millimeter-wave (MMW) fundamental and subharmonic hybrid dual-band CMOS mixer is proposed and presented. Based on a hybrid structure with two switching quads and a quasi-diplexer, the proposed mixer can function as an FM or a SHM. In addition, the hybrid mixer can also operate at two MMW bands concurrently as long as the frequency conversion schemes are carefully designed. This is very appealing for MMW systems to reduce the system size, increase the versatility, and/or extend the available bandwidth.

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