International Journal of Microwave and Wireless Technologies, 2011, 3(3), 355–364.
doi:10.1017/S175907871100033X

RESEARCH PAPER

Reconfigurable digital receiver design and application for instantaneous polarimetric measurement

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This paper presents the development of a reconfigurable receiver to undertake challenging signal processing tasks for a novel polarimetric radar system. The field-programmable gate arrays (FPGAs)-based digital receiver samples incoming signals at intermediate frequency (IF) and processes signals digitally instead of using conventional analog approaches. It offers more robust system stability and avoids unnecessary multichannel calibrations of analog circuits for a full polarimetric radar. Two kinds of dual-orthogonal signals together with corresponding processing algorithms have been investigated; the digital implementation architectures for all algorithms are then presented. Processing algorithms implemented in FPGA chips can be reconfigured adaptively regarding to different transmitted waveforms without modification of hardware. The successful development of such reconfigurable receiver extends our radar capacity and thus yields tremendous experimental flexibility for atmospheric remote sensing and polarimetric studies of ground-based targets.

Keywords: Radar signal processing and system modeling, Radar architecture and systems

Received 15 October 2010; Revised 14 February 2011; first published online 6 April 2011

I. INTRODUCTION

Polarimetric information can be used to improve the radar performance for target detection, identification, and parameters estimation. It has been widely used in many application areas such as terrain observation, disaster surveillance, and atmospheric remote sensing [1–3]. The full polarimetric nature of electromagnetic wave information can so be obtained by measuring the full polarimetric backscattering matrix (BSM) from a target by transmission and reception of two orthogonal polarizations. In this paper we focus our attention on two orthogonal linear polarizations, i.e. horizontal and vertical polarization. In the majority of existing radars with polarimetric capabilities, pulse-to-pulse based switching of the transmitted and/or received polarization is used to measure the elements of the scattering matrix and the BSM is measured in a sequence of two measurements. This introduces temporal, frequency, and phase ambiguities in the polarimetric results.

To overcome the limitation created by polarimetric switching, the PARSAX (Polarimetric Agile Radar for S- and X-bands) radar has been developed at IRCTR, TU Delft [1]. The PARSAX radar is a continuous wave (CW) radar system and provides the special capacity of simultaneous BSM measurement. It simultaneously transmits and receives periodic signals with dual-orthogonality both in polarimetric and in time–frequency spaces within the periodicity time interval. Such types of transmitted signals provide the unique possibility to split all elements of the BSM and to measure all of them simultaneously within one single periodicity time interval. The four complex elements of the BSM can be retrieved on reception by processing the received signals on each polarization channel with different reference signals. Many types of sophisticated signals taking the feature of orthogonality in time–frequency spaces have been investigated in [4, 5]. In the first stage of the PARSAX radar system development, special attentions are given to linear frequency modulated (LFM) and phase-code modulated (PCM) signals.

When utilizing dual-orthogonal signals for simultaneous BSM measurements, the receiver of the radar system must meet a series of requirements. First, the receiver should be able to receive and process two-channel signals at the same time, in order to provide accurate BSM estimation, all receiver channels must have the same characteristics in phase and amplitude. Second, owing to the volume of raw data produced by such radar cannot be efficiently stored, real-time processing is a must and the processor should therefore possess high-performance front-end signal processing capacity. In addition, since different kinds of orthogonal signals can be utilized in simultaneous BSM measurement, when transmitting different orthogonal signals, corresponding different algorithms should be applied to process the received signal and generate the

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estimated BSM, so the processor should be capable of performing all required receiver functions such as filtering and pulse compression, with regard to different types of transmitted signals. The receiver development becomes a challenging task for such full polarimetric radar.

In combination of state-of-the-art Analog-to-digital converter (ADC) techniques and reconfigurable computing techniques, a field-programmable gate arrays (FPGA)-based digital receive has been successfully developed for the PARSAX radar. The new receiver brings ADCs closer to the radar antenna, samples incoming signals at intermediate frequency (IF), and processes signals digitally instead of executing the signal processing in analogue devices, this simplifies the analogue circuits design and avoids multichannel calibrations for full polarimetric radar. The concept of reconfigurable computing has been deployed in the last few years at various levels utilizing different approaches. Current high-end FPGAs have been specifically designed to perform high-speed digital signal processing [6, 7], and are thus ideally suited to be the processor of reconfigurable fully digital receiver for our radar. The high-speed ADCs and high-performance FPGAs combined digital receiver allows for the features of broadband coverage, high performance real-time processing capacity, and multi-waveform adaptation. The processing algorithms and parameters programmed in FPGAs can be dynamically reconfigured according to different transmitted signals, thus yielding the maximum flexibility for the whole radar system.

The structure of the paper is the following. Section II introduces the basic principle of dual-orthogonal signal processing for simultaneous polarimetric measurements, followed by an overview of the PARSAX radar and hardware platform used for reconfigurable digital receiver. Section III presents two kinds of signals used in the current stage of PARSAX development, then the corresponding processing algorithms are theoretically studied, and it is shown how FPGA implementation architectures and digital interpretations of the processing output have been generalized. Section IV introduces the model-oriented FPGA design flow and the implementation feasibility and resource utilization study are presented. Section V includes conclusions and future plans.

II. PARSAX RADAR AND RECONFIGURABLE PROCESSOR

A) Simultaneous polarimetric measurement and signal processing

A technique using two separate transmitting channels for simultaneous scattering matrix measurement has been originally proposed in [5] and now applied in the PARSAX radar. Let $e_H(t)$ and $e_V(t)$ be two transmitted signals with duration T, simultaneously and separately transmitted with horizontal and vertical polarizations. The transmitted signal can be given in vector form by

$$\vec{e}_t(t) = \begin{bmatrix} e_H(t) \\ e_V(t) \end{bmatrix}. \tag{1}$$

In stationary scenarios, the received signal $\vec{e}_r(t)$ is the delayed version of the transmitted vector, and includes the polarization characteristics of target. It can be expressed as:

$$\begin{aligned} \vec{e}_r(t) &= \begin{bmatrix} e_{Hr}(t) \\ e_{Vr}(t) \end{bmatrix} = \begin{bmatrix} s_{HH} & s_{VH} \\ s_{HV} & s_{VV} \end{bmatrix} \begin{bmatrix} e_H(t-\tau) \\ e_V(t-\tau) \end{bmatrix} \\ &= \begin{bmatrix} s_{HH}e_H(t-\tau) + s_{VH}e_V(t-\tau) \\ s_{HV}e_H(t-\tau) + s_{VV}e_V(t-\tau) \end{bmatrix}, \end{aligned} \tag{2}$$

where $e_{Hr}(t)$ and eVr(t) represent received signal from horizontal and vertical polarization channel, respectively;

$$S = \begin{bmatrix} s_{HH} & s_{VH} \\ s_{HV} & s_{VV} \end{bmatrix}$$

is the full polarimetric BSM for single point target; τ is the round-trip propagation delay.

The simultaneous polarimetric signal processing aims at extracting the target BSM within one sweep for CW radar (or one pulse repetition for pulse radar). In the general case, to obtain an estimate of all BSM elements, both received signals $e_{Hr}(t)$ and $e_{Vr}(t)$ are then simultaneously processed in two separate branches with both the delayed replicas of $e_H(t)$ and $e_V(t)$, or equivalently, filtered by a couple of filters matched to $e_H(t)$ and $e_V(t)$ by the expression:

$$\begin{aligned} \vec{e}_r(t) * \vec{e}_t(t) &= \begin{bmatrix} e_{Hr}(t) \\ e_{Vr}(t) \end{bmatrix} * [\, e_H(t) \quad e_V(t) \,] \\ &= \begin{bmatrix} s_{HH}R_{HH}(\tau) + s_{VH}R_{VH}(\tau) & s_{HH}R_{HV}(\tau) + s_{VH}R_{VV}(\tau) \\ s_{HV}R_{HH}(\tau) + s_{VV}R_{VH}(t,\tau) & s_{HV}R_{VH}(\tau) + s_{VV}R_{VV}(\tau) \end{bmatrix}, \end{aligned} \tag{3}$$

where $R_{ij}(\tau)$ is the correlation function of two elements:

$$R_{ij}(\tau) = \int_0^T e_i^*(t) e_j(t+\tau) dt, \quad i, j = H, V. \tag{4}$$

Hence, $R_{HH}(\tau)$ and $R_{VV}(\tau)$ are the autocorrelation functions, $R_{HV}(\tau)$ and $R_{VH}(\tau)$ are the cross-correlation function of $e_H(t)$ and $e_V(t)$. The estimation of the BSM can be retrieved from the four elements of equation (3). If $R_{HV}(\tau)$ and $R_{VH}(\tau)$ satisfy the condition

$$R_{HV}(\tau) = R_{VH}(\tau) = 0, \tag{5}$$

the four-channel outputs of equation (3) provide a precise estimation of the BSM. Equation (5) expresses the signal orthogonality requirement, which typically requires a proper waveform selection of the transmitted signals. In practice, the ideal condition of (5) can only be met approximately. The isolation problem in case of one point target has been studied in [1, 4], the isolation (I) parameter to estimate cross-channel isolation level is defined as

$$I_i \triangleq \min_{\forall \tau} \left[20 \log_{10} \frac{|R_{ii}(0)|}{|R_{ij}(\tau)|} \right], \quad i, j = 1, 2, \tag{6}$$

where $R_{ii}(\tau)$and $R_{ij}(\tau)$ are the autocorrelation and cross-correlation functions of the transmitted signals, the index denotes the waveform that is considered between those

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simultaneously transmitted signals. The isolation I is a measure for protection from the maximum residual "cross-channel" return owing to either the same target or owing to an interfering target.

B) PARSAX radar architecture

Applying the principle described above, the PARSAX radar has been developed by IRCTR, TU Delft to provide a unique simultaneous BSM measurements capacity – the four elements in BSM can be retrieved within one sweep, instead of using polarimetric switching in two sweeps or pulses for the majority of existing full polarimetric radar.

Taking advantages of start-of-the-art microelectronics and digital processing techniques, the PARSAX radar established a novel software-defined architecture as depicted in Fig. 1. In the main operational mode, the radar will be used for atmospheric remote sensing, polarimetric studies of ground-based targets, and sea clutters. These tasks have to be solved in the framework of different missions and in variable scenarios, environment, and weather conditions. Such requirements cannot be satisfied with traditional fixed radar architecture. In our software-defined radar architecture, the wideband arbitrary waveform generator (AWG) is selected as the signal source to generate a pair of transmitted orthogonal signals; the FPGAs in digital receiver are programmed with suitable algorithms to undertake data processing tasks. Owing to the reconfigurable features of AWG and FPGAs, both transmitted waveforms and corresponding processing algorithms can be run-time reconfigured and adaptive with different mission and scenarios, thus yielding tremendous experimental flexibility for scientific research.

Figure 1 depicts the simplified block diagram of the PARSAX radar, the whole system operates as follows. A pair of selected orthogonal signals $e_H(t)$, $e_V(t)$ are generated at IF from the AWG. According to the orthogonality requirements, these two signals are digitally calculated in advance and can be changed at software level. Signals $e_H(t)$ and $e_V(t)$ are up-converted to the S-band (carrier frequency of 3 GHz) in two radio frequency (RF) channels, the horizontal (H)-channel and vertical (V)-channel, respectively. The up-converted signals are then loaded to the feeders of the transmitting antenna through an ortho-mode transducer (OMT) and simultaneously transmitted.

On the receiver site, the signals $e_{Hr}(t)$ and $e_{Vr}(t)$, as the outputs of the RF blocks of the H-channel and V-channel, are amplified by low noise amplifiers (LNA) and down converted from RF to IF. The amplitudes and phases of $e_{Hr}(t)$ and $e_{Vr}(t)$ describe the orthogonally polarized components of the received field. The reconfigurable multichannel digital receiver, shown within the dotted line in Fig. 1, is composed of four synchronized sub-processing branches; An estimate of all BSM elements can be obtained after both received signals, $e_{Hr}(t)$ and $e_{Vr}(t)$, are simultaneously processed by four separate sub-processing branches using different reference signals. The processing which is configured in sub-processors can be scene-adaptive to employ algorithms appropriate for any given waveforms and signal parameters.

C) Reconfigurable receiver hardware architecture

FPGAs have become a popular implementation technology for radar signal processing because they offer a combination of high performance, low cost, and flexibility. In simplest term, FPGAs are composed by large arrays of look-up tables, Digital signal processing (DSP) slices, and memory blocks with flexible interconnects which allow building complex circuits for data processing or logic control. Because of their in-system reconfigurability, a FPGA-based reconfigurable platform has been selected for the PARSAX radar to receive the IF sample data from ADCs, to undertake real-time processing tasks and to transfer the processed data to the host computer.

Each sub-processing branch illustrated in Fig. 1 is composed by one FPGA-based reconfigurable digital signal processing board using the latest technology. The block diagram of the board is shown in Fig. 2. Two A/D converters are 14-bits devices with sampling rates up to 400 MSPS, the sampling clock is synchronously provided from the RF block of the radar system. Data acquisition and processing for each sweep is started by the external trigger signal which is generated by the given frequency reference and synchronized with the AWG and other parts of the radar. The FPGA chip Virtex5SX95T from Xilinx has high computation power and can be configured with different processing algorithms which are customized designs and can so be implemented. Processed data can be transported to the host computer via the PCI-E bus for post-processing and visualization, two DDR2 DRAM banks are used as data buffer between FPGA and PCI-E bus. Our processing board for each channel contains two ADCs; both the received and the reference signals can be sampled and processed. Since reference signal is digitally calculated and generated from an AWG, the

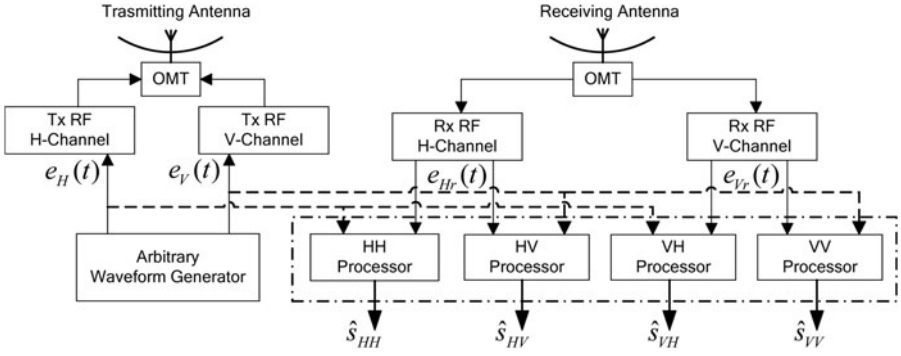

Fig. 1. PARSAX radar block-diagram.

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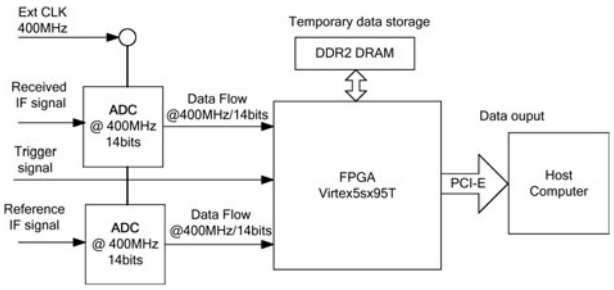

Fig. 2. Hardware platform for each sub-processor.

reference digital sequence can also be stored in the memory blocks of FPGA chip, and then only the received signal need to be sampled. This alternative will consume more memory resources in the FPGA chip, and the pre-stored reference information need to be updated according to different transmitted waveforms.

The whole reconfigurable receiver diagram composed of four FPGA boards is illustrated in Fig. 3. All the four boards work in parallel and are placed in one ASUS P677WS Supercomputer motherboard. In comparison with conventional analog processing approaches, the digital processing boards for the PARSAX radar avoid unnecessary multichannel calibrations of analog hardware owing to component drifts with time and temperature. This results into more robust system stability and thus an improved system performance. The FPGA-based architecture also provides the flexibility to implement digital down-conversion, in-phase and quadrature (I/Q) demodulation, and subsequent waveforms specific algorithm, without modification of the hardware platform.

III. WAVEFORM AND PROCESSING ALGORITHM SELECTION

Different types of sophisticated signals taking the feature of orthogonality in time–frequency can be employed for simultaneous BSM measurements. In the first operational stage of the PARSAX radar, two kinds of signals, (1) linear frequency modulation (LFM) signals with opposite modulation slope and (2) orthogonal phase coded modulation (PCM) signals, have been employed. Related processing algorithms have been designed according to signal specifications, and can be reconfigured in FPGA chips adapting to different transmitted waveforms.

A) LFM Mode and de-ramping processing

A pair of LFM signals with opposite modulation slopes approximately subjects the condition in equation (5), thus can be used for simultaneous BSM measurement. The transmitted signal vector composed of two LFM signals can then be written as:

$$\vec{e}_t(t) = \begin{bmatrix} e_H(t) \\ e_V(t) \end{bmatrix} = \begin{bmatrix} \exp\left(j2\pi(f_c t + \frac{1}{2}\alpha t^2)\right) \\ \exp\left(j2\pi(f_c t - \frac{1}{2}\alpha t^2)\right) \end{bmatrix}, \quad -\frac{T}{2} < t \le \frac{T}{2}, \tag{7}$$

where $e_H(t)$ and $e_V(t)$ are the up-going and down-going LFM signals, f_c is the IF carrier frequency, t is the time variable varying within the pulse-repetition time (PRT) T, and α is the frequency sweep rate equal to the ratio between the transmitted bandwidth B and the PRT.

1) DE-RAMPING PROCESSING

LFM signals can be processed using one multiplication with a matched reference signal. The range information can then be resolved using spectral analysis of the product. This technique is called "de-ramping compression processing" [8].

Figure 4 shows a simplified scheme of the de-ramping algorithm for polarimetric radar with simultaneous measurement of BSM. In order to obtain the estimations of all BSM elements, each of the received signals ($e_{Hr}(t)$, $e_{Vr}(t)$) is mixed with the conjugated replicas of the transmitted

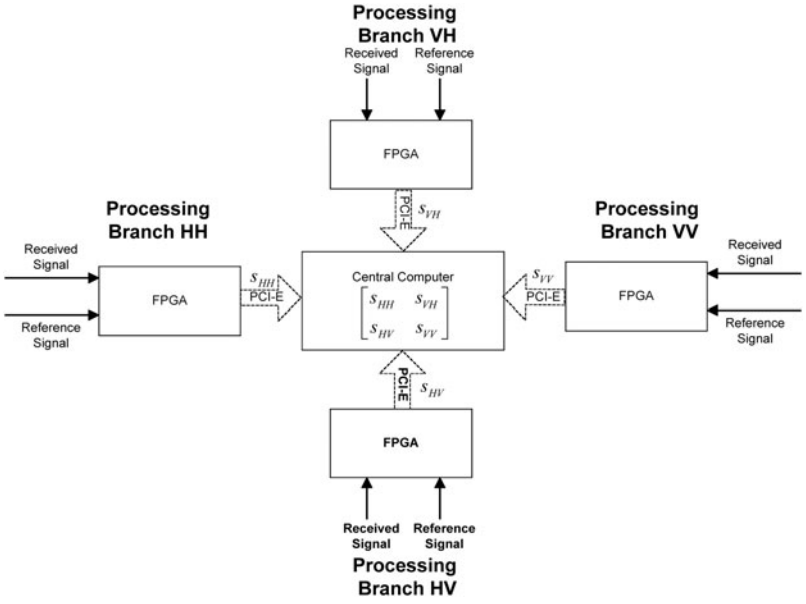

Fig. 3. Reconfigurable receiver diagram for the PARSAX radar.

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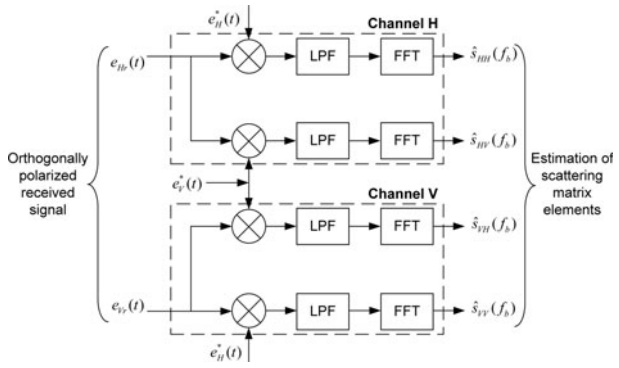

Fig. 4. Multichannel de-ramping processing.

waveforms ($e_H(t)$, $e_V(t)$) and is reduced in slope, i.e. the signals are de-ramped. The signals after multiplication and low-pass filtering (LPF) are called the beat signals. By applying a Fourier transform (i.e. the fast Fourier transform – FFT) onto the beat signals, the resulting spectrum as a function of beat frequencies (f_b) for each ramp corresponds to range profiles for all four elements of the scattering matrix. The processing is summarized by

$$\begin{bmatrix} \hat{s}_{HH}(f_b) & \hat{s}_{HV}(f_b) \\ \hat{s}_{VH}(f_b) & \hat{s}_{VV}(f_b) \end{bmatrix} = FFT\left[LPF\begin{bmatrix} e_{Hr}(t)e_H^*(t) & e_{Hr}(t)e_V^*(t) \\ e_{Vr}(t)e_H^*(t) & e_{Vr}(t)e_V^*(t) \end{bmatrix}\right], \quad t \in [\tau_{max} \ldots T], \tag{8}$$

where FFT means Fast Fourier transform, τ_{max} is maximum time delay of the received signal and T is the LFM-signals' sweep time which equals the duty cycle of the radar with continuous waveforms. Beat frequencies are analyzed in the frequency band $(0 \ldots f_{bmax}]$. The maximum beat frequency (f_{bmax}) is defined in the LPFs and determines the maximum time delay (τ_{max}) and therefore, the maximum observed range (R_{max}).

2) DIGITAL DE-RAMPING ARCHITECTURE

When the de-ramping processing is performed in digital domain, both received the signal and the reference signal is sampled in discrete number and processed digitally. The processing diagram of one digital de-ramping branch is shown in Fig. 5. When conducting IF sampling, the ADC sampling frequency f_s is determined by the LFM bandwidth B and IF carrier frequency f_c according to Nyquist sampling theorem. One such received signal and reference signal are digitized in discrete samples and expressed as $e(n)$ and $e_r(n)$,

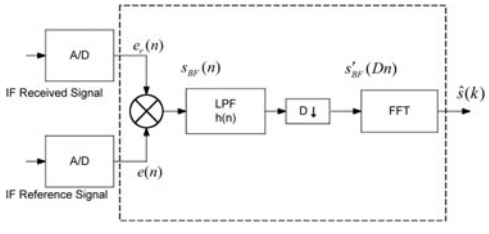

Fig. 5. Digital de-ramping processing implementation diagram.

respectively. After the multiplication of these two signals, the digitized beat frequency signal $s_{BF}(n)$ is generated; the maximum frequency f_{bmax} in $s_{BF}(n)$ is proportional to the maximum range of observation.

When $f_{bmax} << f_s/2$, the digitalized beat frequency signal $s_{BF}(n)$ is over sampled, a decimation operation can be performed to reduce the data rate and data volume for further processing. Before decimation, it is necessary to ensure that the re-sampling will not introduce new aliasing signals, so a LPF has to be implemented as $f_{stop} = f_{bmax}$, where f_{stop} is the stop band of the filter. In order to avoid aliasing the maximum decimation rate D must meet the condition:

$$D < \frac{f_s}{2f_{bmax}}, \tag{9}$$

where f_s is the IF sampling frequency. The input signal for the N points FFT is the D-time decimated beat frequency signal which is expressed as $s'_{BF}(Dn)$ in Fig. 5. The processing output sequence $\hat{s}(k)$ in frequency domain covers the frequency from 0 to $f_s/(2{\cdot}D)$. According to LFM signals' time–frequency relationship defined from equation (7), the frequency information existing in beat signal $s'_{BF}(Dn)$ is proportional to range information from targets, thus the corresponding range span covered by de-ramping processing is

$$\left[0, \frac{cf_sT}{4DB}\right]. \tag{10}$$

The range profile covering above range span is composed by N discrete numbers, thus the digitalized range resolution is

$$\Delta R_d = \frac{cf_sT}{4DBN}. \tag{11}$$

B) Phase code modulation (PCM) signals mode and related processing algorithms

A pair of orthogonal signals with PCM has been recognized as another promising solution for simultaneously scattering matrix measurements [5]. The carrier frequency of transmitted PCM signal is modulated by the phase-code sequence at a given fixed rate (chip rate), so the whole signal is divided into a number of chips with equal duration ΔT. The chip rate Δf is the reciprocal of ΔT, and determines the bandwidth of PCM signals. The cross-correlation level for PCM signals is lower than LFM signals when the Bandwidth-time (BT)-products are equal. Besides, there is no range-Doppler coupling for PCM signals in comparison with LFM signals. So PCM signals are preferable in scenarios with fast moving targets [1].

PCM signals are applicable to correlation processing and matched filter processing and cannot be applied to de-ramping processing. For this reason, our selected FPGA implementation architecture and feasibility study for correlation processing and matched filter processing are summarized in the following.

1) CORRELATION PROCESSING

When applying correlation processing in polarimetric radar, in order to obtain the estimations of all BSM elements, the

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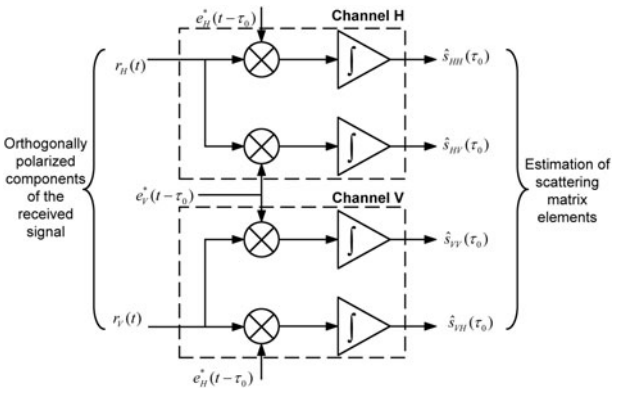

Fig. 6. Multichannel correlation processing.

orthogonally polarized components of the received signal are simultaneously correlated in separate branches with the delayed replicas of $e_H(t)$ and $e_V(t)$, as shown in Fig. 6. The processing of the received signals with orthogonal polarizations ($e_{Hr}(t)$ and $e_{Vr}(t)$) takes place in channels H and V, respectively.

The receiver calculates the correlation integral between the received vector signal, $\vec{e}_r(t) = \left[e_{Hr}(t) \quad e_{Vr}(t) \right]^T$, and conjugated transmitted signals $e^*(t-\tau_0) = \left[e_H^*(t-\tau_0) \; e_V^*(t-\tau_0) \right]^T$, with the expected time shift, τ_0, the superscript T denotes transpose of the vector. We derive

$$\begin{bmatrix} \hat{s}_{HH}(\tau_0) & \hat{s}_{HV}(\tau_0) \\ \hat{s}_{VH}(\tau_0) & \hat{s}_{VV}(\tau_0) \end{bmatrix} = \begin{bmatrix} \int_{\tau_0}^{\tau_0+T} e_{Hr}(t) e_H^*(t-\tau_0) dt & \int_{\tau_0}^{\tau_0+T} e_{Hr}(t) e_V^*(t-\tau_0) dt \\ \int_{\tau_0}^{\tau_0+T} e_{Vr}(t) e_H^*(t-\tau_0) dt & \int_{\tau_0}^{\tau_0+T} e_{Vr}(t) e_V^*(t-\tau_0) dt \end{bmatrix}, \tag{12}$$

where τ_0 is constant, $\hat{s}_{ij}(\tau_0)$, $i, j = H, V$, are the estimations of the BSM for a predetermined (expected) time delay τ_0, which is a constant for one measurement, T is the transmitting signal duration (CW radar duty cycle). The integrals are calculated within the time interval $[\tau_0 \ldots \tau_0 + T]$. The boundaries for integration are fixed because the signals are assumed to be synchronized with each other and all having T-duration.

The digital correlation-processing diagram is shown in Fig. 7. When the correlation processing is implemented in digital domain, the integration processing indicated in equation (12) can be realized by a discrete multiplier followed by an accumulator with accumulation time interval of T. Since the correlation processing can be applied at base band without regarding the carrier frequency, the digital down converter (DDC) can be firstly implemented to convert the IF digitalized received signal $e_r(n)$ and the reference signal $e(n)$ into base band. The decimation operation can then be followed to reduce the data rate and volume. The decimation rate D in such case is determined by the chip rate Δf of PCM signals, and must meet the condition

$$D < \frac{f_s}{2\Delta f}, \tag{13}$$

where f_s is the IF ADC sampling frequency.

The signals generated after DDC and D-time decimation are shown as $e(Dn)$ and $e_r(Dn)$ in Fig. 7. The initial time-delay τ_0 indicated in (12) are realized via initial delay register in the digital domain, the delay clock cycles N_0 is determined by

$$N_0 = \frac{\tau_0 f_s}{D}. \tag{14}$$

In order to cover a certain range span, a series of such multiplier–accumulators should be applied. The time delay between each multiplier–accumulator can be realized via serial shift registers. Assuming the stepped delay time is N clock cycles between two shift registers, the time delay created by this register is

$$\Delta t = \frac{ND}{f_s}. \tag{15}$$

The corresponding digitalized range step is

$$\Delta R_d = \frac{cND}{2f_s}. \tag{16}$$

equation (15) stands for the time differences between each digitalized range bin. On the other hand, the radar range resolution determined by signal bandwidth B is expressed by

$$\Delta R = \frac{c}{2B}. \tag{17}$$

To guarantee that there is no resolution degradation after digitalization, N, determined by equations (16) and (17) should satisfy the condition of:

$$N \le \frac{\Delta T f_s}{D}. \tag{18}$$

Assuming the initial delay time is N_0 clock cycles and the stepped delay time is N clock cycles, the output sequence of correlation processing $\hat{s}(m)$ is given by

$$\hat{s}(m) = \sum_{n=1}^{DT/f_s} r(Dn - N_0 - Nm) e(n), \quad m = 0, 1, \ldots, M-1, \tag{19}$$

where M is the total number of stepped shift registers, determined by the interested range span and limited by the computational resources in chosen FPGA chip. The corresponding range span covered by the digital correlation processing equals

$$\left[\frac{cN_0D}{2f_s}, \frac{cN_0D}{2f_s} + \frac{cNMD}{2f_s} \right]. \tag{20}$$

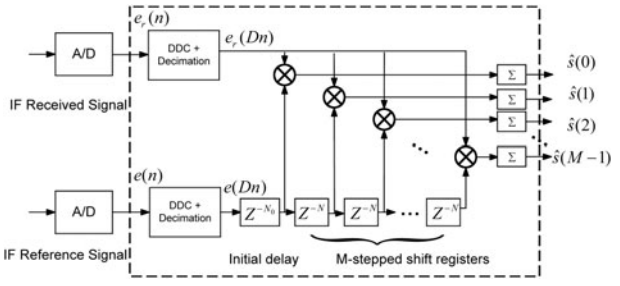

Fig. 7. Digital correlation processing implementation diagram.

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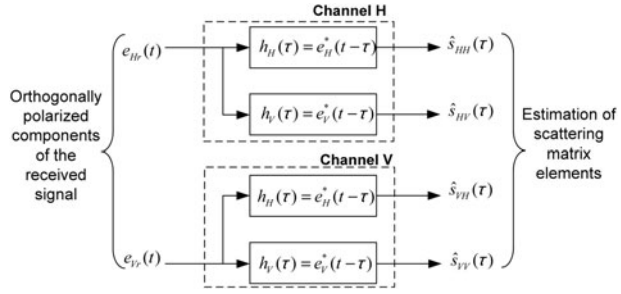

Fig. 8. Multichannel matched filter processing.

2) MATCHED FILTER PROCESSING

By definition the matched filter is a filter which, for a specified signal waveform, will result in the maximum attainable signal-to-noise ratio at the filter output when both signal and additive white Gaussian noise have passed the filter [9]. The idea behind the matched filter is correlation using convolution [10]. For polarimetric radar with simultaneous measurement of BSM elements, the receiver processing includes four matched filters as depicted in Fig. 8, whose impulse responses ($h_H(\tau)$ and $h_V(\tau)$) are the time-reverse conjugate of the vector sounding signal components ($e_H(t)$ and $e_V(t)$).

The estimations of the scattering matrix elements in case of matched filtering for polarimetric radar with continuous waveforms are calculated from

$$\begin{bmatrix} \hat{s}_{HH}(\tau) & \hat{s}_{HV}(\tau) \\ \hat{s}_{VH}(\tau) & \hat{s}_{VV}(\tau) \end{bmatrix} = \begin{bmatrix} \int_0^T e_{Hr}(t)e_H^*(\tau - t)dt & \int_0^T e_{Hr}(t)e_V^*(\tau - t)dt \\ \int_0^T e_{Vr}(t)e_H^*(\tau - t)dt & \int_0^T e_{Vr}(t)e_V^*(\tau - t)dt \end{bmatrix}. \quad (21)$$

As expressed in (21), matched filter processing is equivalent to convolving the received signals with a conjugated time-reversed version of the reference signal (cross-correlation). It can be implemented computationally efficient in frequency domain based on the convolution theorem [11].

Figure 9 shows our digital matched filter processing implementation diagram. Using the principle that multiplication in the frequency domain corresponds to convolution in the time domain. Both received signal and reference signal are transformed into the frequency domain using the FFT, multiplied in frequency domain after conjugation for reference signal, and then transformed back into the time domain using the Inverse FFT. In order to implement matched filter processing in real time, the same DDC and decimation processing are used to reduce the data rate and processing intensity. So the implementation of the matched filter in frequency domain can be expressed by

$$\hat{s}(Dn) = IFFT[FFT(e_r(Dn))conj(FFT(e(Dn)))], \quad (22)$$

where $e_r(Dn)$ and $e(Dn)$ represent the received signal and reference signal after DDC and D-time decimation.

In CW radar case, if both the received signal and the reference signal is sampled in the whole duty cycle T, the length of the FFT is thus determined by the IF sampling frequency f_s and decimation rate D, thus the FFT length and inverse FFT length N_{FFT} can be expressed by

$$N_{FFT} = \frac{Tf_s}{D}. \quad (23)$$

For the same processing length, the time-domain processing requires on the order of $N_{FFT}{}^2$ operations (multiplications and additions), while frequency-domain processing composed by two FFT and one inverse FFT requires on the order of $3N_{\mathrm{FFT}}\lg(N_{\mathrm{FFT}})$ operations, where $\lg(N_{\mathrm{FFT}})$ denotes the logarithm-base-2 of N_{FFT}. For processing length longer than 64 points, the frequency processing is more efficient than the time-domain processing [10], thus, the frequency-domain matched-filter processing consumes less computational resources for FPGA implementation.

The matched-filter processing output $\hat{s}(Dn)$ is the discrete sequence with the length of N_{FFT}, it stands for time interval from 0 to T; so the range span covered by matched-filter processing equals

$$\left[0, \frac{cT}{2}\right]. \quad (24)$$

The range profile covering the whole range span is composed by N_{FFT} discrete numbers, thus the digitalized range resolution can be generalized from (23) and (24) as

$$\Delta R_d = \frac{cD}{2f_s}. \quad (25)$$

In order to make sure there is no range resolution degradation after digitalization, the decimation rate D should meet the following conditions:

$$D \le \frac{f_s}{2B}. \quad (26)$$

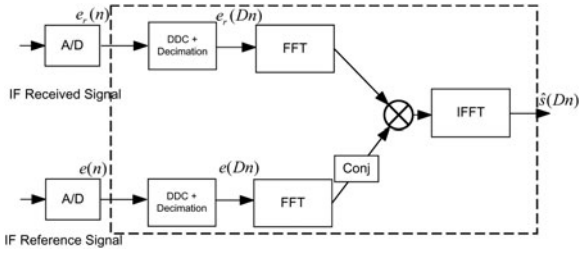

Fig. 9. Digital matched filter processing implementation diagram.

IV. FPGA IMPLEMENTATION PROCEDURE AND FEASIBILITY STUDY

A) FPGA implementation

Traditional FPGA design flows have historically mirrored processes originally developed for building application specific integrated circuits (ASICs), the algorithms are typically described in a hardware description language (HDL) like

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VHDL or Verilog. In contrast, a model-oriented FPGA design flow has been established to develop the algorithms described above for the PARSAX radar, all algorithms are modeled by high-level blocksets in system generator environment instead of writing raw HDL codes.

The general procedure for our FPGA implementation is illustrated in Fig. 10. The whole FPGA design task is divided into two parts from initial stage: the algorithm design and peripheral interface design. The left branch in Fig. 10 illustrates the design flow for model-oriented algorithm design; all signal processing algorithms following the FPGA implementation architecture and described in Figs 5, 7 and 9 are firstly modeled in the system generator; then two times packaged ASCII netlist (NGC) file can be generated. The right branch in Fig. 10 shows the board-related peripheral interface design flow; all hard-wire connection and control logics between FPGA and other peripheral chips are described by VHDL, the compatible NGC file is generated after VHDL synthesis. These two NGC-files are then joined together for further NGC building processing, after a chip-dependent place and route (PAR) processing in Xilinx ISE® ISE is the name of the software tool from Xilinx Company design tool suite, the final bitstream file can then be generated and downloaded to FPGA.

Following the implementation procedure depicted in Fig. 10, each algorithm finally generates a standalone bitstream file. Each bitstream file can then be used to configure the FPGA chip to conduct different signal processing task.

For the algorithm design, the system generator-based high-level design approach provides increased productivity, especially greater ability to explore architecture and debug complex algorithms realized in hardware; for peripheral interface design, in order to meet critical timing constrains, this part of the design is described by low-level VHDL codes. The established design procedure separates the algorithm design from peripheral interface design using different design methodologies, thus increases the reliability and efficiency for FPGA implementation.

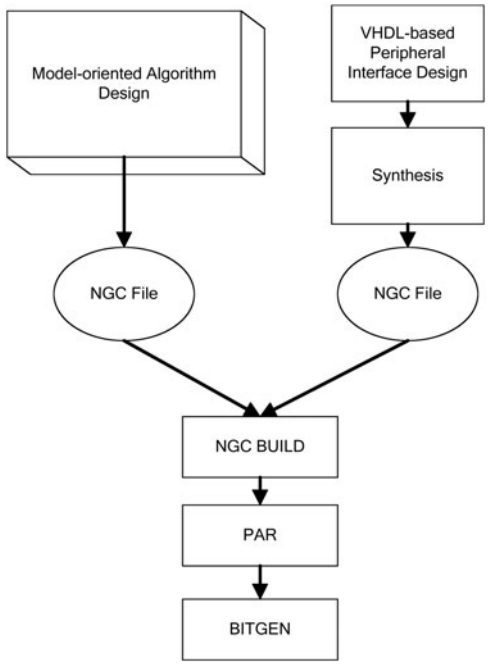

Fig. 10. Model-oriented FPGA design procedure.

B) Resource utilization and feasibility study

All the above investigated waveform sets form a "waveform library" for the PARSAX radar, while all algorithms compose an "algorithm library". As soon as scenario preferred waveform sets are selected to configure the AWG, the bitstream file containing corresponding processing algorithm can then download into FPGA chips and reconfigure the digital receiver to conduct different signal processing tasks. Such fast reconfigurable feature from waveforms to processing algorithms tremendously extends the radar capability and flexibility.

Nevertheless, correlation processing and matched-filter processing can also be applied to LFM signals [8]. De-ramping processing for LFM signals and correlation/matched filter processing for PCM signals have been tested and validated with the specified FPGA implementation architecture, the corresponding bitstream files are generated following the design procedure illustrated in Fig. 10. One FPGA chip of Xilinx Virtex5sx95T is used for the feasibility study and responsible for one channel's data processing. Regarding the PARSAX radar signal specifications ($f_s =$ 400 MHz, $f_c = 125$ MHz, $B = 50$ MHz) and FPGA computational resources, the processing parameters and capacities for different waveforms are summarized in Table 1.

For the de-ramping processing with 400 MHz IF sampling frequency, the anti-aliasing LPF with 512 taps is applied to select 5 MHz from beat frequency, then 22-time decimation can be applied to reduce the data volume, the FFT length for time–frequency conversion is 16K, the generated range profile covers the range spectra from 0 to 15 km; For the correlation processing and matched filter processing, the LPF stop band's decimation rate is limited by signal bandwidth $B = 50$ MHz, 64-tap LPF is applied after converting the IF signals to base band and the maximum decimation rate is 3. Because of relatively low decimation rate for the correlation processing and the matched filter processing, the data volume for these two processing is increased in comparison with the de-ramping processing, the observation range for correlation processing is 750 m and limited by the computational resources in FPGA, while maximum FFT length for matched filter processing is 8K and limited by the memory resources in FPGA. Figure 11 shows the physical FPGA resource utilization for each algorithm.

The logic resources and computational resources in Xilinx Virtex4 FPGA can be divided into four categories: basic flip-flops, logic slice composed by look-up table, Block RAMs, and DSP slices composed by dedicated multiplier–accumulator for signal processing. As depicted in Fig. 11, in the de-ramping algorithm, it averagely consumes approximate 50% of the FPGA recourses, DSP slices are mainly used for

Table 1. Processing algorithms comparison for the PARSAX radar.

	De-ramping	Correlation	Matched filter
Applicable waveform	LFM	LFM, PCM	LFM, PCM
FIR taps	512	64	64
Decimation rate	22	3	3
FFT length	16 K	–	8 K
Observation range	0–15 km	0–750 m	0–18.75 km

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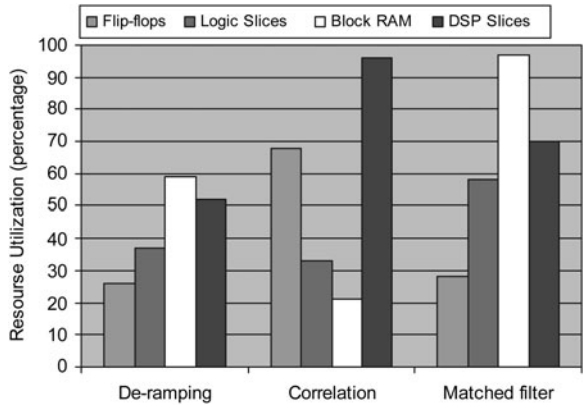

Fig. 11. Resource utilization on Virtex4sx95t FPGA.

long-tap FIR filter and FFT, block RAMs are consumed for frame data storage for 64K FFT. In the correlation algorithm, each correlation tap contains one 18-bits multiplication and one summation; the overall DSP slices in one FPGA chip can only afford 250 correlation taps thus the range coverage is limited by this fact; in addition, because the need for a shift-register between two correlation taps, the correlation processing also consumes more flip-flops in comparison with the two other algorithms. In the matched filter algorithm, the major limitation is the block RAMs, since two FFTs and one IFFT processing are all frame-based, so data buffers must be created between input data and FFT processing core, thus the matched filter consumes more memory resources, the data flow control for the matched filter algorithm is more complicated than for the other two algorithms, and as a result, it consumes relative more logic slices.

According to the analysis from Table 1 and Fig. 10, the de-ramping processing offers the best computational efficiency and the observation range can be easily configured according to user's requirements. However, it is only applicable for LFM signals [12]. The correlation processing and matched filter processing can be applied to all pulse-compression waveforms but consumes more computational resources, especially the correlation processing in time domain. The feasibility study of R. Fratila [13] shows that when even using all DSP resources within one chip of the FPGA, the observation range can be only around 750 m for the PARSAX radar. However, the observation range spectra and digitalized resolution of correlation processing can be easily configured by changing the initial delay and delay step between shift registers, this feature can be useful when the radar operates to cover different range spectra using different range resolution. Matched-filter processing illustrated in Fig. 9 reduced the computational resources by transforming from time domain to frequency domain, but the implementation architecture is relatively complicated and it consumes more memory resources in comparison with other two processing algorithms.

V. CONCLUSIONS

This article outlines the work on the design of a reconfigurable receiver for the PARSAX radar. In combination with the start-of-the-art microelectronics and digital processing techniques, the PARSAX radar established novel software-defined architecture. Based on software-defined architecture, both transmitted waveforms and corresponding processing algorithms can be run-time reconfigured without any hardware modification, thus the whole radar system is adaptive with different mission and scenarios. An FPGA-based multichannel reconfigurable digital receiver has been developed to undertake the high throughput real-time data processing tasks. In comparison with conventional analog processing approaches, the digital processing boards for the PARSAX radar avoid unnecessary multichannel calibrations of analog hardware owing to component drifts with time and temperature, this result into a more robust system stability and thus an improved system performance.

De-ramping processing for LFM signals, correlation processing, and matched filter processing for PCM signals with suitable FPGA implementation architectures has been analyzed in detail. The advantages and disadvantages for each algorithm have been generalized based on the results from our FPGA implementation feasibility and recourse utilization study. Each proposed processing algorithm forms a downloadable bitstream file, which is ready to configure the FPGA chips in different scenarios and adaptive to different transmitted waveforms.

ACKNOWLEDGEMENTS

At the International Research Centre for Telecommunications and Radar (IRCTR), Delft University of Technology a major research project PARSAX is executed concerning the design and development of full polarimetric FM–CW radar with dual-orthogonal signals for simultaneous measurement of all elements of radar target's polarization scattering matrix. This project is performed under a contract with the Dutch Technology Foundation STW.

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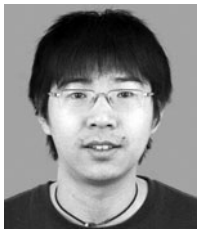

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