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Low-cost TRM technologies for phased array radars

HÅKAN BERG, HEIKO THIESIES AND NIKLAS BILLSTRÖM

Low-cost enabling technologies for T/R modules (TRMs) in phased array radars are proposed and analyzed in terms of technology, performance, and cost aspects. Phase and amplitude controlling integrated circuits (ICs) realized in a low-cost standard silicon process are demonstrated. The design of several ICs at the S-, C-, on X-band has shown that silicon germanium is a strong contender for gallium arsenide. This also applies to TRMs suited for military active phased array antenna (AESA) radars. The circuits presented in this paper are manufactured by austriamicrosystems in their 0.35 μm SiGe-BiCMOS process with an f_T of around 70 GHz. A TRM packaging concept based on soldered surface-mount technology and organic substrates is also demonstrated. A cost analysis concludes that by using the proposed packaging concept and the SiGe core-chip technology, the TRM production cost can be potentially reduced by 70% compared to traditional ceramic hermetic packaging with core chip in GaAs technology.

Keywords: BiCMOS integrated circuits, MMICs, Phased array radar, Multichip modules, Surface mounting, Printed circuits, Life cycle costing

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I. INTRODUCTION

Active phased array antennas (AESAs) have been on the agenda for military radar application since the early 1980s. Several systems have been launched since then but, in general, the development has been much slower than expected due to the added complexity of technology andalso due to the very high manufacturing cost of the active antenna.

The experience so far is that the number of T/R modules (TRMs) per system and the TRM unit production cost are crucial parameters with respect to both purchase price and life cycle cost (LCC). Investigation of "new/alternative" low-cost technology concepts for TRMs is therefore essential. The forthcoming analysis of this paper will address two such low-cost enabling technologies:

- SiGe monolithic microwave integrated circuit (MMIC) core chip.
- Non-hermetic surface-mount TRM packaging.

Saab Microwave Systems have considerable experience in designing MMICs for radar application TRMs. Low noise amplifiers (LNAs), so-called core chips, power amplifiers, and low-cost SiGe ICs have been developed [1, 2]. Silicon-based processes have shown very good results as far as environmental durability is concerned.

If the architecture in Fig. 1, with LNA and power amplifiers outside the core chip, is used for the TRM, the noise figure and output power are less crucial for the core chip itself. This makes it possible to use silicon germanium to realize core functionality while optimal technologies, e.g. GaAs and GaN, can be chosen for LNA and High power amplifier (HPA), thereby optimizing the overall noise figure and power added efficiency. This has been considered for phased array radar applications for some time [1–5].

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II. TRM PACKAGING TECHNOLOGY

A) TRM packaging cost analysis

For TRMs two main packaging concepts, defined below, were investigated and compared:

1) *MIL*: traditional "hybrid" technology using bare dies, ceramic substrates, and brazed/welded metal frames and lids providing hermeticity. This is the workhorse in existing systems of radar TRMs today at the C- and X-band.
2) *SMT*: soldered surface mount components using standard plastic mold packages (QFN, TSSOP) on organic substrates. Low-cost SMD enclosures are used for EMC and mechanical protection (non-hermetic). SMT technology today is mainly driven by high-volume consumer applications and is used up to at least 30 GHz in telecom applications.

These two concepts are further conceptually depicted in Fig. 2, and the SMT option is also demonstrated for an X-band TRM in Fig. 1. The concept of TRM packaging has been studied at Saab Microwave Systems for several years in national projects [6] and EDA projects such as MIMOSA [7] and STAMP [8].

Until recently, the SMT option has not been viable for military microwave sensors/radars because of low-cost robust standard chip packages that have not been available for these applications. However, today plastic molded packages in combination with rugged chip passivation are provided by several major SiGe and GaAs foundries.

An important issue is whether the ruggedness of non-hermetic TRMs will be adequate for harsh military

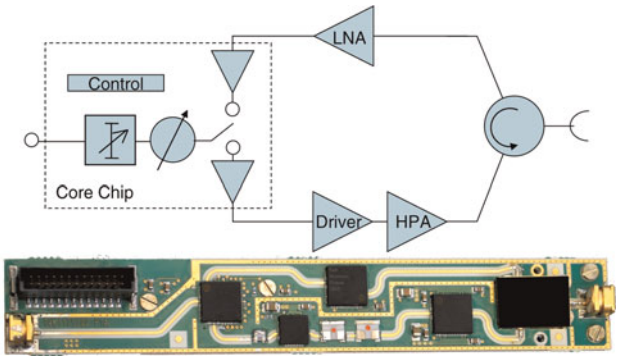

Fig. 1. Example of a low-cost TRM based on packaged ICs together with basic functional architecture.

applications. Environmental investigation in the previously mentioned projects indicates that the answer to this question is yes. Depending on application and system concept, some additional "climatization" measures might be necessary at a higher mechanical/enclosure level. However, the cost of these measures is believed to be rather insignificant compared to the savings achieved for TRMs.

Regarding RF performance, the two packaging concepts are more or less equivalent up to at least 18 GHz.

III. TRM COST ANALYSIS

A) TRM packaging

1) PREREQUISITES

The first step in the analysis was to set up reasonable prerequisites for the analysis. For the initial analysis of packaging concepts, all RF functions were based on GaAs MMIC technology except for the drop-in circulator. The analysis was performed for a C-band TRM. The comparison was based on the following prerequisites:

- C-band radar application (1 GHz system BW, ~8 W of peak output power).
- *Substrate*: Dupont951 Low temperature cofire ceramic (LTCC) for the MIL TRM and Ro4350 with FR4 core for the SMT TRM. The estimation also accounts for the fact that the SMT TRM will become 20% larger due to the added circuit board area needed for packaged MMICs.
- *Mechanics*: Brazed carrier + lid + frame for MIL and soldered carrier + lid for SMT.
- *Chip/MMIC (Lim/LNA/core chip/driver/HPA)*: Bare dies for MIL and BCB protected dies in molded QFN-type packages for the SMT TRM. All dies are especially designed and optimized for the application, meaning that foundry prices (e.g. €/mm²) were considered rather than market "MMIC off-the-shelf" prices. Note that the extra costs for the BCB and packaging were added for the SMT calculations.
- *MMIC assembly*: Conductive epoxy and wire bonding (HPA is pre-soldered to a heat spreader for MIL) and standard solder pick-and-place for SMT.
- *Other*: Necessary logics and voltage regulators were included similarly for both MIL and SMT.

2) METHODOLOGY

After deciding on the prerequisites, production flowcharts coherent with the two packaging concepts were established. Each operation was then studied and analyzed in terms of time, cost per hour, operation yield, repair/scrap yield, and cassation. The estimations were based on the existing production of similar items as well as some necessary new assumptions for large-volume production. Materials cost was based on available prices in 2007.

Based on these data first time yield, production cost, and cost of poor quality (repair and cassation) were calculated for each operation as well as for the modules.

3) RESULTING RELATIVE UNIT PRODUCTION COST

The cost estimation was performed for a production volume of 10 000 TRMs per year. The traditional hermetic MIL packaging, considered as the technology workhorse of today, was used as a reference (100%); see Fig. 3. The calculations further estimated that a similar first time yield of typically 85% was achieved for both concepts.

The result of Fig. 3 indicates a 60% percentage cost reduction when using the SMT packaging concept compared

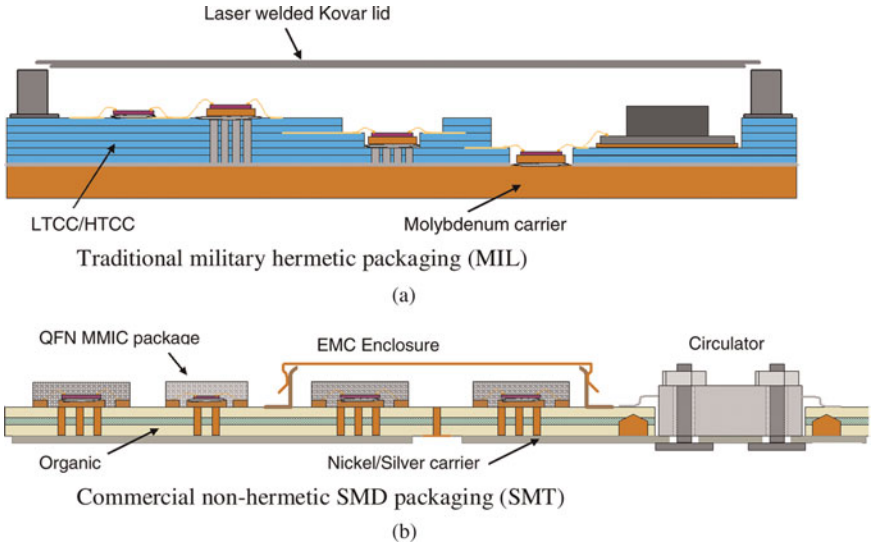

Fig. 2. Conceptual drawings describing the MIL and the SMT packaging concepts for TRMs.

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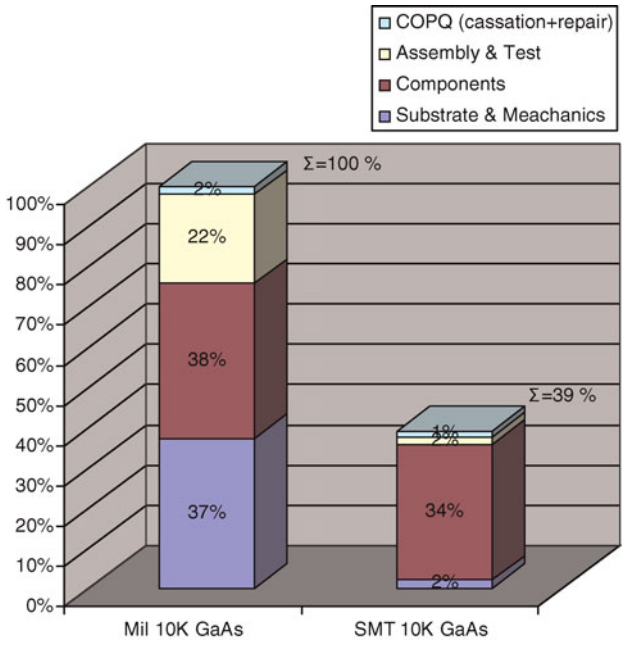

Fig. 3. Calculated relative unit production cost for the MIL and the SMT packaging concepts. The calculations were based on volumes of 10 000 units/year.

with the traditional MIL packaging. Huge cost savings were estimated for materials/components as well as for the assembly and test. For the MIL concept, 37% of the total cost was due to the LTCC substrate and the mechanics (carrier/lid/frame) while this share was reduced to only 5% for the SMT packaging TRM. The standard soldered pick-and-place assembly, performed on large panels, was also a main differentiator comparing the concepts. Simplified testing and exclusion of the hermeticity requirements also significantly contributed to the estimated cost reduction.

B) SiGe cost impact

It is noteworthy from the previous analysis that when using the SMT packaging concept the production cost is almost totally dominated (≈85%) by the component cost, whereas for the MIL approach the component cost was only roughly 40%. A closer look at the material and component cost share of the SMT TRM (Fig. 4) reveals that the component cost is dominated mainly by the HPA, core chip, and the ferrite circulator.

Together these three components stand for roughly 70% of the total material cost when using the SMT packaging concept. Consequently, significant cost savings can be achieved by reducing the cost of these components. In the following analysis, we will concentrate on the reduction of the core-chip cost by using SiGe BiCMOS MMIC technology instead of GaAs.

1) CORE-CHIP COST

The main parameters for core-chip cost analysis are as follows:

- wafer cost (for ∼10 000 TRMs/year),
- wafer size,
- die size,
- yield.

When analyzing these costs, the main differentiator in unit core-chip cost was wafer size. In this estimation, 4 in wafers were assumed for GaAs and 8 in wafers for SiGe BiCMOS. A 0.25 μm p-HEMT was assumed for GaAs and a 0.35 μm SiGe BiCMOS process for Si. The analysis showed that SiGe core-chip cost was typically 20% of the GaAs core chip.

The SiGe core chip also includes some logics such as S/P conversion and necessary data buffers, whereas the GaAs core chip has a simple parallel logical interface. This means that the cost for a separate logic IC was excluded in the SiGe core-chip TRM cost calculation. However, the cost of

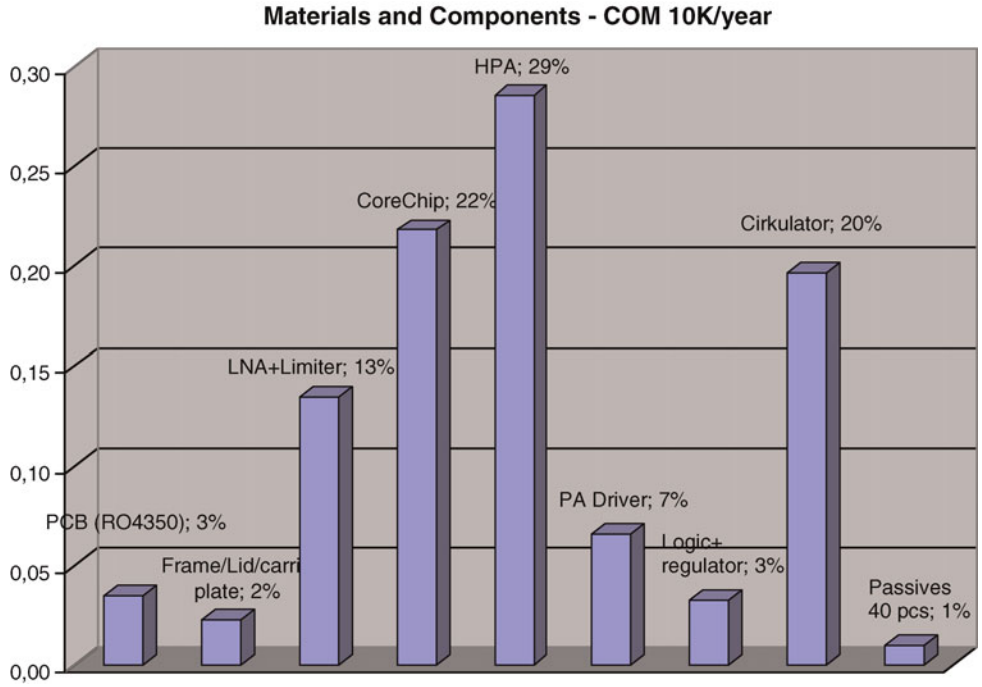

Fig. 4. Estimated materials and components relative cost share for the SMT packaging concept (GaAs core chip).

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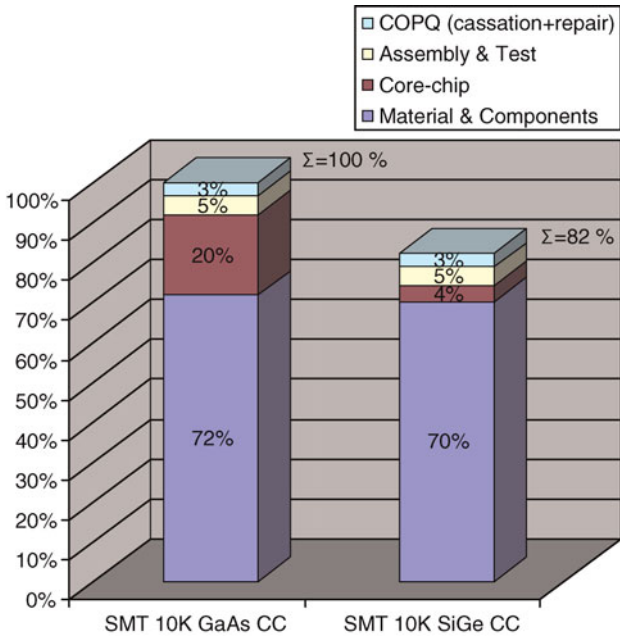

Fig. 5. Relative cost comparison of the impact of different core-chip technologies (GaAs and SiGe) for the SMT packaging concept.

the logic IC is rather small, and hence the effect of this was not very significant.

2) TRM COST ANALYSIS

The result of the calculation for the SMT packaging TRM, when different core-chip technologies were accounted for, is shown in Fig. 5. The results indicate that the TRM unit price can be further reduced by 18% by using SiGe instead of GaAs.

The expected cost reduction for the MIL TRM was much smaller, due to the lesser component cost share. The total cost was only reduced by roughly 6%.

C) Conclusions of TRM cost analysis

The conclusions of the performed analysis are pretty clear, even if specific details regarding the cost can be further discussed. The main cost reduction, cutting the cost by more than 50%, can be achieved by using the proposed SMT packaging concept. SMT packaging takes advantage of the high-frequency surface-mount packaging concept driven by telecom and defence R&D programs for the last 10 years.

Changing from GaAs to SiGe core chip means a smaller but still significant relative cost reduction when the MIL packaging concept is used. However, the relative cost impact of SiGe becomes very significant when SMT packaging is employed. Overall, the analysis indicates that the TRM cost, for S/C/X-band radar application, can potentially be reduced by approximately 70% compared to the typical TRM (MIL/GaAs core chip) unit cost of today.

IV. MMIC TECHNOLOGY

As shown above the cost impact of ICs becomes more pronounced when a low-cost, high-volume approach is used for the TRM, which makes it desirable to use low-cost semiconductor technologies where possible. It has been shown [1, 3–5] that this can be done when the core chip is considered, because the core chip has relatively moderate requirements on noise figure and output power but high requirements on integration, yield, and digital content. This, together with cost, makes the strongest argument in favor of silicon germanium when compared to other semiconductor technologies. One aspect that is often overlooked is that the high level of integration does not apply only to digital circuits. Of perhaps equal importance is the possibility to design microwave circuits with a high density. This allows for a designer to design more complex microwave circuits without the penalty of parasitics that follow from a large circuit area.

V. SIGE DESIGN CONSIDERATIONS

Compared with designing core chips in gallium arsenide, there are differences in doing the same in silicon due to the differences in device characteristics. Below are listed a few of these without any order of precedence; for a more thorough comparison, see the conference proceedings [3]:

- MOSFETs make poor switches at high frequencies compared to pHEMT-based switches. This leads to a worse loss-isolation ratio.
- Silicon can be considered as a lossy dielectric or even a resistive material, which means that it is not useful as a traditional microwave substrate as is the case with semi-insulating GaAs. The losses in, for example, inductors are still comparable to those of inductors supplied in gallium arsenide design kits.
- The design flow supported by silicon foundries is much more advanced, including autorouting, etc.
- When noise figure, linearity, and parasitics are considered, gallium arsenide transistors outclass silicon and silicon germanium ones. For core chips this is of less importance, as stated in the introduction.
- The physical size of comparable devices is typically much smaller in silicon than in gallium arsenide. This allows for more complex designs that can enhance the performance of the total IC.
- The DC behavior of silicon devices is usually well modeled which is why more complex analog circuits, e.g. operational amplifiers, temperature sensors, etc. can be designed with a high degree of accuracy.
- The high yield compared to gallium arsenide ICs together with access to CMOS circuits means that it is possible to use digital control circuits internally on chip.
- The small size of microwave devices and access to digital circuits allow one to design circuits, e.g. phase shifters, without equidistant steps and instead use on-chip tables and memories to fix this. This sometimes allows for simpler microwave circuits to be used.
- The maturity of silicon processes and its good environmental protection relax the requirements on the environmental protection of the next level in TRM hierarchy.
- Most silicon foundries support only time-domain simulators, e.g. Spectre. This can be a problem since the next system level is usually designed using microwave design tools.

The conclusion is that it is not a good idea to move a design directly from a gallium arsenide process to a silicon

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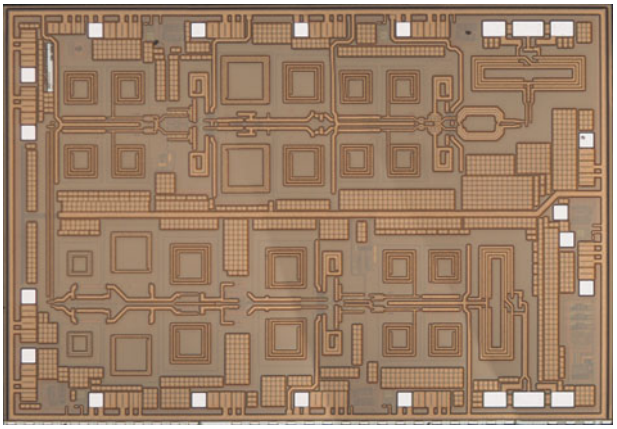

Fig. 6. Microphotograph of the S-band core chip (Score).

germanium process. The biggest issue, however, is the poor performance of the switches. One must therefore put more effort to first redesign switched applications such as phase shifters and attenuators.

Switched attenuators are thus replaced and amplitude control can instead be realized using variable gain amplifiers (VGAs). To realize phase shifters without switches is a bit more complicated. There is always the possibility of using a vector modulator, which might be inevitable if broadband phase shifters are to be designed. In that case only one 90° phase shifter needs to be realized together with VGAs. In this work, however, phase shifters based on switched LC networks are used. The goal has been to minimize the effect of switches on total performance. The third application for switches is T/R functionality when transmit–receive functionality is required. In this case an even more complex architecture has been implemented and is patent pending. The idea is to make T/R switching by an active three-port device, where transmission between the desired ports is defined by the active elements. The next issue that needs to be addressed is the fact that differential circuits are preferred in silicon RFICs. This means that baluns are needed at input and output. Lattice baluns, coupled inductors, or active baluns could be used, depending on the requirements on common-mode suppression, noise figure, and bandwidth. In this work, only passive baluns are used. First-order lattice baluns are broadband and well matched with low losses. They do, however, have rather poor common mode suppression over a larger frequency band.

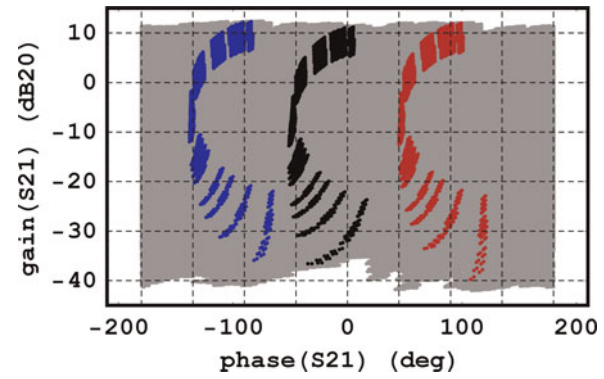

Fig. 7. Measured phase and gain states of the SiGe Score. The two million states are shown in gray color and the three amplitude sweeps with different phase states are represented in blue, black, and red color, respectively (from left to right).

VI. DESIGNED CORE CHIPS IN SILICON

Several core chips were designed and manufactured in silicon germanium at Saab Microwave Systems as part of ongoing development toward low-cost AESA radars. So far core chips at the S- on C-band have been demonstrated. Substantial work, however, has been spent aiming toward X-band and multiband applications. Most of that work has not been aimed directly at TRMs and is therefore omitted in this paper.

A) S-band core chip (Score)

A single leg core chip for the S-band has been designed and manufactured (Fig. 6). The layout and performance are optimized to fit into a leaded plastic package to enable a low-cost module based on commercial board technology. The design has a bandwidth of 3.0–3.5 GHz and is well suited for airborne surveillance radar. It has an extreme available resolution covering 45 dB and 360°: a total of 21 bits corresponding to 2 million states. Since this resolution is usually not needed, one can choose the state that best corresponds to the required

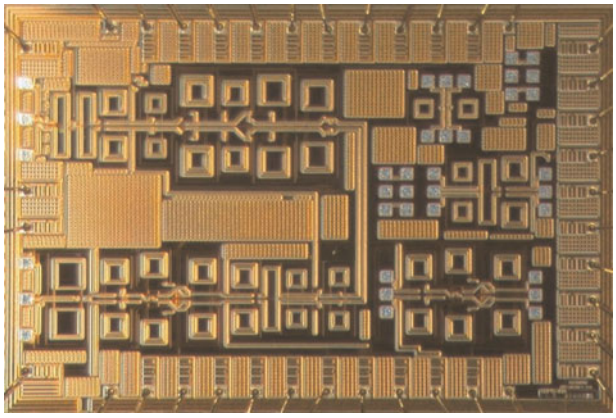

Fig. 8. Microphotograph of the C-band core chip (SiGeMINI).

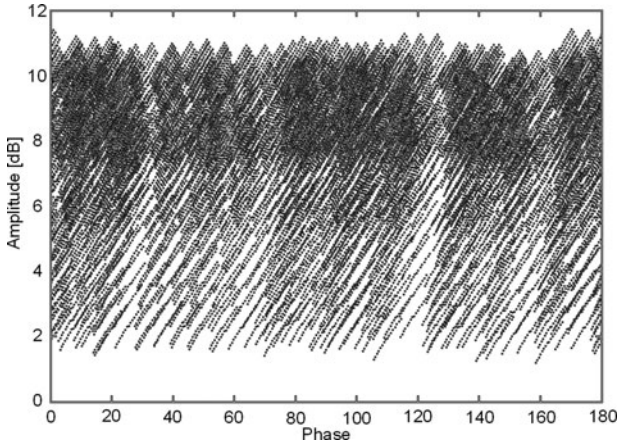

Fig. 9. Phase and gain states for SiGeMINI when the analog amplitude control is disabled.

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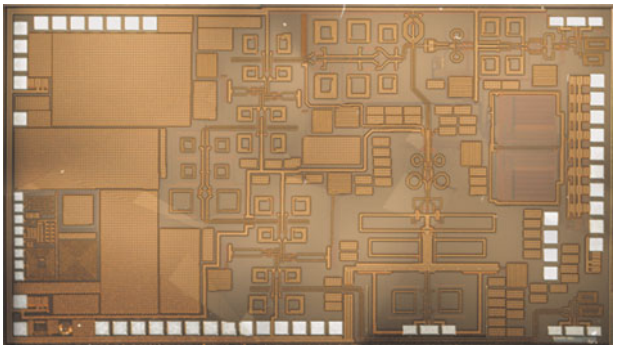

Fig. 10. Microphotograph of the C-band core chip (Sleipner).

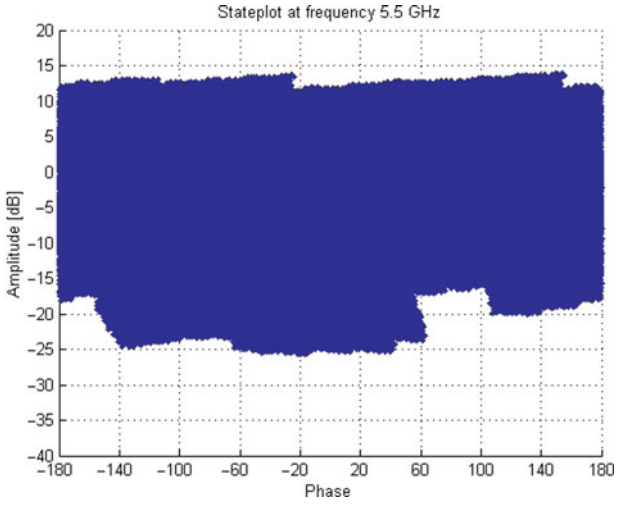

Fig. 11. Phase and gain states for Sleipner.

state. This approach with an excess number of states requires a serial interface, which has been implemented. Added value from the high level of integration is that a temperature sensor is also implemented. This is one example of the possibility to reduce the number of components at module level. The IC has a total die size of 3.8 × 2.8 mm.

The IC above has its input at the top and output at the bottom. ESD-protected pads can be seen around the edges of the IC. All internal bias voltages and current references are created internally from a single +5 V supply.

In Fig. 7 one can see that the 2 million available states present an extreme resolution in phase and gain for gain settings between +10 and −35 dB. One can also see that there are some differences between the three highlighted curves showing three different phase states. This implies that there is some coupling between input and output on the chip. The magnitude of this coupling can be calculated to be in the order of −50 dB. This is in the same order of magnitude as the coupling between two ground-signal–ground-probes at the distance in question.

B) C-band core chip (SiGeMINI)

As part of an AESA study program at Saab Microwave Systems, a silicon germanium core chip [1] at the C-band was designed in parallel to the work with a gallium arsenide one [2]. The SiGe core chip consists of a single leg topology with phase and amplitude control. It was considered to be a demonstrator of the potential of low-cost silicon in high-frequency applications with performance suitable for radar. The amplitude control was divided into two parts: a 5-bit fine amplitude control that can be used to compensate for differences in gain originating from temperature and process variation in both IC and module, and an analog amplitude control with high dynamic range that can be used for tapering the antenna. The analog control signal is accessible directly since this is a demonstrator not directly aiming at a product. For the same reason no internal voltage references were used. These could instead be controlled from the outside in order to increase the testability during the measurements. Extra test circuits were included on chip, which made the total chip area 5.04 × 3.4 mm. The IC is designed to fit inside a 7 × 7 mm QFN package (Fig. 8).

Below the measured phase and gain states are shown when the analog amplitude control is not activated. One can see that there is a good resolution in phase and amplitude over gain settings between +10 and +2 dB. The phase states shown cover only half a circle: 0–180° since the analog amplitude control also switches the polarity of the signal (Fig. 9).

One can see that even though the analog amplitude control is not activated, the IC has more than sufficient resolution. This reduced amplitude control is however too small if antenna tapering is to be done with the core chip. This would be fulfilled using the analog amplitude control.

C) C-band core chip with T/R function (Sleipner)

Using the sub-circuits from SiGeMINI, a core chip including T/R functionality was designed. It has a T-like architecture as mentioned above. The switching is done by switching the gain on and off in the three legs (Fig. 10).

This design was done as a "drop-in" replacement to a gallium arsenide core chip, so the size and pad locations are everything but optimal. RF port locations together with

Table 1. Summarized results.

Parameter	Gemini-S (GaAs) [2]	Gemini-C (GaAs) [2]	Score (SiGe)	SiGeMINI (SiGe)	Sleipner (SiGe)
Frequency band (GHz)	3–3.5	5–6	3–3.5	5–6	5–6
Max gain *Rx*/*Tx* (dB)	11/24	12	10	10	16/13
Noise figure (*Rx*) (dB)	<10	<8	<8	<12	<7
Input TOI (*Rx*) (dBm)	>16	>16	>15	>10	>5
P1dB (*Tx*) (dBm)	+20	+16	+8	+10	+13
Gain control	7 bit, 40 dB	6 bit, 20 dB	11 bit, 45 dB	5 bit + analog, 45 dB	6 bit, 31.5 dB
Phase control	6 bit, 360°	7 bit, 360°	10 bit, 360°	9 bit, 360°	6 bit, 360°
Interface	Parallel	Parallel	Serial	Serial/parallel	Serial
Supply voltages (V)	+3.5, −5	+3.5, −0.5, −5	+5	+5, +4, +2	+5

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conductive substrate caused some leakage between input and output. This resulted in unwanted variations in phase depending on commanded amplitude and vice versa. The states, however, cover the phase state diagram for gain settings between +11 and −17 dB with an extremely high resolution. The best suited states can then be chosen using a table in a ROM implemented on chip (Fig. 11).

D) Summary and comparison

Below some of the microwave parameters for the three core chips presented in the paper are shown together with two typical GaAs core chips from [2] (Table 1).

VII. CONCLUSION

Two low-cost enabling TRM technologies have been proposed and analyzed. Three core chips manufactured in a standard silicon germanium process have been presented. This process was shown to be an attractive alternative for some circuit applications, of which phase and amplitude control in AESA-type radars is one. A non-hermetic surface-mount packaging concept (SMT) has also been proposed. Cost analysis shows that a potential 60% cost reduction can be achieved compared to traditional ceramic hermetic packaging (MIL). The change from GaAs core chip to SiGe core chip reduces the cost by 6% for a traditional MIL TRM and by 18% for a TRM using SMT packaging.

The cost analysis concludes that by using the proposed packaging concept and SiGe core-chip technology, TRM production cost can be potentially reduced by 70% compared to traditional ceramic hermetic packaging with core chip in GaAs technology.

ACKNOWLEDGEMENT

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