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RESEARCH PAPER

J-band amplifier design using gain-enhanced cascodes in 0.13 μm SiGe

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This paper presents two J-band amplifiers in different 0.13 μm SiGe technologies: a small signal amplifier (SSA) in a technology in which never before gain has been shown over 200 GHz; and a low noise amplifier (LNA) design for 230 GHz applications in an advanced SiGe HBT technology with higher fT/fmax, demonstrating the combination of high gain, low noise, and low power in a single amplifier. Both circuits consist of a four-stage pseudo-differential cascode topology. By employing series–series feedback at the single-stage level the small-signal gain is increased, enabling circuit operation at high-frequencies and with improved efficiency, while maintaining unconditional stability. The SSA was fabricated in a SiGe BiCMOS technology by Infineon with fT/fmax values of 250/360 GHz. It has measured 19.5 dB gain at 212 GHz with a 3 dB bandwidth of 21 GHz. It draws 65 mA from a 3.3 V supply. On the other hand, a LNA was designed in a SiGe BiCMOS technology by IHP with f_T/f_{max} of 300/450 GHz. The LNA has measured 22.5 dB gain at 233 GHz with a 3 dB bandwidth of 10 GHz and a simulated noise figure of 12.5 dB. The LNA draws only 17 mA from a 4 V supply. The design methodology, which led to these record results, is described in detail with the LNA as an example.

Keywords: Low noise and communication receivers, Circuit design and applications

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I. INTRODUCTION

Millimeter-wave (mmWave) frequencies are attractive for a wide range of applications in various fields, including security, safety, health care, industrial quality control, and scientific research.

Frequencies above 100 GHz have lately received increasing attention [1], based on the rapidly growing need for higher data rates in communication technology. As the available bandwidth is small in classically used low frequency-bands, high data rate communication requires complicated and noise-sensitive modulation schemes. Technology, especially device performance, sets here a natural limit. The alternative is a shift upwards in operational frequency, as above 100 GHz wider bandwidth is available. A set of frequency bands where atmospheric attenuation is low and which are thus well suited for high data rate communication is between 200 and 300 GHz.

Apart from communication, other applications also benefit from the bandwidth available at high-frequencies. On a circuit building block level high power, high bandwidth multiplier chains for signal generation have been demonstrated [2]. For radar circuits, wider bandwidth improves the range resolution [3], leading to more precise measurements. For passive imaging [4] enormous bandwidth at high-frequency is of utmost importance, as it is a part of the equation of the noise equivalent temperature difference, which is a measure for detector sensitivity. In this application, cost-effective solutions with silicon technology have the potential to revolutionize the field of security screening.

Traditionally, these high-frequency bands were the domain of III–V semiconductors, due to their superior device characteristics. But with the recent advances in fabrication technology, heterojunction bipolar transistors (HBTs) with a maximum oscillation frequency f_{max} beyond 450 GHz [5] have become available. This motivates the development of radio frequency (RF) integrated circuits towards higher frequencies than previously deemed feasible in silicon. The resulting low production costs at high volumes are the major requirement for further growth in emerging consumer markets.

Whether in communication, radar or imaging applications, there is a need to minimize noise in a wireless receiver front-end. Referring to Friis' formula [6], typically a low noise amplifier (LNA) as a first active component in such a system provides sufficient gain for the incoming signal to reduce the noise impact of subsequent components. This optimizes the signal-to-noise ratio.

On the other hand, not only high gain, but also bandwidth and power consumption are extremely important for the performance of a LNA integrated into a wireless receiver front-end. Therefore all of them have to be optimized, if the LNA is to be used in a real system [3].

Despite the advances in silicon germanium technology, gain at higher frequencies is still limited. This creates not

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only the need for multistage design, but also for optimizing single stage gain. Feedback can provide a compensation for the gain roll-off at elevated frequencies, thus enhancing single stage performance.

To showcase the potential power and reliability of this method, two amplifiers in technologies from different foundries have been designed.

The first presented amplifier is a four-stage small signal amplifier (SSA) in Infineons B11HFC technology [7]. It has a high bandwidth and over 20 dB of gain for differential in-system usage at an operational frequency at which, to the authors best knowledge, gain has never been published before in this particular technology [8, 9].

Previously published J-band LNA designs have shown either high gain with high power consumption [10] or high bandwidth [11, 12], but never both in combination. Thus, the second amplifier presented in this work is a four-stage LNA in IHPs SG13G2 technology, that combines high gain with low power consumption, while surpassing the bandwidth limit of the previously published amplifiers with comparable high gain.

This paper is organized as follows: Section II discusses the theory behind using an inductor as a series–series feedback element to boost the gain of a cascode topology. Section III describes the design methodology based on S-parameter analysis, which leads to the circuit architectures from Section IV. Measured results of both circuits are presented in Section V. Finally, Section VI provides a conclusion.

II. SERIES–SERIES FEEDBACK FOR GAIN ENHANCEMENT

In bipolar transistors the optimum collector current density for minimum noise figure, even though increasing with operational frequency, is factors smaller than the necessary current density to reach optimum f_{max} [13]. Thus, biasing the transistor for low-noise operation diminishes single stage gain, but also reduces power consumption, increasing efficiency. To compensate for the low single stage gain, different approaches are possible.

As the unilateral power gain is an inherent figure of merit of a transistor [14], most approaches are based on reducing the internal feedback of the device, thus providing unilateralization. A common way in CMOS technology is capacitive cross-coupling for neutralization of the pseudo-differential common-source or cascode-structure [15, 16].

An alternative first step to increase the gain and to extend the operational bandwidth of a mm-wave amplifier is to employ a cascode structure. The usage of a common-base as a load to a common-emitter transistor reduces the Miller capacitance and therefore greatly improves reverse isolation, thus stability and ease of impedance matching.

However, the unilateral power gain is not the absolute maximum achievable gain of a transistor as shown and defined in [17]. Contrarily, as previously analyzed for CMOS structures [18], the introduction of feedback at the common-base transistor of the cascode is an option for compensating the gain roll-off at higher frequencies, actually decreasing the reverse isolation and introducing the risk of instability. Simultaneously maintaining unconditional stability thus becomes priority.

Feedback theory based on two port analysis as found in textbooks like [19] describes the underlying working principle of the method applied here through simplification.

Figure 1 breaks down an exemplary cascode consisting of common-emitter transistor Q1, common-base transistor Q2 and feedback inductor L_{fb} into their simplified high-frequency small signal equivalent circuits. Two-port representation is indicated in the figure. Including the additional inductor, the cascode now consists of two cascaded single feedback loops. The inherent Miller-capacitance as part of Y_μ is the major feedback element in the common-emitter transistor, best described as shunt-shunt feedback. Modeling the voltage transfer function in terms of a single feedback loop, the feed-forward factor a_1, and the feed-backward factor f_1

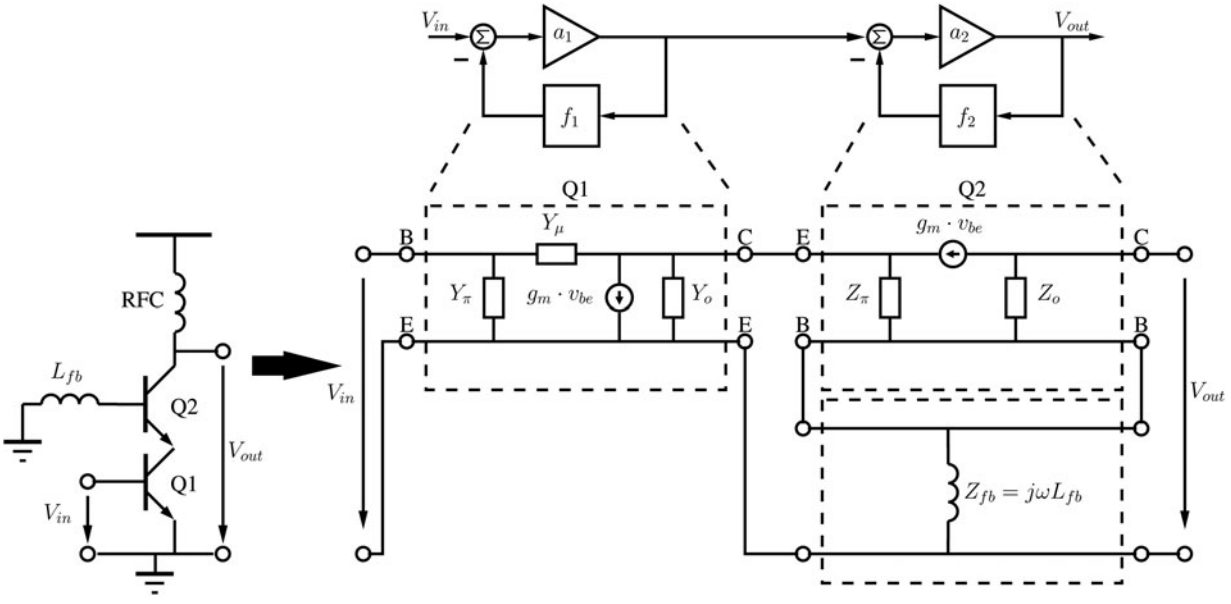

Fig. 1. High-frequency small signal equivalent circuit of a cascode. The additional inductor L_{fb} introduces a frequency dependent component to the feedback function, diminishing the phase margin, but also boosting the power gain.

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are found to be:

$$a_1 = \frac{Y_\mu - g_m}{(Y_L + Y_\mu + Y_o)(Y_S + Y_\mu + Y_\pi)}, \quad (1)$$

$$f_1 = -Y_\mu. \quad (2)$$

Here, Y_S is the source admittance and Y_L is the combined input admittance of the following common base transistor and the feedback inductor L_{fb}.

Equation (3) gives the voltage transfer function for the common emitter transistor:

$$A_1 = Y_S \cdot \frac{a_1}{1 + a_1 f_1}. \quad (3)$$

At the common-base transistor L_{fb} introduces a feedback path extrinsic to the device. Similar to the case of the common emitter transistor, two-port analysis allows further insight into the working mechanism of the series–series feedback applied here at the common base transistor. As a first step, the Z-parameter-matrices of the common-base transistor and the feedback inductor are added. Extracting the factors a_2 and f_2 for the voltage transfer function A_2 of a single series–series feedback loop as shown in equation (6) results in:

$$a_2 = \frac{Z_{fb}(Z_\pi g_m - 1) + Z_o Z_\pi g_m}{(Z_L + Z_{fb} + Z_o)(Z_S Z_\pi g_m - Z_S + Z_{fb}(Z_\pi g_m - 1) - Z_\pi)}, \quad (4)$$

$$f_2 = Z_{fb} = j\omega L_{fb}. \quad (5)$$

Here, Z_S is the output impedance of the preceding common emitter transistor and Z_L is the load impedance.

$$A_2 = -Z_L \cdot \frac{a_2}{1 + a_2 f_2}. \quad (6)$$

The open loop gain T and the overall voltage transfer function H of the two concatenated single feedback loops then are:

$$T = A_1 \cdot a_2 \cdot f_2, \quad (7)$$

$$H = A_1 \cdot A_2 = \frac{a_2}{(1/A_1) + T}. \quad (8)$$

As shown in equation (5), both magnitude and phase of a_2 and f_2 change with either increasing frequency or inductance, resulting in a trade-off of phase margin for gain by altering the open loop gain T in such a way that it partly compensates $1/A_1$. If now L_{fb} becomes too large, the open loop gain shifts the real part of either the input or output impedance of the circuit to negative values. This is equivalent to S_{11} or S_{22} rising above unity, which equals instability and potentially oscillation.

Kim *et al.* [20] investigated the influence of an additional inductance at the base of a common-base transistor amplifier on the maximum stable gain (MSG) and the stability factor k, showing that for inductors of implementable size with regards to accurate modeling, stability can be maintained while increasing the overall gain.

The next section provides further insights into the necessary design methodology based on S-parameter analysis, discussing the benefits and how to avoid the potential risk of instability by employing a frequency dependent feedback network in cascode SSA.

III. DESIGN METHODOLOGY FOR GAIN ENHANCED CASCODES

This section presents the methodology, which was used during the design phase of both amplifiers. It reliably and repetitively produces stable high gain amplifiers at frequencies above $1/3f_{max}$ of the used technology.

According to the design goal, the basic circuit parameters are chosen. For LNA design, the cascode is biased at the optimal current density for low noise operation J_{opt}. Following this step, the emitter-sizes of the transistors are scaled in such a way that impedance and noise matching can be achieved simultaneously with a simple L-match.

From simulating the optimal feedback inductance value for different transistor sizes it is apparent, that the feedback inductor becomes smaller and therefore harder to model, the bigger the used transistors are. Thus, it is advised to choose the transistor size as small as still suitable to the design goals. Figs 2 and 3 show simulation results for a cascode with transistors in IHP technology with an emitter area of $A_E = 2 \times (0.12 \times 0.96)\ \mu m^2$, which is used in the LNA design presented in this work. Here, the inductor is already of parasitic size.

The series–series feedback inductor is introduced at the base of the common-base transistor. As this is a reactive feedback element, the lowest frequency at which the amplifier still has gain becomes important, because at this point the maximum transducer gain is at its highest. Thus, at the low end of the operational bandwidth, the inductor size versus the stability factors k and μ is simulated, see Fig. 2. The continuous decrease of the Edward and Sinsky stability factor μ indicates a reduction in stability as the inductance increases. Simultaneously it is observed, that as Rollet's stability factor

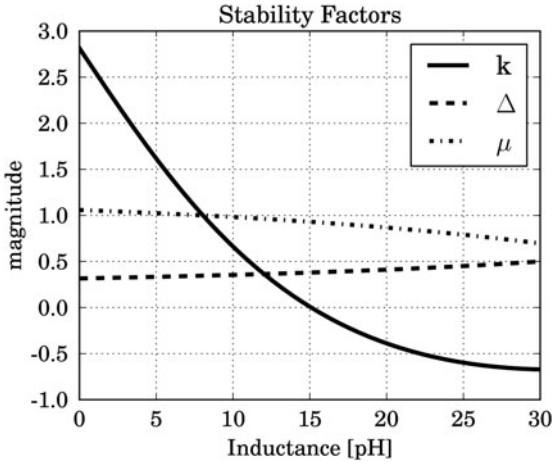

Fig. 2. Influence of the feedback inductor L_{fb} on stability factors k, Δ, and μ as simulated for a cascode in IHP SG13G2 technology at 230 GHz. As the inductor size increases, μ decreases, indicating reduced stability. As k and μ drop below 1, the cascode leaves the area of unconditional stability. The influence of L_{fb} on Δ is negligible.

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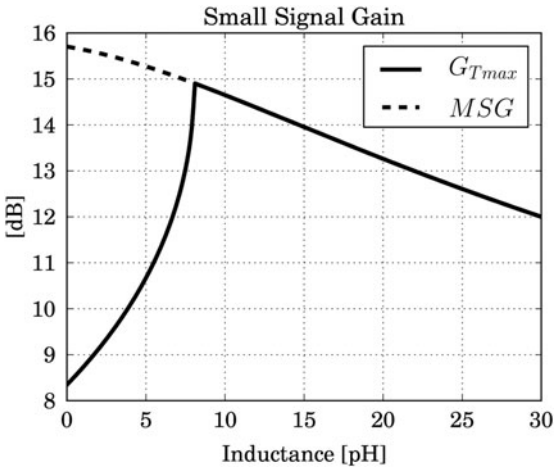

Fig. 3. Influence of the feedback inductor L_{fb} on the maximum transducer gain G_{Tmax} and the MSG. When k becomes 1, G_{Tmax} equals MSG. Up to this point, it is still possible to conjugately match the cascode at input and output, resulting in improved gain and preserved unconditional circuit stability.

k becomes one, the maximum transducer gain G_{Tmax} equals the MSG, see Fig. 3. After this point, the cascode is no longer unconditionally stable, as the load stability circle moves into the Γ_L plane. A further consequence of k becoming smaller than one is, that it is no longer possible to achieve a simultaneous conjugated match, thus degrading power transfer and therefore power gain. As is typical for series–series feedback used for gain enhancement, increasing the inductance of L_{fb} also reduces the input and output impedances of the cascode, which changes the size of the output matching elements. This may be particularly critical for power amplifier design, as maximum size transistors are preferred, which especially at frequencies above 160 GHz have low output impedance, even if a cascode topology is utilized [21].

Following this reasoning and to ensure stable amplifier operation in face of simulation model imperfections, the inductance value has to be chosen conservatively. Rigorous electromagnetic (EM)-modeling becomes necessary at this point, especially if the inductor is small in physical size.

Afterwards, the use of standard formulas for simultaneous conjugated matching as discussed in [22] provides values for input, output, and interstage matching elements. The inherent loss at high-frequencies of integrated matching elements like transmission lines reduces the achievable gain, but aids the preservation of circuit stability. Thus it is recommended not to compensate for the losses of matching elements by further increasing the feedback.

On the same note, the matching procedure described in [23], while being successfully employed in many LNA designs today, limits the achievable gain due to inductive degeneration. Therefore it is only suited for transistor operation above $1/3f_{max}$ as long as the used degeneration inductor is small.

If single-stage gain is still too low for the envisioned application, multiple stages can be cascaded. As small transistor sizes with limited current handling capability are used in consecutive stages, linearity problems may arise.

As a last step, every single amplifier stage on its own and all amplifier stages together are simulated not only in the desired frequency-band of operation, but over the whole frequency range, to ensure stability.

IV. CIRCUIT ARCHITECTURE

This section presents the circuit architecture of both amplifiers, that has been the result of following the described design methodology, while highlighting the unique choices for the differing design goals. Last but not least, the passive elements used for on-wafer probing are discussed.

Full-wave EM-simulation results (from HFSS) of the transmission lines and interconnects were included as S-parameter blocks in the simulation during the design phase. In the single amplifier stages, the layout of all elements relevant at higher frequencies is completely symmetrical. This also includes all parasitics, which are introduced through inter-transistor connections or via to the transmission lines and capacitors. These parasitics are incorporated into the simulation post-layout as S-parameter blocks to analyze and correct for their influence on circuit performance.

Both amplifiers consist of four concatenated pseudo-differential cascode stages. A block-level representation of both amplifiers is shown in Fig. 4, including the Marchand baluns and the tuned pads for on-wafer probing.

Standard resistive biasing is utilized for the cascodes in both cases. The bias network of the common-emitter transistor consists of a current mirror with a resistive connection to the base of the transistor. The resistor has a value of 2 kΩ, which is high enough for the current mirror not to compromise the noise figure of the amplifier. The transistor employed in the current mirror is of half the size of one amplification transistor, thus the resistance at the base of the current mirror transistor has double the value of the resistance at the base of an amplification transistor. The common-base transistor is supplied through a simple voltage divider with a high-frequency short circuit to ground provided by metal-insulator-metal (MIM) capacitors with a cumulative value of 600 fF.

To avoid the influence of via parasitics, a thin strip of metal on the lowest layer of both processes form the small inductor L_{fb}, acting as a reactive feedback element for gain enhancement. During the design period, this metal-strip has been modeled as a shielded transmission line. Its impedance and length have been adjusted to provide high gain, while maintaining circuit stability within the available transistor

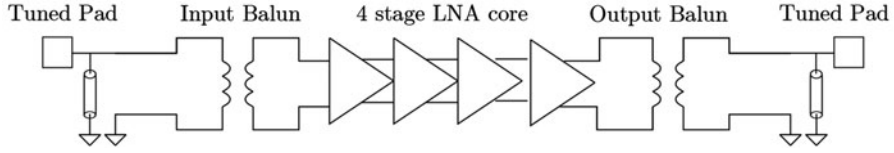

Fig. 4. A block-level representation of both amplifier architectures. Each amplifier consists of four equal, pseudo-differential stages connected in series, with Marchand baluns and tuned pads on both ends.

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parameters. Simulation predicts unconditional stability for both amplifiers over the whole frequency range from 1 to 300 GHz.

A) The SSA

Infineons 0.13 μm SiGe BiCMOS technology B11HFC is the basis for the SSA. It features high speed npn-HBTs with an effective emitter width of 0.13 μm, an f_T/f_{max} of 250/360 GHz. For these transistors to reach their optimum f_{max}, Infineon recommends the use of a BEBC transistor layout, as employed in this design. Four narrow and two thick copper layers for RF design purposes are available for routing purposes. Additionally, there are MIM capacitors (1.54 fF/μm^2) and both TaN- and polysilicon resistors, to cover the whole range of typically needed resistance values.

Each of the four concatenated stages of the SSA consists of a pseudo-differential cascode as presented in Fig. 5. In this technology, the emitter length of the device is adjustable at will. Therefore the transistors use an emitter length of 5 μm, as bigger transistors do not add significant more small signal gain, but increase current consumption considerably. The transistors are biased to operate below the high-current region to further reduce the current consumption, considering their non-minimal size. The ensuing lowered gain is then mitigated through the use of the described series–series feedback method.

The applied feedback inductor L_{fb} has 5 pH of effective inductance, while featuring a post-layout EM-simulated quality factor of 9.

Input impedance matching to a differential 100 Ω reference is done by an L-match consisting of a 18 fF MIM capacitor and a 70 μm transmission line. The output match is provided by a T-match with a 40 μm transmission line at the collector of each common-base transistor, a 37 μm transmission line as a short circuit stub to the supply and a 21 fF DC blocking MIM capacitor.

All four stages draw 65 mA from a 3.3 V supply. The output referred 1 dB compression point was simulated to be at −270 mdBm, using the same SPICE Gummel-Poon transistor model as has been used for all small signal simulations. The SSA uses an area of 580 × 245 μm^2; baluns and pads add to that, resulting in an overall area-consumption of 1070 × 270 μm^2.

B) The LNA

The LNA is fabricated in IHP's 0.13 μm SiGe BiCMOS technology SG13G2. Besides the 0.13 μm CMOS baseline process with five fine and two thick top patterned aluminum metal layers (2 and 3 μm) for RF applications, this technology is equipped with silicided and unsilicided polysilicon resistors, MIM capacitors (1.5 fF/μm^2). The effective emitter width of the HBTs is 120 nm. The f_T/f_{max} for this technology is 300/450 GHz.

The presented LNA is designed with four concatenated pseudo-differential cascode stages as shown in Fig. 6. To obtain an optimum noise match to a differential 100 Ω source impedance, the emitter-length of bipolar transistors can be scaled by simply connecting single devices in parallel, while keeping the current density for minimum noise J_{opt} the same Sorin. Following this principle, all four stages employ identical device sizes of $A_E = 2 \times (0.12 \times 0.96)$ μm^2. The transistors are used in a BEC configuration, which is the transistor layout recommended by the manufacturer in this technology. The HBTs are biased in a trade-off for low noise versus sufficient gain for suppressing the noise contribution of subsequent stages.

For this technology, bias point and transistor size, the effective inductance of the feedback inductor L_{fb} is chosen as determined in Section III to be 7 pH. Post-layout EM-simulation shows a Q-factor of 4 for this inductor.

For impedance matching purposes, transmission lines $TL1$, $TL2$, and MIM capacitors are used. An unshielded 70 μm long transmission line in the highest metal layer supplies each side of the differential cascode structure. DC-blocking MIM capacitors with a value of 6 fF each complete the output match to differential 100 Ω. Input matching is done with two 20 μm coupled transmission lines.

A filter network composed of $R1$ and $C1$ minimizes potential common mode instability due to coupling between the stages through the shared power supply connection.

All four stages of the LNA draw in total 17 mA current from a 4 V supply. Because these transistors are considerably smaller and due to the noise matching procedure biased to use very little current in comparison with the SSA, the output referred 1 dB compression point of this four stage amplifier was simulated to be at −10.9 dBm. The circuit itself is 270 × 280 μm^2

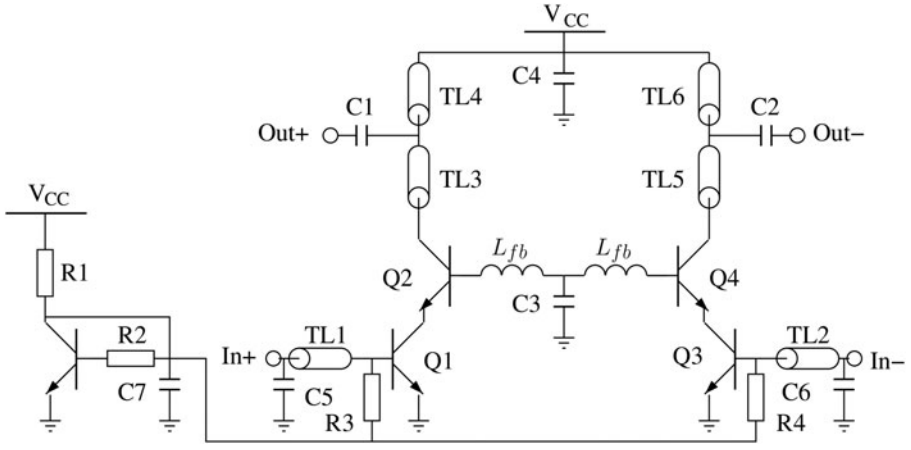

Fig. 5. Single stage circuit schematic of the SSA designed in Infineon technology. Input matching is achieved with series transmission lines and shunt capacitors, output matching with a T-match consisting of two transmission lines and a MIM capacitor on each side. An inductor at the base of the common-base transistor provides series–series feedback for gain-enhancement.

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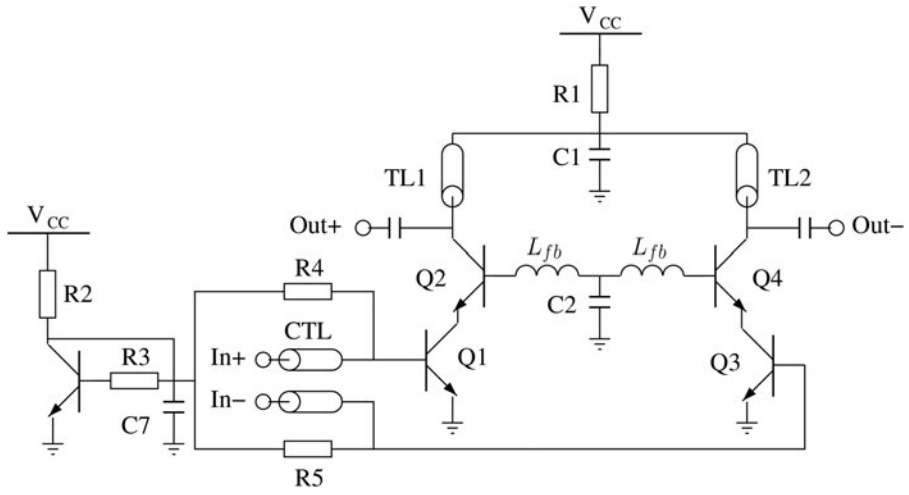

Fig. 6. Single stage circuit schematic of the LNA designed in IHP technology. Input matching is done with a coupled transmission line, output matching with an *L*-match consisting of one transmission line and a MIM capacitor on each side. R1 and C1 form a filter network for suppressing common-mode oscillations. Similar to the SSA, an inductor at the base of the common-base transistor is used for gain-enhancement.

in size; each balun adds another 130 × 240 μm² and the pads increase the break-out length by 95 μm.

C) Passive elements

Input and output Marchand baluns allow the use of single-ended 50 Ω probe contacts. This impedance is then transformed by the baluns to differential 100 Ω. In both technologies, they are implemented with a two-wire coupled transmission line structure in the top thick metalization layer with a 2.4 μm conductor width and a spacing of 2.4 μm. The coupled transmission lines are arranged in a rectangular loop. Their length corresponds to $\lambda/2$ at the design frequency, which is 360 μm in this case. A single balun has an EM-simulated loss of 1.5 dB.

For on-waver probing ground-signal-ground pads were added to the single-ended output of the baluns. A short grounded transmission-line stub compensates the pads' capacitance.

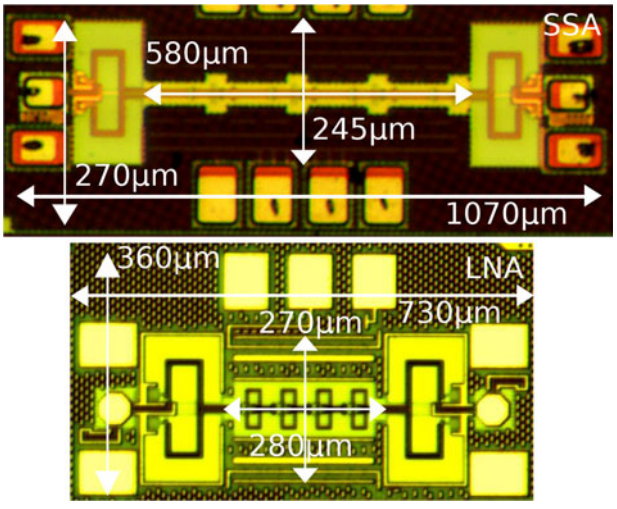

Fig. 7. Top chip micrograph: The SSA uses 580 × 245 μm² of area; baluns and pads add to that, resulting in an overall area-consumption of 1070 × 270 μm². Bottom chip micrograph: The area of the LNA without pads and baluns, e.g. for differential in-system usage, is 280 × 270 μm². The whole circuit breakout area is 730 × 360 μm².

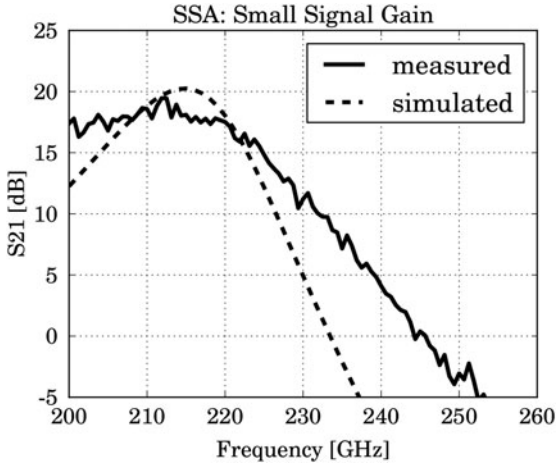

Fig. 8. Measured and simulated small signal gain of the amplifier in Infineon technology in comparison. The measured and simulated data both include the baluns and tuned RF pads at the input and output.

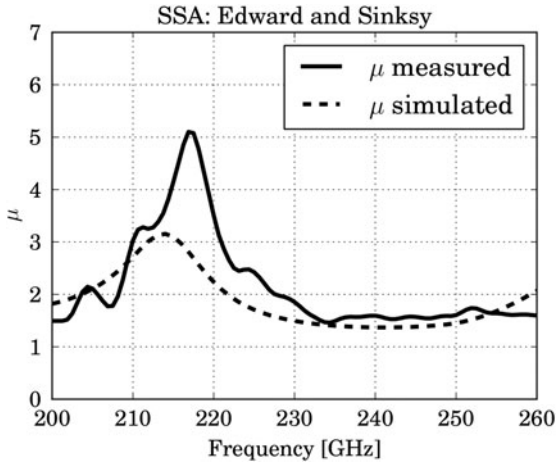

Fig. 9. Measured stability factor μ for the four-stage Infineon amplifier, indicates unconditional stability. For noise reduction purposes, the measured data has been averaged. The simulated μ of the whole four-stage SSA including baluns is equally above unity.

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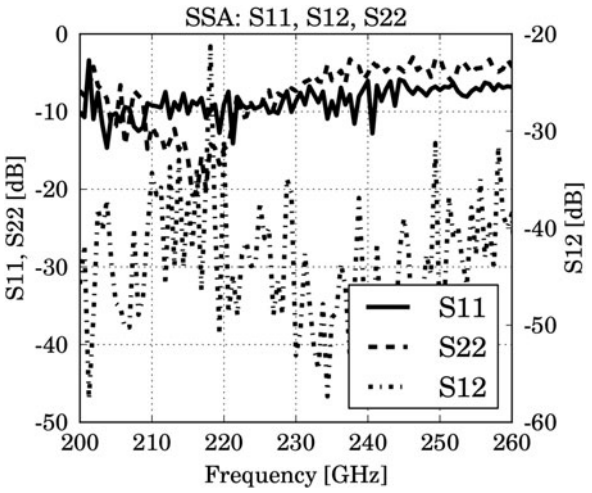

Fig. 10. Measured reverse isolation and reflection of the four-stage Infineon SSA including baluns and pads.

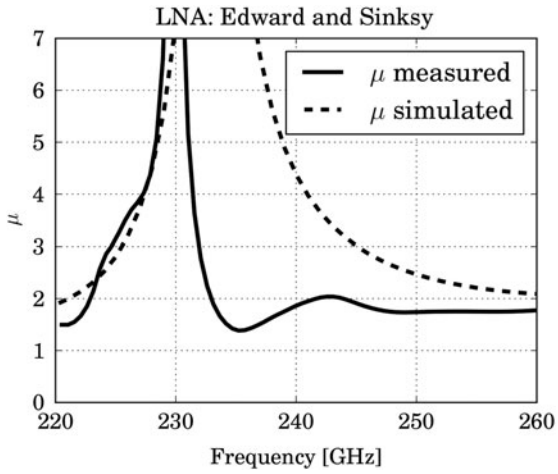

Fig. 13. Measured stability factor μ for the four-stage LNA, indicates unconditional stability. For noise reduction purposes, the measured data has been averaged. The simulated μ of the whole four-stage LNA including baluns is equally above unity.

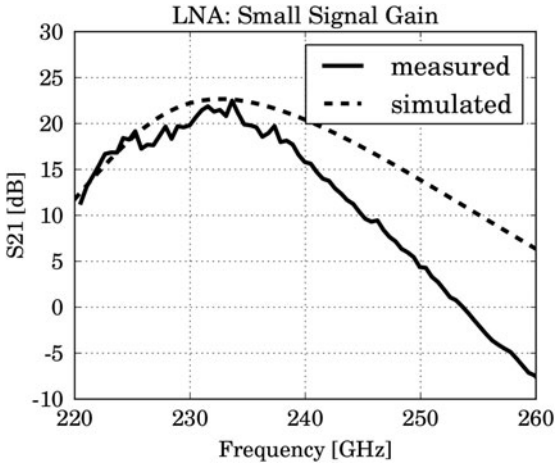

Fig. 11. Measured and simulated small signal gain of the LNA in IHP technology in comparison. The measured data includes the baluns and tuned RF pads at the input and output, the simulated data includes balun losses only.

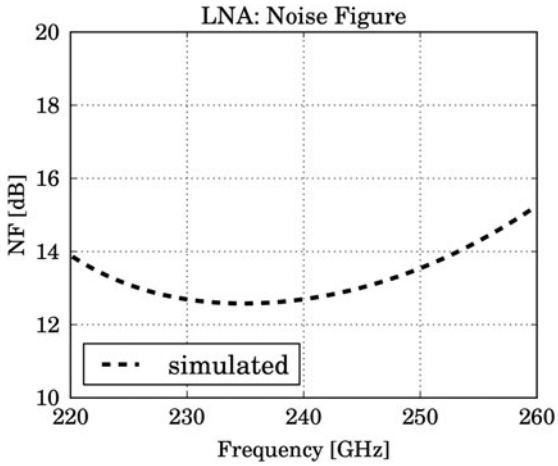

Fig. 14. Simulated noise figure of the four-stage LNA. The notch at the design frequency confirms the matching of the noise impedance to the source impedance.

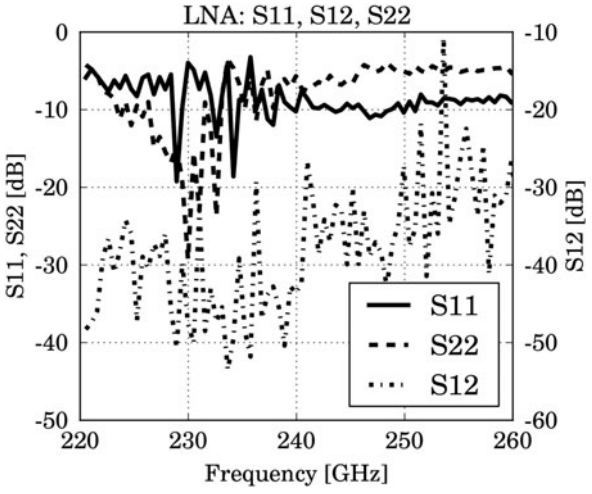

Fig. 12. Measured reverse isolation and reflection of the four-stage LNA including baluns and pads.

To determine the characteristics of the amplifiers for differential in-system usage, it is necessary to deembed the balun-plus-pad combinations on both sides of an amplifier. For that purpose a breakout structure of two balun-plus-pad combinations were placed back to back in both technology runs.

V. MEASURED RESULTS

Both amplifiers were characterized using ground-signal-ground (GSG) waveguide probes for the 220–325 GHz band by GGB (GGB Industries Inc.), OML (Oleson Microwave Labs Inc.) mmWave VNA extender modules and an Agilent E8361A network analyzer. For on-wafer characterization, on-chip baluns have been added at both the input and the output. As extracted from the breakout structures mentioned in the previous section, the measured average loss due to the pads and baluns is around 2.5 dB per side from 200–280 GHz in both technologies. Figure 7 presents micrographs of both amplifiers.

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Table 1. Comparison of mmWave LNAs.

Author	Öjefors [12]	Mao [11]	Schmalz [10]	This work	This work
Frequency (GHz)	210	245	245	212	233
f_T/f_{max} (GHz)	280/435	300/500	300/500	250/360	300/450
Technology	SiGe	SiGe	SiGe	SiGe	SiGe
Topology	3 stage differential cascode	4 stage single-ended CB	5 stage different cascode	4 stage different cascode	4 stage different cascode
Gain (dB)	14	12	18	19.5, probing, 24.5 in-system	22.5, probing, 27.5 in-system
3 dB BW (GHz)	28	25	8	21	10
NF (dB)	13 (simulation)	11.3 (simulation)	11 (measurement)	14 (simulation)	12.5 (simulation)
OP_{1dB} (dBm)	–	–	–	−270 m (simulation)	−10.89 (simulation)
DC power	42 mA @ 3.6 V	14 mA @ 2 V	82 mA @ 3.7 V	65 mA @ 3.3 V	17 mA @ 4 V
Area (μm^2)	385 × 155	420 × 460	360 × 430	580 × 245	280 × 270

CB, common base; NF, noise figure; BW, bandwidth.

A) The SSA

The SSA in Infineon's B11HFC technology has 19.5 dB of gain at 212 GHz with a measured 3 dB bandwidth of 21 GHz, see Fig. 8. If the pad and balun losses are deembedded, the gain is 5 dB higher and comes out at 24.5 dB. Measurement equipment limits the accurate determination of the bandwidth on the lower side, as the probes and OML modules are only specified between 220–320 GHz. Unconditional stability is attested through the Edward & Sinsky stability factor μ, which is above unity in the whole measured frequency range, as can be found in Fig. 9. Equally, the reverse isolation is around −30 dB in the frequency band of interest, as shown in Fig. 10.

B) The LNA

Figure 11 presents the measured and simulated small signal gain S_{21} in comparison for the LNA implemented in the IHP SG13G2 process. They are in good agreement, which validates the quality of the EM-modeling used for simulation of the matching elements. The four-stage amplifier has 22.5 dB maximum gain at 233 GHz. The 3 dB-bandwidth is 10 GHz. Correcting for pad and balun losses, the LNA has a net gain of 27.5 dB for differential in-system usage, e.g. to drive a mixer directly from an on-chip differential antenna. The input and output return losses S_{11} and S_{22} are plotted in Fig. 12, together with the reverse isolation S_{12}. The Edward & Sinsky stability factor, calculated from the measured S-parameters, indicates unconditional stability over the whole measured frequency range, as shown in Fig. 13.

Because of limitations in measurement equipment, specifically the unavailability of a high-frequency noise source and a fundamental J-band mixer, the actual noise figure has not been measured. Instead Fig. 14 presents the simulated noise figure over frequency. Due to the noise impedance match to the source impedance at the design frequency of 230 GHz, it comes out at 12.5 dB. At the bottom of Fig. 7 a micrograph of the 280 × 270 μm^2 small 233 GHz LNA can be found.

VI. CONCLUSION

Two amplifiers in differing SiGe BiCMOS technologies have been presented. Both rely on the deliberate use of feedback for gain-enhancement to achieve high gain above 200 GHz. Employing a 0.13 μm SiGe BiCMOS process currently under development for the SSA and a 0.13 μm SiGe BiCMOS process available through MPW for the LNA, this paper demonstrates the feasibility of further exploration of high mmWave frequencies, potentially up to the THz region. Table 1 summarizes the results of all J-band LNA implementations the authors are aware of. To the authors' best knowledge, the gain and bandwidth achieved with the SSA is the highest ever reported in that particular technology. For the LNA, both 22.5 dB as a measured breakout structure and the deembedded 27.5 dB gain for differential in-system usage are the highest gain ever reported in any SiGe technology in this frequency range.

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