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A 31 GHz body-biased configurable power amplifier in 28 nm FD-SOI CMOS for 5 G applications

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Research Paper

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Abstract

This paper presents a 31 GHz integrated power amplifier (PA) in 28 nm Fully Depleted Silicon-On-Insulator Complementary Metal Oxide Semiconductor (FD-SOI CMOS) technology and targeting SoC implementation for 5 G applications. Fine-grain wide range power control with more than 10 dB tuning range is enabled by body biasing feature while the design improves voltage standing wave ratio (VSWR) robustness, stability and reverse isolation by using optimized 90° hybrid couplers and capacitive neutralization on both stages. Maximum power gain of 32.6 dB, PAE_{max} of 25.5% and P_{sat} of 17.9 dBm are measured while robustness to industrial temperature range and process spread is demonstrated. Temperature-induced performance variation compensation, as well as amplitude-to-phase modulation (AM-PM) optimization regarding output power back-off, are achieved through body-bias node. This PA exhibits an International Technology Roadmap for Semiconductors figure of merit (ITRS FOM) of 26 925, the highest reported around 30 GHz to authors' knowledge.

Introduction

The race for high-data rates is driving the telecommunication industry into millimeter-wave (mmW) frequency bands exploration for 5 G network standardization. The frequency bands around 30 GHz are particularly attractive.

To cover several frequency bands, multi-band power amplifiers (PAs) are an interesting solution [1]. However, achieving high-performance levels over all frequency bands of interest is difficult. 5 G network will have to be adaptive as different use cases leading to different performances requirements are forecasted. To tackle this challenge, PAs with operating mode and/or frequency configurability are needed. Furthermore, efficiency/performance trade-off is still challenging for 5 G PAs. In the state-of-the-art, gain control is implemented in [2] but requires a dedicated stage while the saturated output power (P_{sat}) remains limited. P_{sat} enhancement is possible by using stacked-transistors topology but can lead to prohibitive power consumption levels [3] while 5 G networks target limited power consumption and network nodes densification.

The need for configurability and digital intensive standards drives the need for large-scale SoC integration in advanced CMOS technologies. The 28 nm FD-SOI CMOS technology demonstrated promising performances for mmW PA design [4].

To address these challenges, we propose a 31 GHz PA exhibiting a balanced topology and implemented in 28 nm FD-SOI technology from STMicroelectronics. Power gain very fine grain configuration, as well as temperature-induced performances compensation and AM-PM optimization regarding power back-off, are performed thanks to extensive usage of body-bias. This configurability achieved with relatively constant power efficiency performance; thanks to a novel output load determination strategy, enables an efficient system-level control in SoC implementation.

This article is an extended version of [5] and provides in-depth description and development about the design; from technology to design choices as well as extended measurements results.

The section "28 nm FD-SOI for mmW PA design" of this article highlights 28 nm FD-SOI flavors and the PA configurability possibilities it offers. The section "PA design" depicts the proposed PA design, topology choices as well as active and passive devices optimization. Extensive measurements and state-of-the-art comparison are available in the section "Measurements". Finally, a conclusion highlighting the main features of this work is provided.

28 nm FD-SOI for mmW PA design

Active devices and technology back-end-of-line

SOI technology differs from classical bulk CMOS by featuring an ultra-thin silicon layer over a buried oxide. This buried oxide allows several improvements compared to bulk technology:

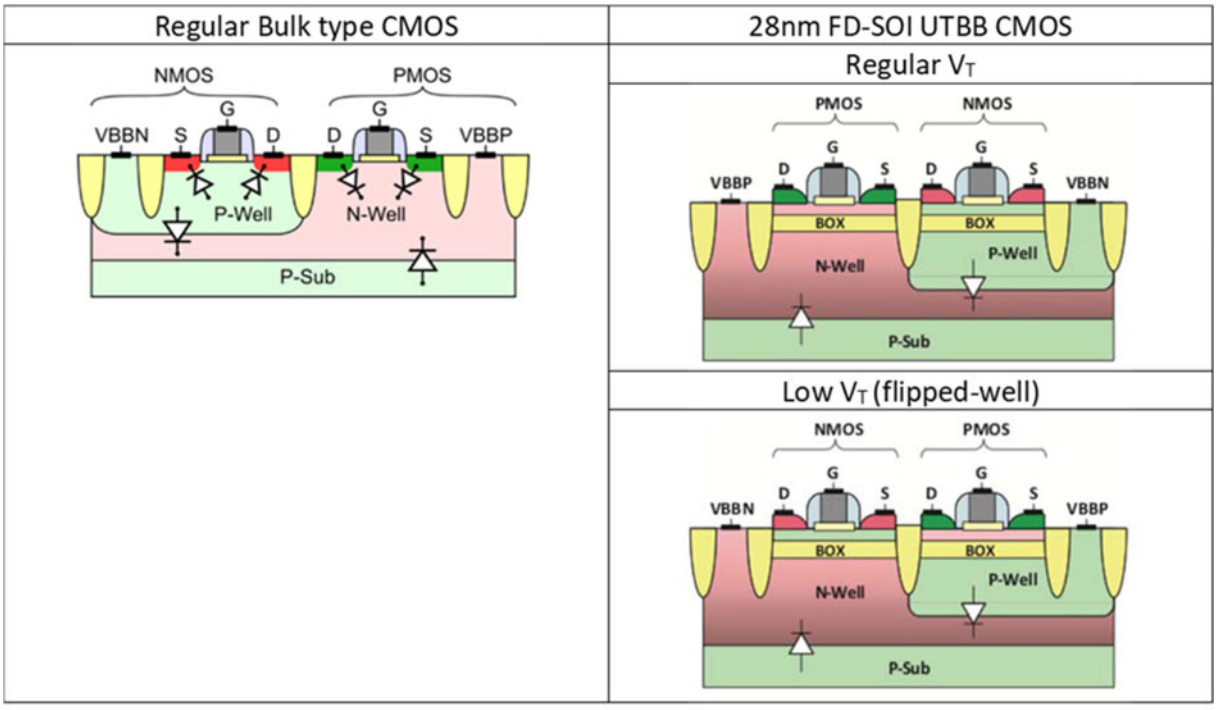

Fig. 1. Cross-section of regular Bulk CMOS technology VS 28 nm UTBB FD-SOI CMOS technology transistors.

- Channel-to-substrate leakage limitation by isolating the channel from the substrate.
- Source-to-substrate and drain-to-substrate junction diode elimination as well as source-substrate and drain-substrate parasitic capacitance limitation.
- An additional control lever through substrate voltage, the body-bias, allowing threshold voltage (V_T) variation.

Two transistors types are available in the technology. "Regular V_T" (RVT), similar to bulk transistors, and "low V_T" (LVT) transistors featuring a flipped-well structure with lower threshold voltages for both NMOS and PMOS transistors. A comparative cross-section scheme featuring regular CMOS bulk and 28 nm FD-SOI technology transistors is available in Fig. 1 [6].

Forward and reverse body-bias (V_{body}) can be applied to those active devices. V_{body} range is limited by parasitic diodes in the well. Indeed, if those diodes are not kept in a blocked state, harmful excessive currents (for FBB) and critical breakdown (for RBB) can occur. Table 1 lists those biasing modes and their limits. Figure 2(a) highlights the achievable V_T range through body-bias node [6]. In the particular case of NLVT transistor, a very large variation of 250 mV is achieved through body-bias while on a classical bulk CMOS transistor only a few mV of V_T variation can be reached, see Fig. 2(b).

Another advantage of this technology for mmW circuit design is the high f_t and f_{max} achieved values. Metal1-Pcell for a NLVT transistor with a gate length (L_g) of 30 nm, a number of fingers (N_f) of 20, and a finger width (W_f) of 800 nm achieves a f_t and f_{max} of respectively, 295 GHz and 394 GHz. Measurements with an optimized BEOL reported a f_t of 256 GHz and f_{max} of 346 GHz [7].

In this work, we used the 28 nm FD-SOI CMOS technology with a back-end-of-line featuring 10 metal layers. This stack-up is composed of:

- Six thin copper metal layers of the same thickness named M1 to M6.
- Two intermediary copper metal layers with identical thickness named B1 and B2.
- Two thick copper metal layers named IA and IB.
- A thick AluCap named LB.

While the thin metal layers are particularly useful for digital routing, their high resistivity is too large for radio-frequency (RF) applications like RF path routing or passive devices implementation. The RF routing must be implemented on the thickest metal layers IA and IB while B1 and B2 are useful for crossing – particularly if they are stacked – where additional metal layers are needed. An illustration of the 10 metal layers 28 nm FD-SOI CMOS technology used in this work is available in Fig. 3.

Body biasing and PA tuning capability

To illustrate the PA configurability achievable through body-bias, $I_D = f(V_{GS})$ curves of a NLVT transistor ($L_g = 30$ nm, $N_f = 50$, $W_f = 1$um) for a fixed V_{DS} of 1 V are plotted in Fig. 4, featuring body-bias variations.

To achieve a higher I_D level, corresponding to switching operating class from Class AB to Class A, it is possible to either increase V_{GS} by 275 mV or set the body-bias to 3 V. Therefore, a small variation of V_{GS} leads to a large drain current variation while body-bias dynamic range is wider and allows very fine-tuning of operating class through V_T variation. This tuning ability has been used in the proposed circuit and has also been used in [4, 8] for pseudo-Doherty implementation.

In the proposed circuit simulations, we estimated that a 100 mV increase of V_{GS} implies 6.7 dB gain improvement. A V_{body} increase of 100 mV leads to only 0.8 dB gain enhancement. Fine gain control is then enabled by the body-bias and does not require any dedicated stage nor adds complexity to the signal path.

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Table 1. 28 nm FD-SOI CMOS technology transistors body biasing mode, limits and nominal voltage

Transistor Type	Biasing mode and limits (V)	Nominal body biasing
LVT NMOS	FBB: -3 to -0.3 to +3	GND
LVT PMOS	FBB: -3 to +0.3 to +3	GND
RVT NMOS	RBB: -3 to $\frac{V_{DD}}{2}+0.3$ to +3	GND
RVT PMOS	RBB: -3 to $\frac{V_{DD}}{2}-0.3$ to +3	VDD

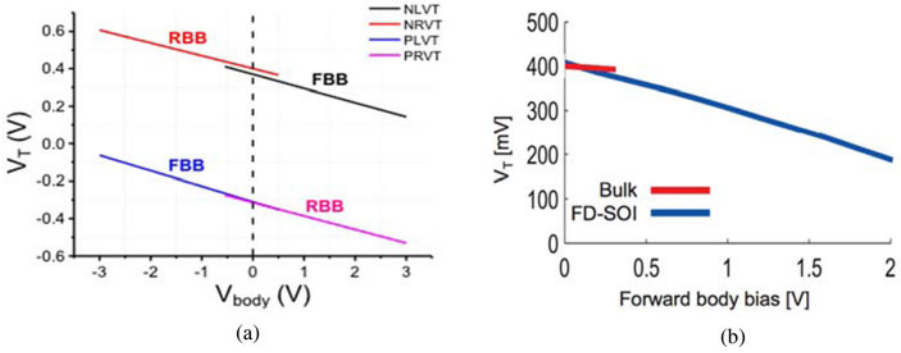

Fig. 2. (a) V_T achievable range with NMOS and PMOS LVT and RVT transistors at minimum gate length in 28 nm FD-SOI. (b) Forward body biasing induced V_T variation comparison between Bulk and 28 nm FD-SOI technologies (NMOS).

PA design

Overall topology

In this work we identified and focused on several challenges related to 5 G PA design:

- The PA is the most power-consuming block in modern transceivers and a challenge of 5 G is to limit the network power consumption while densifying the number of cells. Therefore, PA with limited power consumption and high efficiency is needed.
- Complex modulation schemes used in 5 G with high PAPR leads to stringent linearity requirements.
- High-gain levels are needed. Gain configurability as well as performances and power consumption adaptability allow system-level control for SoC.
- In beamforming phased array, the environment of individual PA differs and can lead to impedance mismatch. This can produce harmful voltage overshoot at the output of individual PA.

To tackle these challenges, we implement a balanced topology. This type of topology offers robustness to input/output impedance mismatch that could occur in beamforming phased array. As it performs power combining, P_{sat} and $P_{1\,dB}$ are improved by 3 dB. The balanced topology reduces IM_3 by 6 dB and offers

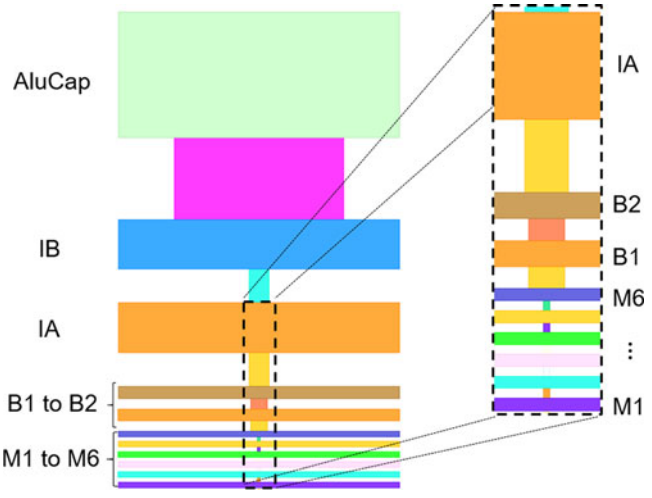

Fig. 3. 10 metal layers 28 nm FD-SOI CMOS technology back-end-of-line illustration.

ACPR improvements compared to an individual amplifier with the same topology.

Both amplification paths of the balanced PA are identical. As we target a high PAE and limited power consumption

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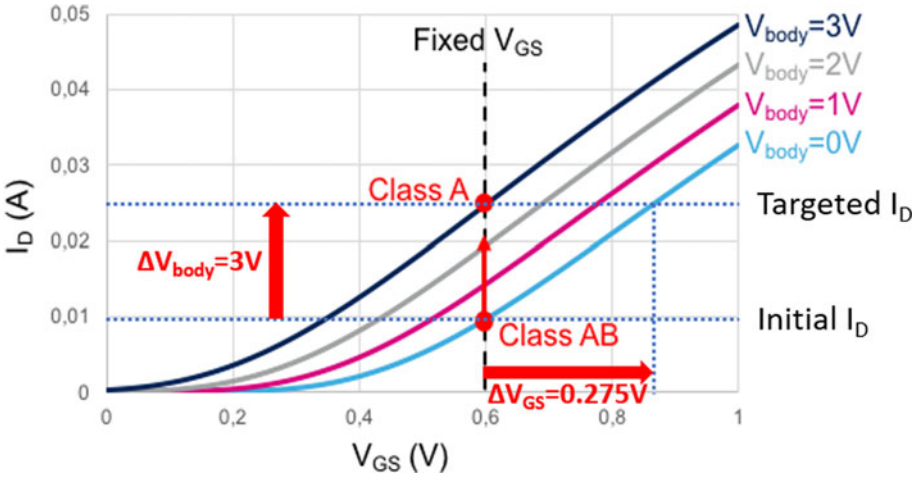

Fig. 4. V_{GS} and V_{body} dynamic comparison for fixed I_D level target for Class AB to Class A shifting.

simultaneously with a high gain, we limit the number of amplification stages to two stages.

Differential topology is used for both amplification stages. It provides additional power combining and higher stability thanks to a dynamic virtual ground compared to a single-ended amplifier. Indeed, single-ended are highly sensitive to ground return path parasitic, possibly leading to oscillations. The dynamic virtual ground between two differential paths in a differential architecture make the circuit ground insensitive to the ground path parasitic and therefore provides better stability than single-ended PAs.

Baluns and transformers in a differential design offers enhanced reliability and robustness by providing electrical and galvanic isolation between stages. It also allows the use of center-tap to apply voltages and eliminates the need of DC blocking capacitance on RF path and choke inductors with large area footprint.

To achieve satisfying linearity in multi-stage PAs, each stage must be linear enough to not degrade the linearity of the next stage. It means that the OCP1 of each stage must be higher than the ICP1 of the following one. The body-bias used to improve the gain has a negative impact on the OCP1. Therefore, to keep the best overall linearity performances we implement the body-bias on the last amplification stage on V_{b_CS} node.

All the layout optimizations discussed in the following sections strictly respect the DRC and ERC rules. Electromigration conditions fulfilment is also checked carefully. For the most extreme encountered measured conditions – corresponding to a maximum body-bias value at saturated output power from the measurements in the section "Measurements" – electromigration rules are fulfilled for 10 years of operation at 100°C. By applying the lifetime derating indicated in the design rules manual, 2 years of continuous operation under those extreme conditions are achievable with electromigration reliability fulfilled at 125°C.

The overall PA topology is available in Fig. 5(a).

Transistor design

In deep sub-micron technology mmW circuit implementation, transistor sizing and design optimization are crucial. The transistor total width of both amplification stages is chosen for a current density of 220 µA/um to maximize f_{max}. For this current density, a gate length of 60 nm shows quasi the same f_{max} than the minimal gate length of 30 nm (Fig. 6(a)).

Finger width parameter has an influence on both f_t and f_{max}, linked to intrinsic gate resistances and capacitances. To find the optimum W_f we simulate f_t and f_{max} of a Metal1-Pcell transistor with a fixed 400 µm total width (W_{tot}). Results are available in Fig. 6(b). The optimum finger width in this technology is then 1 µm, as it is a trade-off between f_t and f_{max}.

Thanks to the technology margins offered by the technology, this design around 30 GHz can be carried out with a non-minimal 60 nm gate length transistors, ensuring comfortable transconductance. The use of non-minimum gate length transistors offers several advantages over performances and robust integration. An increased L_g reduces the current per gate finger at high power and thus limits the stress related to electromigration. Local process variability risk, leading to performance dispersion between chips, is also reduced. Higher L_g also limits gate resistance (R_G) and C_{GD}/C_{GS} ratio. C_{DS} parasitic capacitance is also limited and eases output matching.

A specific layout optimization strategy has been adopted to maximize f_t and f_{max} and reduce parasitic interconnects. A double gate access has been designed to reduce R_G, enhancing f_{max}. It also provides higher robustness regarding high power induced stress compared to a single access. A staggered structure is implemented for drain and source connections. It consists of an iterative reduction of the metallic finger length from lower to higher metal layers. This limits drain and source parasitic resistances thanks to metal stacking as well as C_{DS} as less surface is in regard between drain and source interdigitated fingers. Fringe capacitance to ground is also limited for f_t and f_{max} enhancement. Simulated effective f_t for the Metal1-Pcell is 220 GHz while with the fully optimized back-end-of-line 190 GHz is achieved. A 3D view of the transistor layout is available in Fig. 7.

To optimize the overall layout, each transistor of both amplification stages is subdivided into 32 µm W_{tot} elementary transistor cells. Under all operating conditions, all the active devices remain in their safe operating area. This specific transistor optimal design has been carefully implemented to fulfil all DRC rules.

Amplification stages design

Two distinct amplification stages have been designed. Their topology is exhibited in Fig. 5(b).

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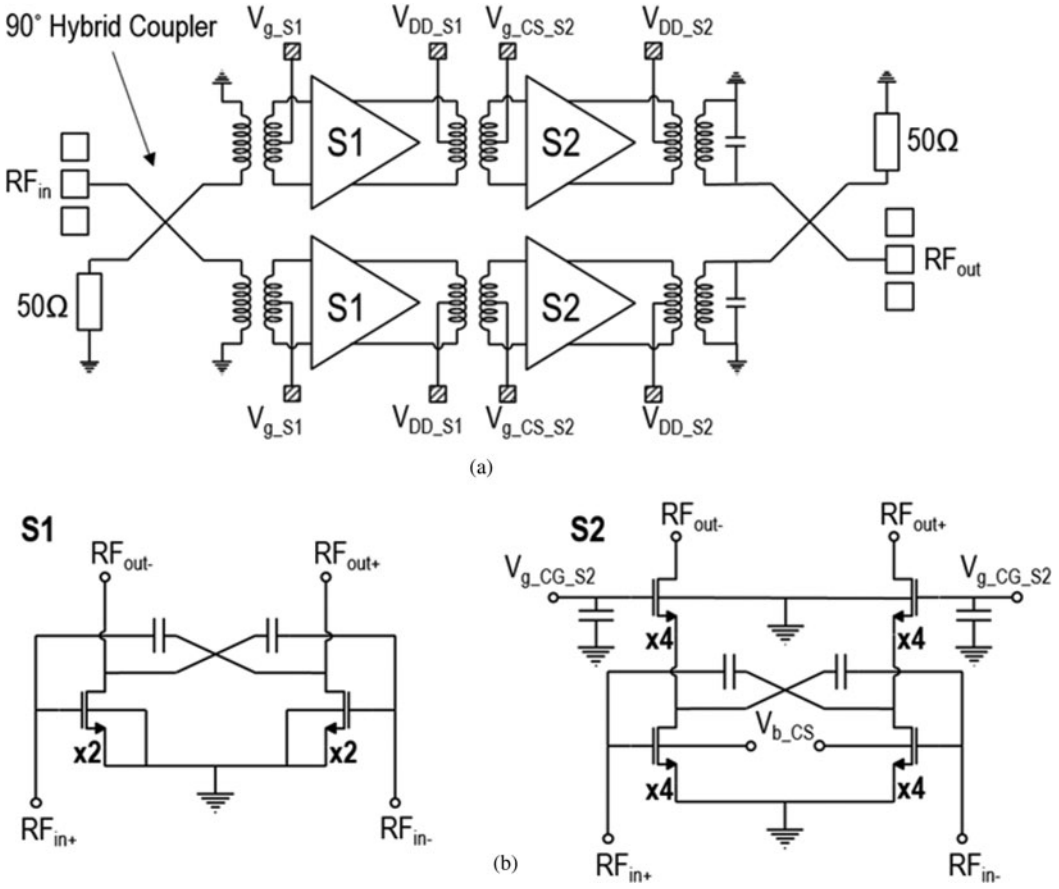

Fig. 5. (a) Proposed PA overall topology. (b) Amplification stages.

The first amplification stage (S1) consists of a differential LVTNMOS common-source. It is operated in linear Class A and delivers a fixed gain to respect the overall linearity specification. It is fed by a 0.7 V power supply to improve efficiency. Capacitive neutrodyne neutralization using 16fF MOM capacitors is performed to compensate C_{GD} [9] and improves both gain and reverse isolation. W_{tot} of the transistor used in this stage is 64 µm, subdivided in 2×32 µm elementary transistors.

The second amplification stage (S2) exhibits a differential cascode architecture to enhance the bandwidth, reverse isolation, and output power. It is supplied by a 1.98 V power supply. 32fF capacitive neutrodyne neutralization is realized for the same reason than in S1. *CG* and *CS* transistors of the cascode architecture both have a W_{tot} of 128 µm, subdivided in 4×32 µm elementary transistors. Interconnections have been optimized to limit parasitics.

Forward body-bias is applied on V_{b_CS} node to achieve a very fine grain wide gain range control. For V_{b_CS} varying from 0 V to 1.65 V, V_T decreases linearly from 326 mV to 184 mV. This enables S2 continuous operating class shifting from Class AB to Class A.

A novel approach for S2 output matching is proposed in this work.

Traditionally, load-pull simulations under nominal operating conditions are used to determine the output load, maximizing both PAE and output power. Load-pull simulations results for both Class AB and Class A modes are available in Fig. 8. An optimal output load impedance of $Z_{load\_Class-AB} = 41 + j67\ \Omega$ is defined for Class AB operation while in Class A the optimal

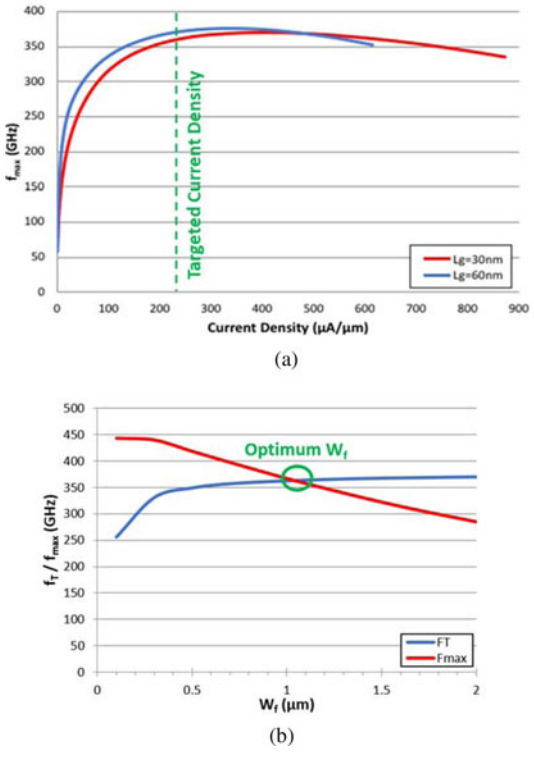

Fig. 6. (a) f_{max} comparison between gate length of 60 nm and 30 nm. (b) f_t and f_{max} versus gate length for a fixed 400 µm transistor.

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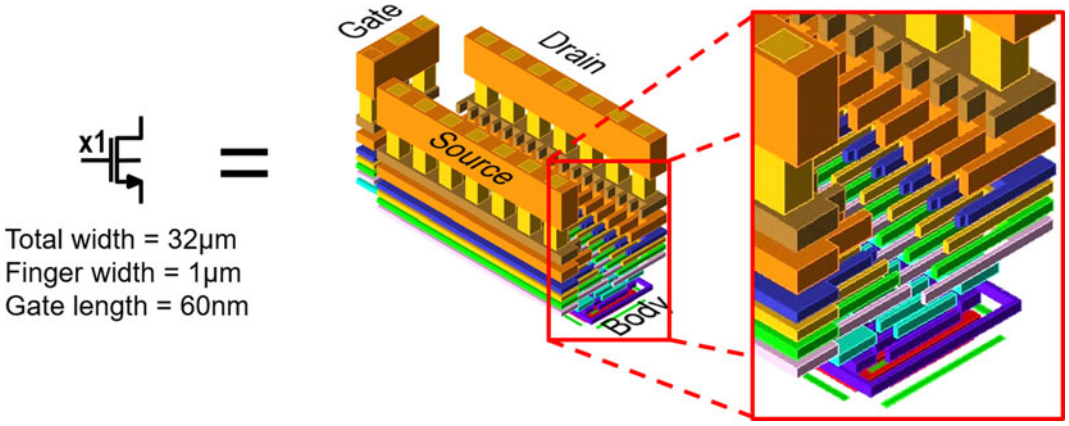

Fig. 7. 3D view of the elementary transistor cell with optimal layout.

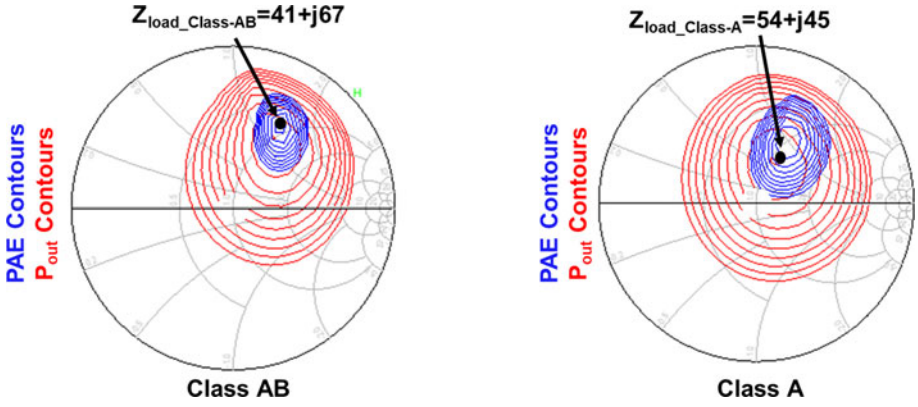

Fig. 8. Load pull simulation results for Class AB and Class A modes of operation and associated optimum output impedances.

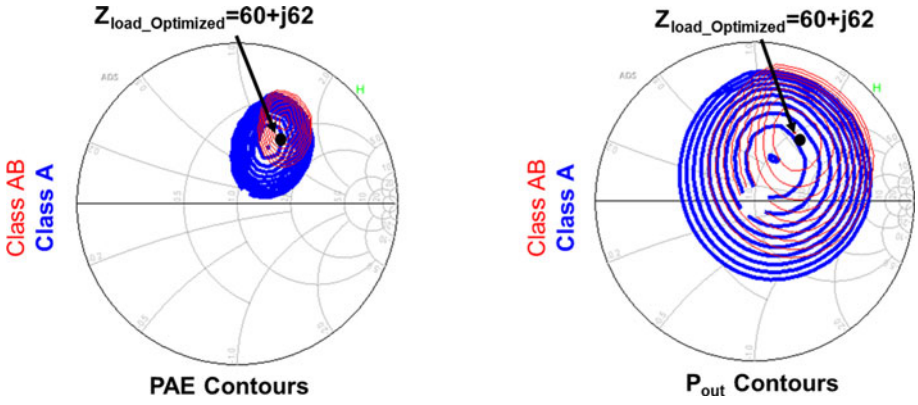

Fig. 9. Optimum output load determination strategy illustration.

output impedance is $Z_{load\_Class-A} = 54 + j45\ \Omega$. Therefore, choosing between one of those two different optimal impedances privilege one mode among the other. Generally, this choice is made to privilege the linear operation mode.

In this work, we focus on optimal matching for all modes of operation. Therefore, the choice of output load is made as a compromise between P_{sat} and PAE_{max} Smith charts contours for all modes enabled by body-bias variation. Therefore, instead of advantaging one mode among the other, the load is optimum for all modes, from Class AB to Class A. This is illustrated in Fig. 9. This choice ensures a quasi-constant PAE_{max} under all operating modes and the optimal output impedance for all modes is $Z_{load\_Optimized} = 60 + j62\ \Omega$.

Passive design and optimization

90° Hybrid coupler

The balanced topology implementation requires the use of 90° hybrid couplers. Several distributed 90° hybrid couplers topologies are reported in the literature, like branch-lines or coupled-lines couplers [10] and have been used extensively for MMIC. However, regular 90° hybrid couplers on-chip integration in deep sub-micron CMOS technology is challenging for 5 G mmW frequency bands as they are based on the use of $\lambda/4$ transmission lines. Indeed, those lines suffer from a large area footprint around 30 GHz and the induced losses on RF path can degrade the overall system efficiency.

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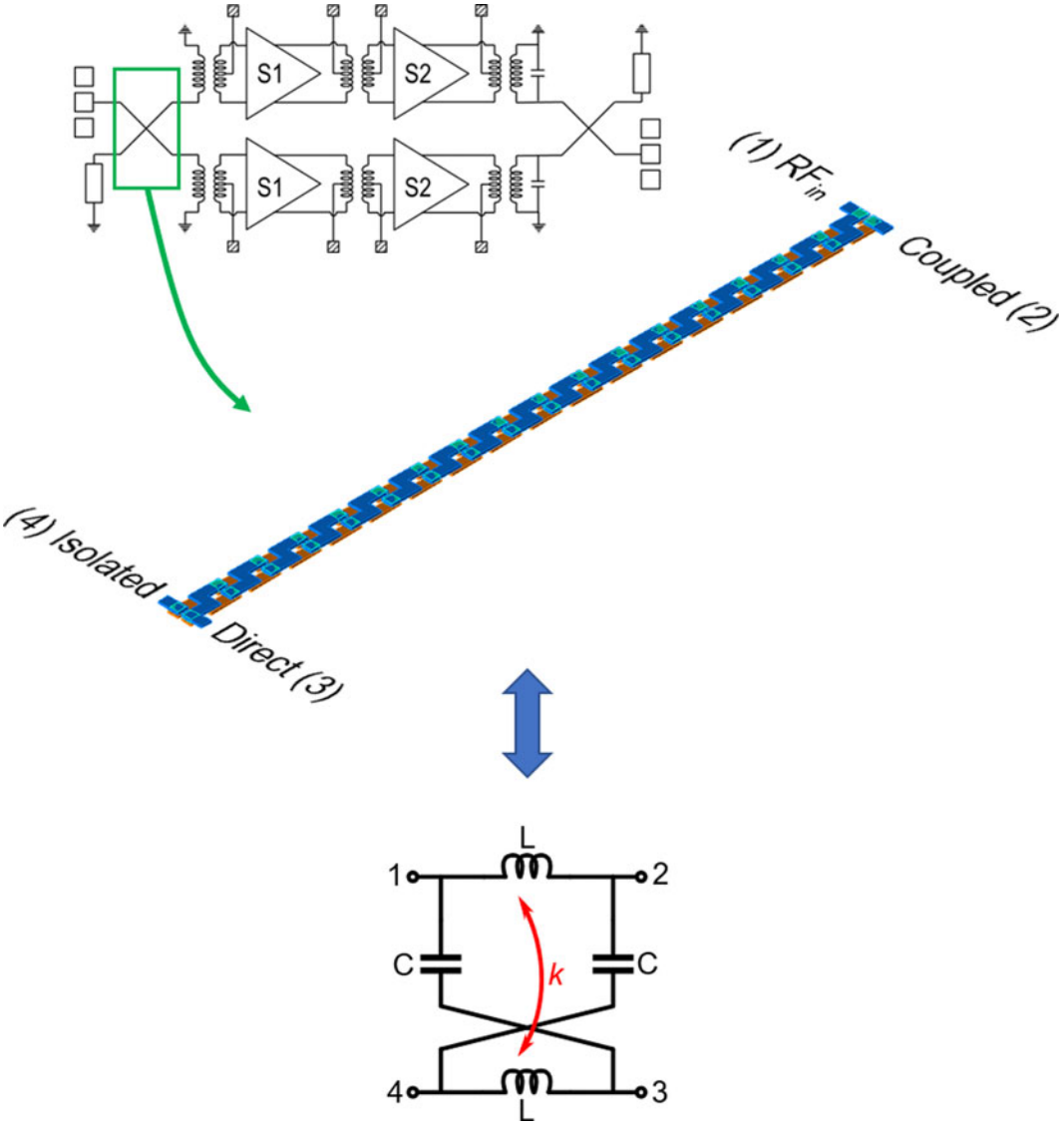

Fig. 10. Quadrature hybrid coupler design and associated lumped elements model.

Recently, a compact distributed quadrature hybrid coupler featuring a twisted design has been introduced in [11], its size and design flexibility allowing a pragmatic design. This design has been validated in 28 nm FD-SOI CMOS technology in [8] and demonstrated robustness to 3:1 VSWR conditions. In this work we implemented this promising topology.

This section details the design procedure developed in [8, 11].

The distributed quadrature hybrid coupler can be seen as a simple lumped elements model as shown in Fig. 10.

Lumped elements C and L values are defined by equations (1) and (2) with Z_0 the characteristic impedance of the coupler, f_0 its central frequency and k the coupling coefficient.

$$L = \frac{Z_0 \cdot (2-k)}{\omega_0}, \tag{1}$$

$$C = \frac{(2-k)}{Z_0 \cdot 2\omega_0}. \tag{2}$$

To synthetize these values, the starting point is a unitary cell as the one shown in Fig. 11. Inductances and capacitances are distributed along the two tracks. The unitary inductance L_u, capacitance C_u and resistance R_u can be extracted with electromagnetic (EM) tools. The hybrid coupler can then be designed by cascading N unitary cells; and the total inductance, capacitance, and resistance values are defined as in equations (3)–(5).

Couplers are implemented in the two thickest copper metal layers offered by the technology, IA and IB, to limit losses and the unitary cell dimensioning is made to respect DRC rules while providing enough inductance and capacitance values as well as a limited resistance on each track. The use of quadratic hybrid coupler improves the robustness to impedance mismatch, matching, isolation and stability in the overall PA topology.

$$L_{tot} = N \cdot L_u, \tag{3}$$

$$C_{tot} = N \cdot C_u, \tag{4}$$

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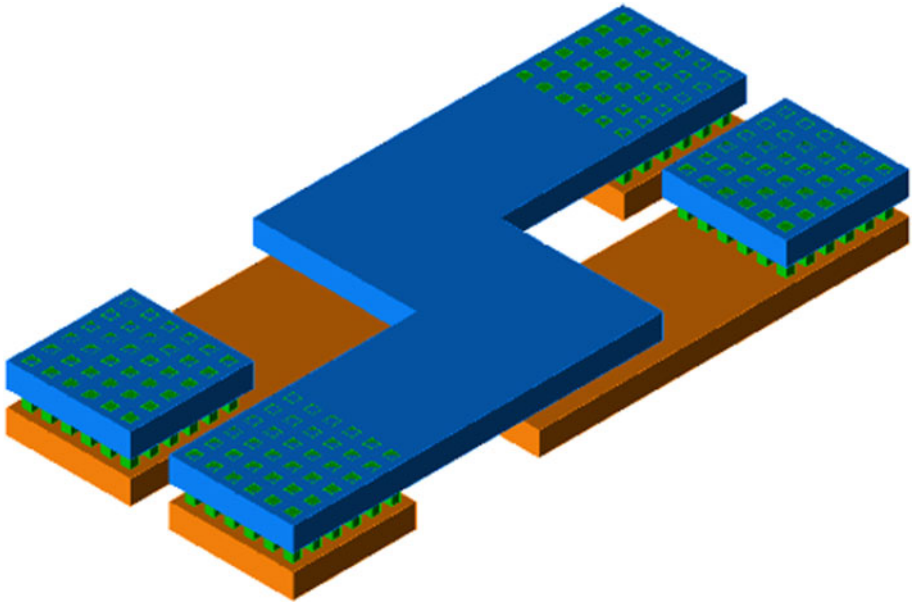

Fig. 11. Unitary cell for quadrature hybrid coupler design.

Table 2. S1 and S2 stages optimum input/output impedance values

$Z_{out\_opt\_S2}$ [Ω]	60 + j62
$Z_{in\_opt\_S2}$ [Ω]	10 + j52
$Z_{out\_opt\_S1}$ [Ω]	58 + j106
$Z_{in\_opt\_S1}$ [Ω]	15 + j102

$$R_{tot} = N \cdot R_u. \quad (5)$$

Output, inter-stage and input impedance matching network

Table 2 sums up the optimal input and output impedances for both amplification stages S1 and S2. From these values, the impedance transformations are made by using baluns and transformers. The output load matching to 50 Ω is synthesized with a flipped balun in a stacked configuration, performing also the differential-to-single-ended conversion. The primary winding is featuring two turns and is implemented on IB metal layer with a 6 µm width. The crossing between the two turns is made on IA metal layer to keep the advantage of the low resistivity of those thick metal layers and avoid additional loss. The secondary winding is positioned over the second turn of the primary to maximize the coupling and is implemented on LB AluCap, with a 6 µm width. S2 supply voltage is applied through the primary winding center tap. A 105fF capacitance is inserted between the two secondary winding terminations to refine the balun central frequency and broadens the bandwidth. A 28 GHz bandwidth – from 22 GHz to 50 GHz – is achieved while insertion losses are lower than 1 dB from 14 GHz. A 3D view of the output balun and post-layout simulations performances are available in Fig. 12.

As both amplification stages, S1 and S2 have a differential topology, the inter-stage matching network is realized with a transformer. Both primary and secondary windings use a single-turn configuration. The primary and secondary winding are implemented on IB and LB metal layers respectively, with a 6 µm width. The primary winding center tap is used to apply S1 supply voltage while the secondary winding is used to apply the gate bias for the common-source stage of the cascode topology in S2. Insertion loss under 1 dB is achieved from 17 GHz while a 6 GHz bandwidth centered at 34 GHz is obtained. A 3D view of the inter-stage transformer, as well as post-layout simulations results, are available in Fig. 13.

Finally, the input matching network performs both single-ended-to-differential conversion and impedance transformation from 50 Ω to $Z_{in\_opt\_S1}$. For this purpose, it is implemented with a stacked flipped balun. The secondary winding has a 3-turns topology implemented on IB. The crossings between turns and parts of the 2nd and 3rd turns are implemented on IA due to DRM constraints and to avoid additional loss due to the lower resistivity of thinner metal layers. The single-turn primary winding is stacked over the second turn of the secondary winding to maximize coupling. The center tap of the secondary winding is used to apply S1 gate bias. Insertion loss under 1 dB is achieved from 30 GHz and a bandwidth of 7 GHz, centered at 34 GHz, is obtained. Figure 14 presents a 3D view and the post-layout performances for this input balun.

Measurements

The overall PA layout has been optimized in respect with electromigration requirements up to 125°C and density rules targeting industrial requirements. The proposed PA has been manufactured in 28 nm UTBB FD-SOI CMOS featuring 10 metal layers. A photomicrograph of the manufactured chip is available in Fig. 15.

In this section, small-signal, large-signal, and AM-PM measurements are presented. A robustness and reliability evaluation is also reported and provides a statistical study as well as measurements under different temperature of operation up to 125°C.

Small-signal measurements

Small-signal measurements have been performed on 20–40 GHz frequency range. The body-bias voltage is varied from 0 V to 1.65 V. S-parameters measurement results are plotted in Fig. 16.

The small-signal gain is improved with the V_{b_CS} increase. It goes incrementally from a maximum of 21.9 dB for $V_{b\_CS} = 0$ V

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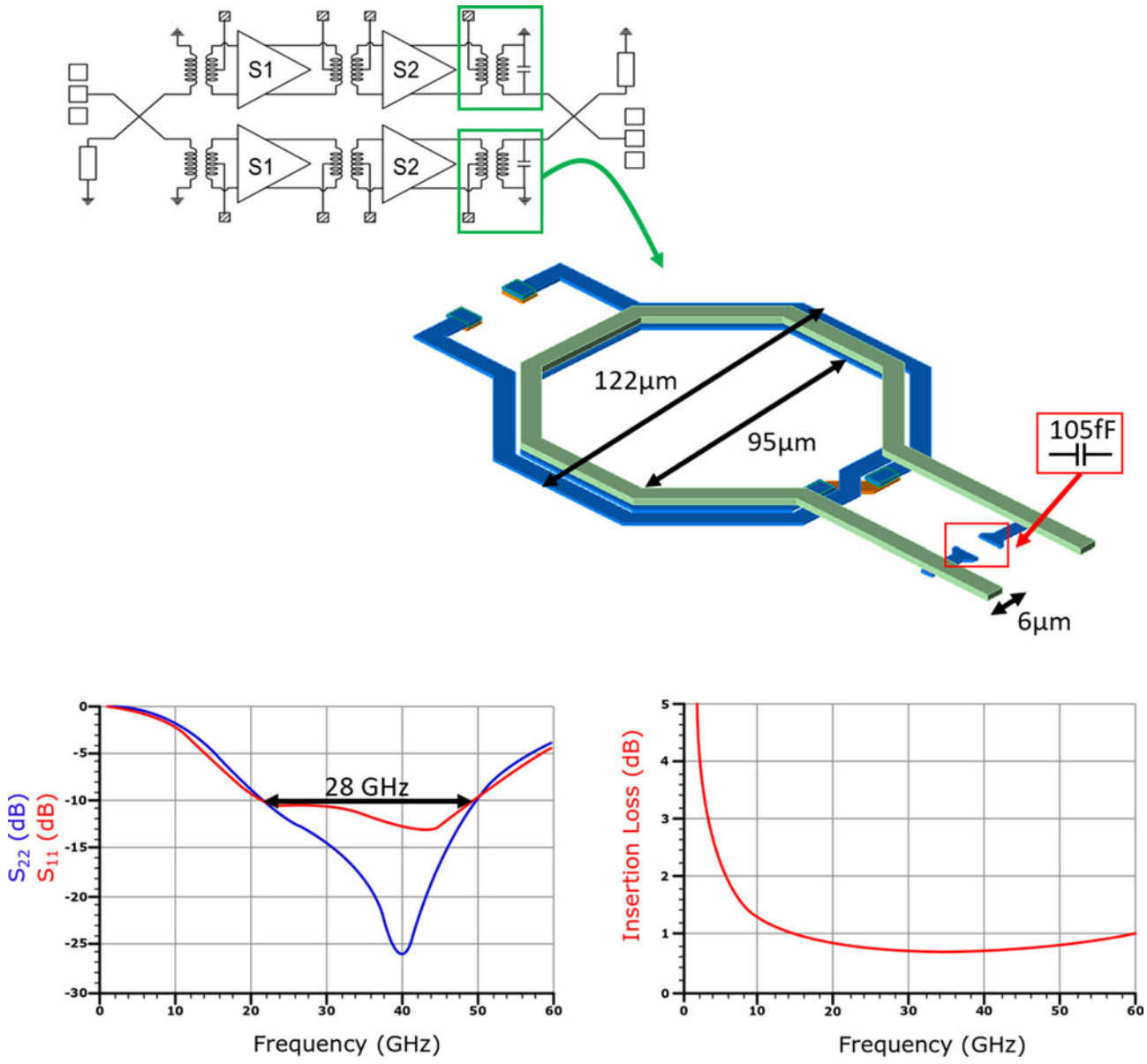

Fig. 12. Output balun 3D view, dimensions and post-layout simulations results.

to reach 32.6 dB when $V_{b\_CS} = 1.65$ V at 31 GHz. A maximum 3 dB bandwidth ($BW_{3\,dB}$) of 6 GHz is measured. It covers the targeted 5 G frequency band from 31.8 GHz to 33.4 GHz under all V_{b_CS} conditions. This behavior illustrates the dynamic gain control with a range of over 10 dB enabled by the body-bias over the targeted frequency band.

S_{11} and S_{22} curves show good 50 Ω matching and stable conditions met overall V_{b_CS} range. S_{12} plot highlights a 35 dB reverse isolation overall body-bias conditions. This good isolation is achieved thanks to the topology choices depicted in the previous section.

Large signal measurements

Power gain, PAE and power consumption measurements under continuous-wave for a large input sweep at 31 GHz are available in Fig. 17.

The power gain graph confirms the wide gain tuning behavior highlighted in the previous section and enabled by body-bias setting. The power gain range goes from 21.9 dB for $V_{b\_CS} = 0$ V with incremental steps up to 32.6 dB when $V_{b\_CS} = 1.65$ V. A $P_{1\,dB}$ of 15.3 dBm is achieved for $V_{b\_CS} = 0$ V with a 0.9 dB gain expansion confirming Class AB operation. With $V_{b\_CS} = 1.65$ V, the gain curve is typical for Class A operation while $P_{1\,dB}$ reaches 11.6 dBm.

Therefore body-bias offers continuous class shifting and two extreme operating modes can be identified:

- High-linearity mode for $V_{b\_CS} = 0$ V
- High-gain mode for $V_{b\_CS} = 1.65$ V

The P_{sat} reaches 17.3 and 17.9 dBm for the high-linearity and the high-gain modes, respectively.

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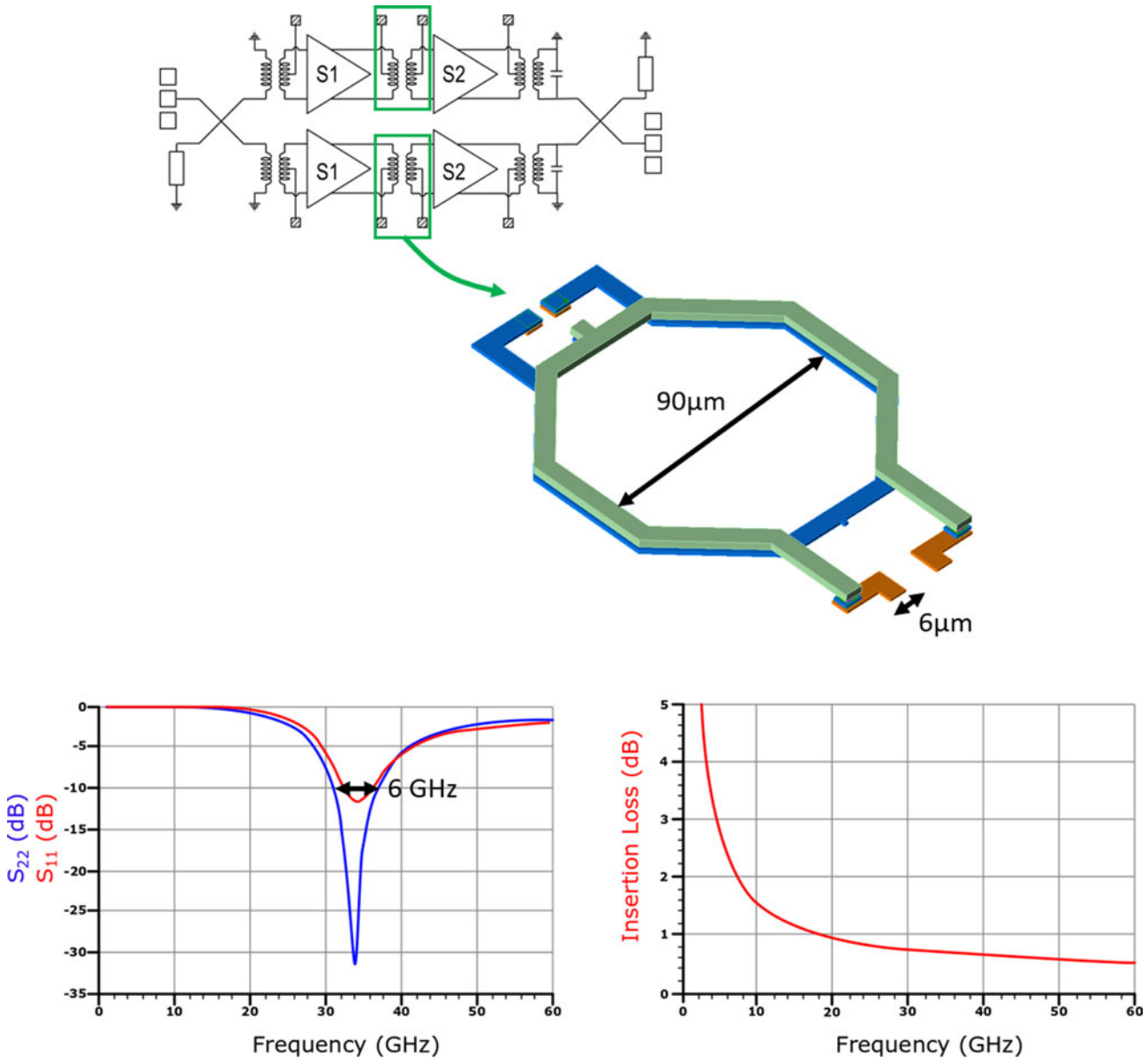

Fig. 13. Inter-stage transformer 3D view, dimensions and post-layout simulations results.

PAE_{max} is 24.7% in high-linearity mode and reaches 25.5% in high-gain mode. As expected, PAE_{max} is quasi the same for all operating modes thanks to the output load optimization strategy.

Back-off efficiency is an important parameter to evaluate. In this work, PAE at 6 dB P_{sat} back off is over 10% in all modes and is slightly affected by V_{b_CS} settings.

The presented PA has a P_{DC} of 76.1 mW in high-linearity mode and reaches 140.2 mW in high-gain mode. It is then possible to operate the PA in the high-linearity mode most of the time and use the high-gain mode when an extreme gain is necessary. Therefore, it is possible to control and limit the average power consumption in the overall system.

These measurements clearly highlight the wide range of fine-grain tuning abilities offered by the body-bias in SOI technology. This type of adaptability is useful to compensate for any performance drift that could occur during the manufacturing process or environment of operation, allowing robust adaptive systems.

Large signal measurements have also been performed between 28 GHz and 35 GHz for both high-linearity and high-gain modes. Results are reported in Fig. 18.

From 30 GHz to 33 GHz, a PAE_{max} over 20% is achieved under both operating modes while P_{sat} remains over 6 dBm. The maximum $PAE_{-1\,dB}$ measured is 21% at 31 GHz corresponding to 15.3 dBm $P_{1\,dB}$ in high-linearity mode.

These measurements confirm the PA performances suitability for applications on the 31.8 GHz to 33.4 GHz expected 5 G frequency band.

AM-PM measurements

AM-PM measurements have been performed at 31 GHz for both extreme operating modes and the results are available in Fig. 19.

The curve for $V_{b\_CS} = 0$ V presents a typical Class AB behavior. A phase expansion with a maximum deviation of 12.7° from the normalized origin is reached and is linked to the gain expansion

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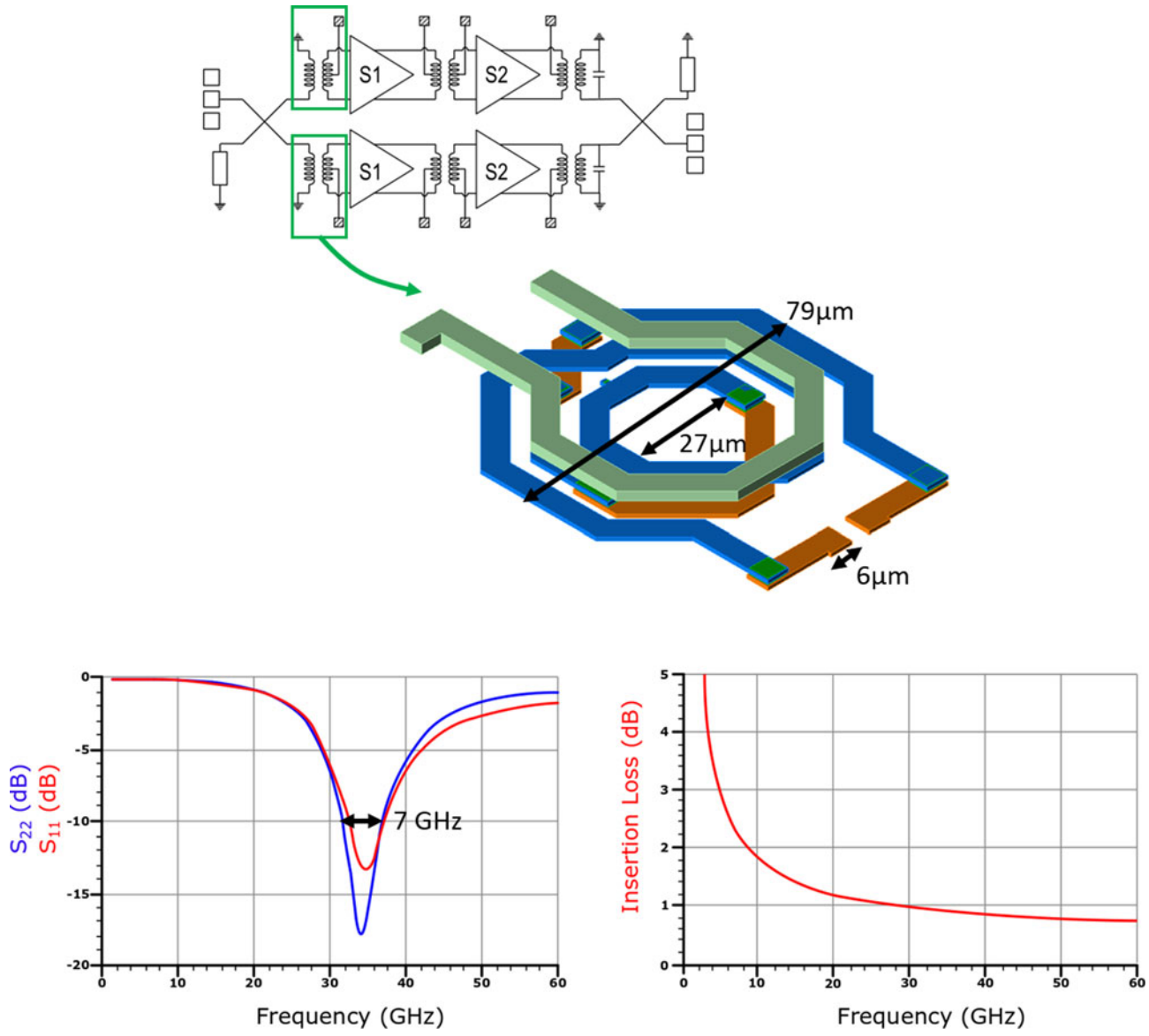

Fig. 14. Input balun 3D view, dimensions and post-layout simulations results.

typical in Class AB. For $V_{b\_CS} = 1.65$ V, AM-PM curves show typical Class A behavior. When the gain is flat and output power is low no phase deviation occurs. The phase then decreases sharply when the output power is close to the OCP1 (−21.6° at $P_{1\,dB}$). High phase deviation is then reported during compression up to saturation. Intermediary values of V_{b_CS} lead to intermediary AM-PM curves.

It is noticeable that at high output power levels, $V_{b\_CS} = 0$ V is leading to the lowest phase variation. In the output power range between 4.5 and 11.2 dBm, $V_{b\_CS} = 0.25$ V achieves the lowest AM-PM variation among all other modes. Finally, under 4.5 dBm output power level, all operating conditions show very low phase deviation.

It is then possible to plot the optimized AM-PM curves enabled by body-bias where V_{b_CS} is set to its optimal value depending on output power back-off to compensate AM-PM variations.

Therefore, the dynamical class shifting enabled by body-bias allows dynamical AM-PM setting to achieve desired trade-off between gain, output power, linearity, and consumption performances.

Robustness and reliability evaluation

On-wafer variability statistical study

A statistical study has been performed to evaluate induced on-wafer variability. For this purpose, large-signal measurements on 13 on-wafer occurrences of the same circuit on one wafer have been realized using the same operating conditions. Performances in both extreme operating modes have been evaluated. The results and the corresponding average and standard deviation values are available in Fig. 20.

A very low standard deviation has been measured for all modes with a maximum of 0.08 dB for P_{sat}, 0.62 dB for power gain, and 0.35% for PAE_{max}.

This has been possible to achieve thanks to the design choices made at an early stage and the limited technology process spread.

Measurements under various temperature of operation between 25°C and 125°C

Robustness to temperature variations has been evaluated with large-signal measurements on 25–125°C temperature range with

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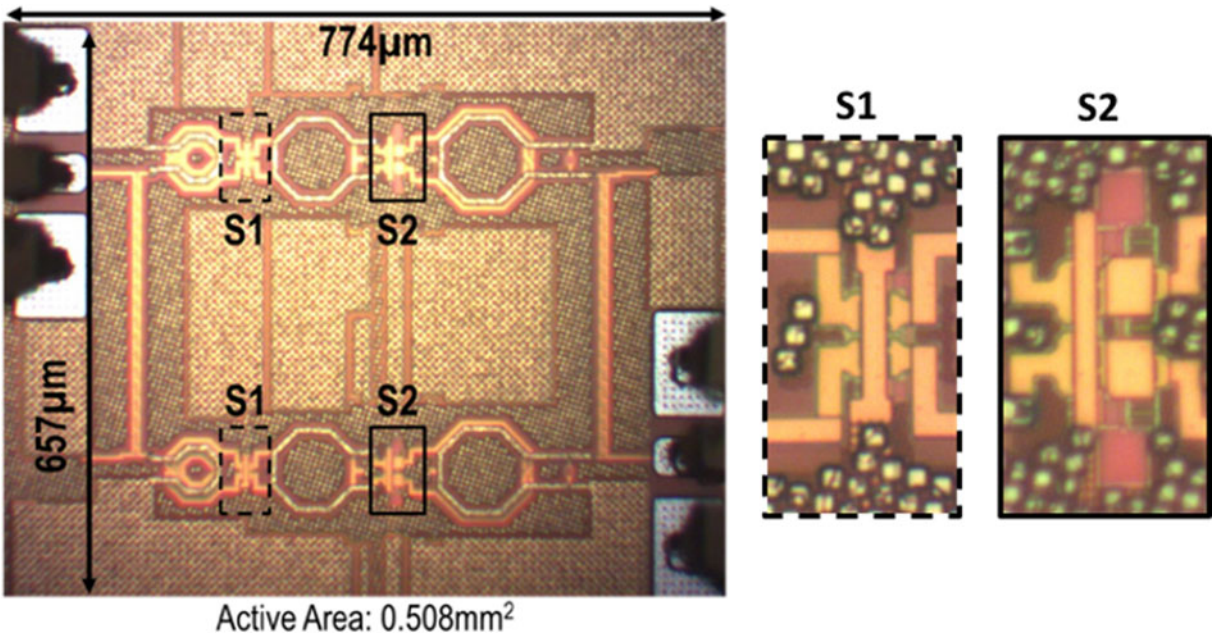

Fig. 15. Manufactured power amplifier photomicrograph.

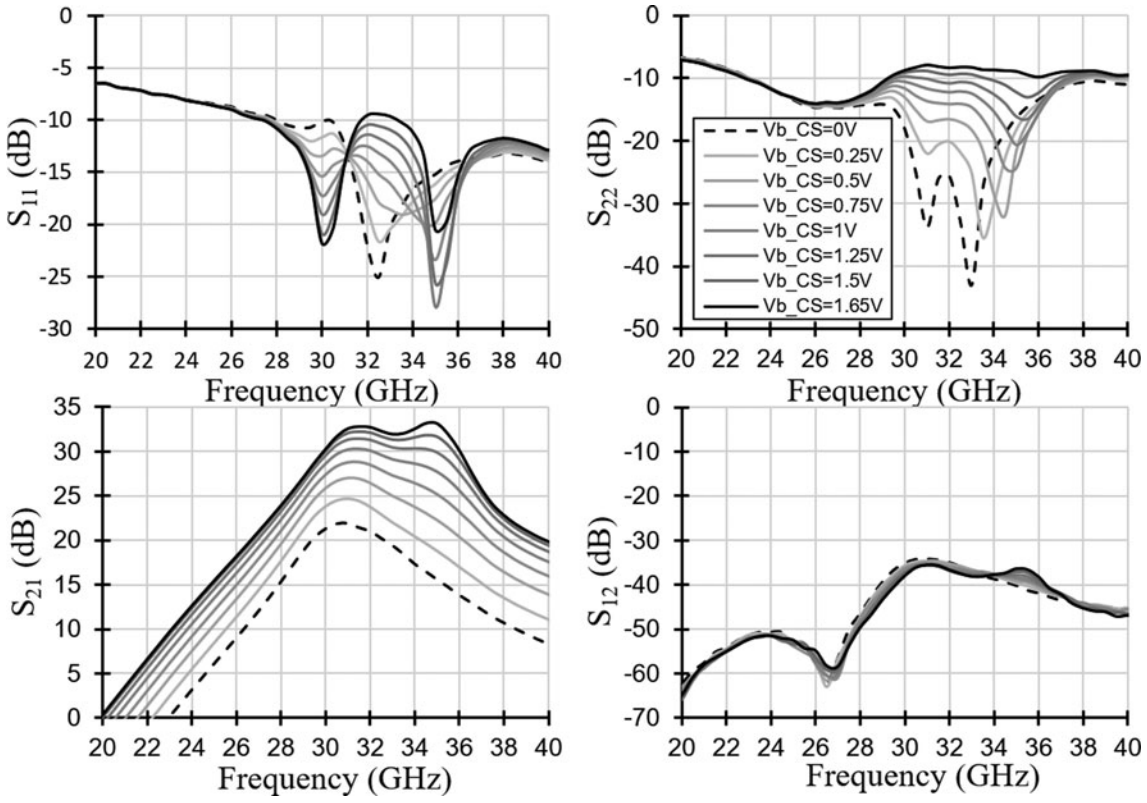

Fig. 16. Measured S-Parameters with body biasing continuous tuning.

V_{b_CS} varying from 0 V to 1.65 V. Measurements results are available in Fig. 21.

The measured performances modifications induced by the temperature increase can be explained by its physical impact on the chip with the occurrence of two distinct effects.

When the temperature is increased, internal transistor parameters are modified. It affects the V_T that decreases while temperature increases. This induced V_T reduction leads to a higher drain current level for a fixed V_{DS}, in the same way, that it can be done with body-biasing at ambient temperature. Therefore, it

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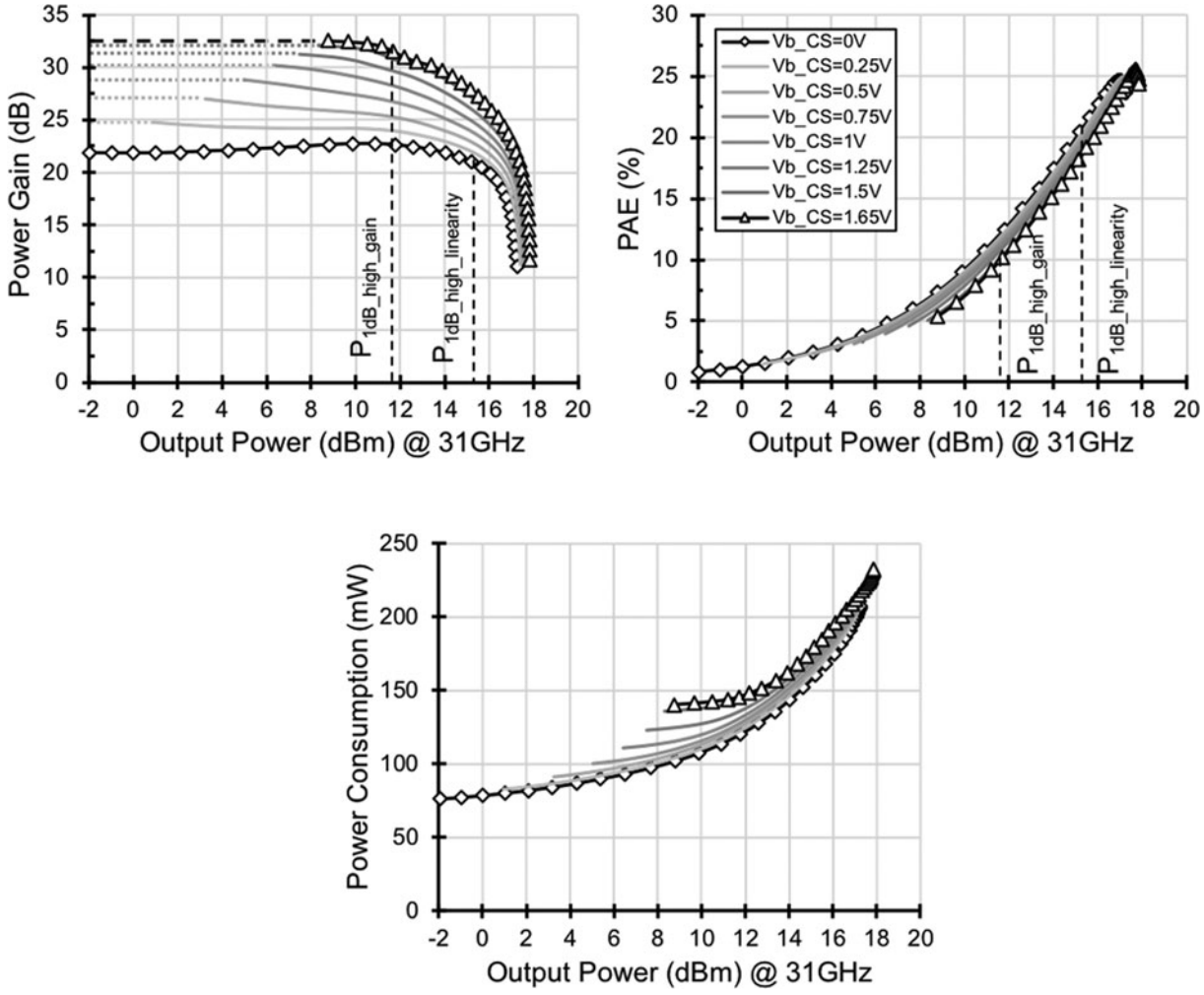

Fig. 17. Large-signal measurements: Gain, PAE and power consumption with body biasing continuous tuning.

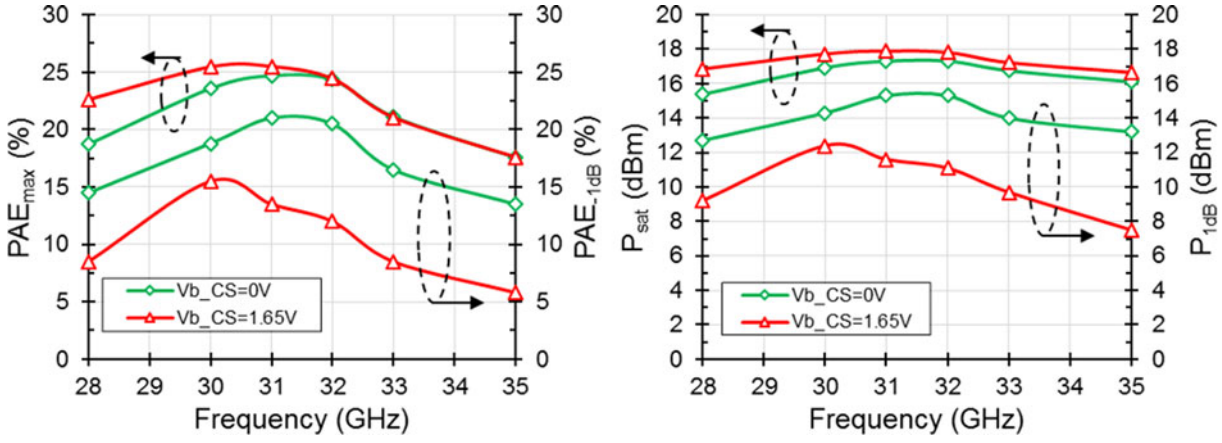

Fig. 18. Large-signal measurements: PAE_{max}/$PAE_{-1\,dB}$ and P_{sat}/$P_{1\,dB}$ in extreme modes from 28 GHz to 35 GHz.

induces the observed higher power consumption. This V_T variation affects both amplification stages and does not have the same impact over performances for all V_{b_CS} values. In fact, for $V_{b\_CS} = 0$ V, the V_T variation induces a higher gain as the operating class drifts from class AB to class A. For $V_{b\_CS} = 1.65$ V, the PA is already in class A. Therefore, the V_T shift operates a drift from class A to over class A, in a mode of operation where the power consumption is higher for reduced gain performances.

Concerning P_{sat} variations, they are linked to the PA routing and thus the same behavior in function of temperature is observed for all V_{b_CS} values. Indeed, the copper resistivity is increased with the temperature. Thus, the drain access resistance (balun parasitic

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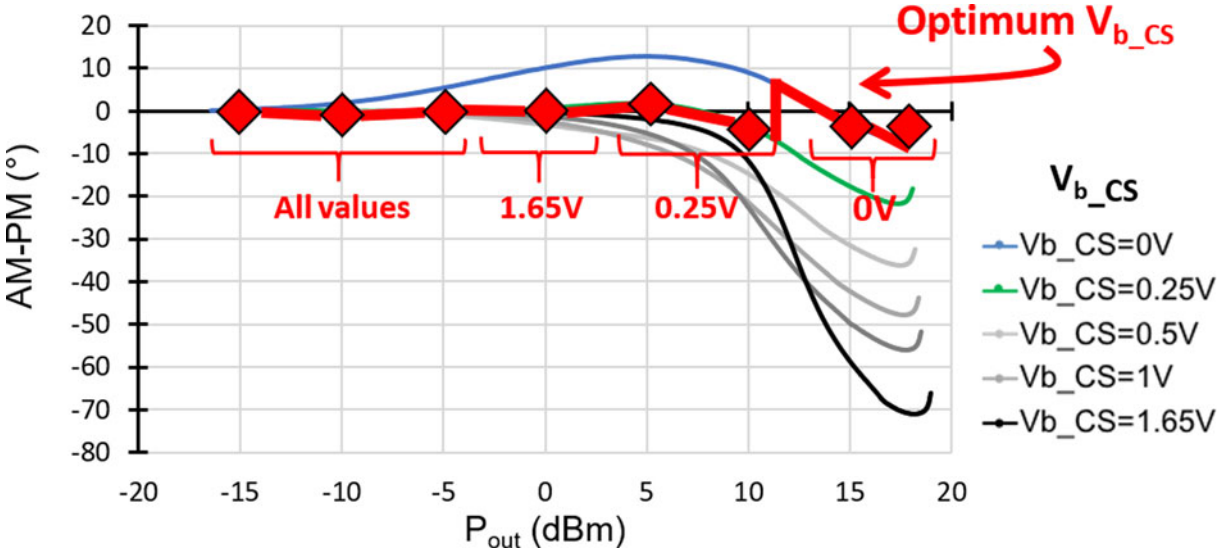
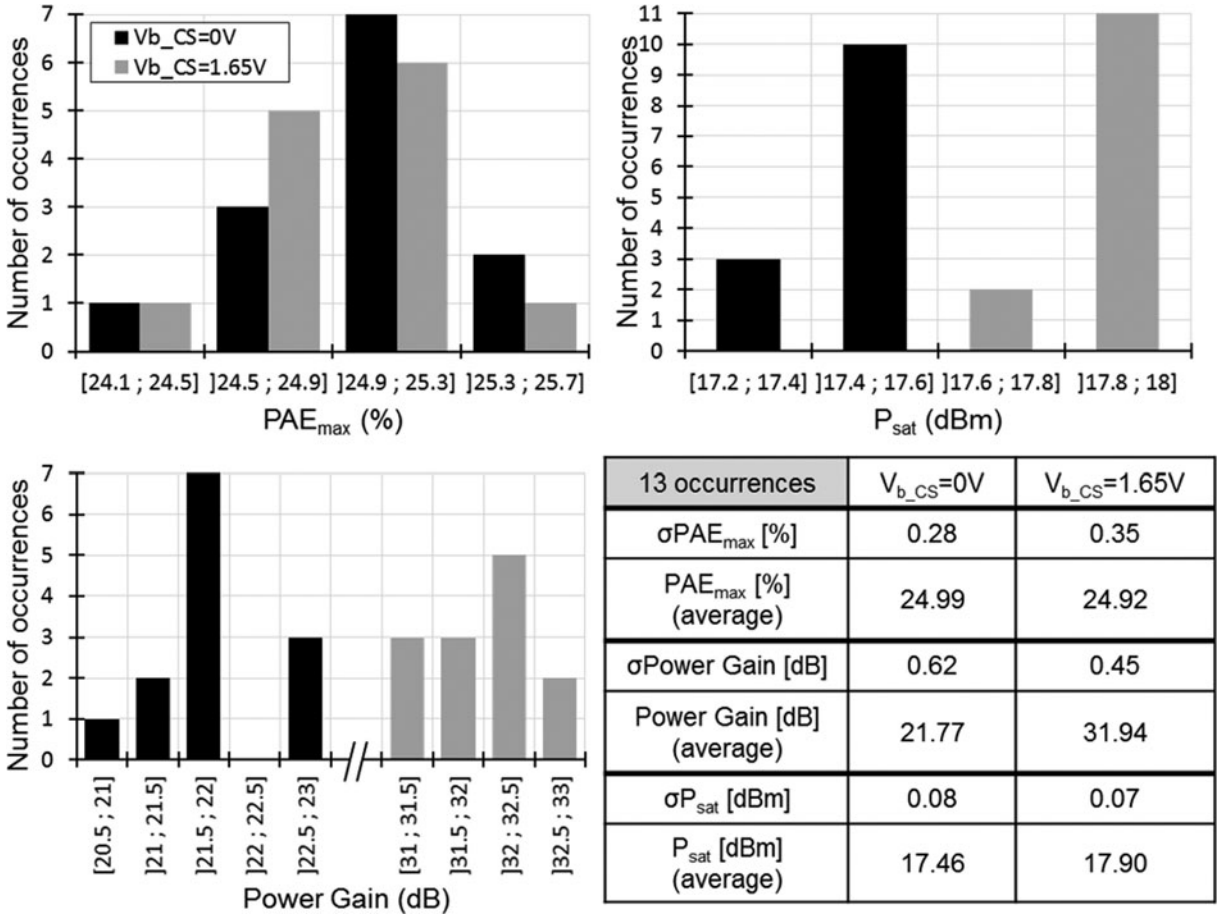


Fig. 19. AM-PM versus P_{out} measurements at 31 GHz with body biasing tuning from 0 V to 1.65 V and optimum V_{b_CS} AM-PM compensation curve.



13 occurrences	V_{b_CS}=0V	V_{b_CS}=1.65V
σPAE_{max} [%]	0.28	0.35
PAE_{max} [%] (average)	24.99	24.92
σPower Gain [dB]	0.62	0.45
Power Gain [dB] (average)	21.77	31.94
σP_{sat} [dBm]	0.08	0.07
P_{sat} [dBm] (average)	17.46	17.90

Fig. 20. Statistical PAE_{max}, power gain and P_{sat} measurements over 13 on-wafer occurrences at 31 GHz with identical bias and supply conditions.

resistance) of the power stage is increased. This reduces the total V_{DS} value of this stage for fixed current conditions. Therefore, the saturated output power is reduced.

For the complete measured temperature range, the temperature-induced degradation remains limited and body-bias variation still performs a large gain tuning range. Therefore, the proposed PA can be operated normally in this temperature range.

These results highlight the circuit and technology robustness to industrial temperature range.

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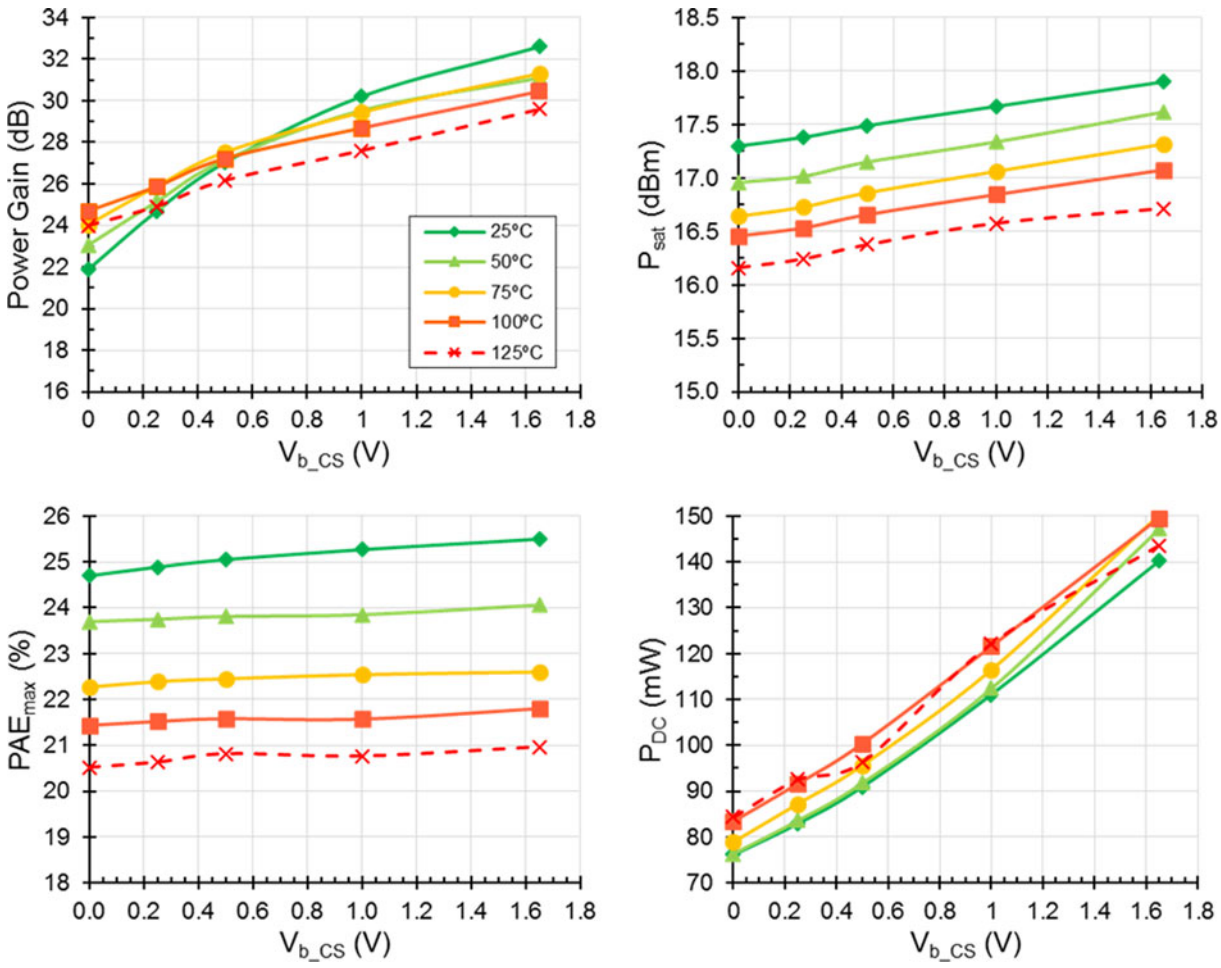

Fig. 21. Large-Signal measurements at 31 GHz from 25°C to 125°C with V_{b_CS} tuning from 0 V to 1.65 V.

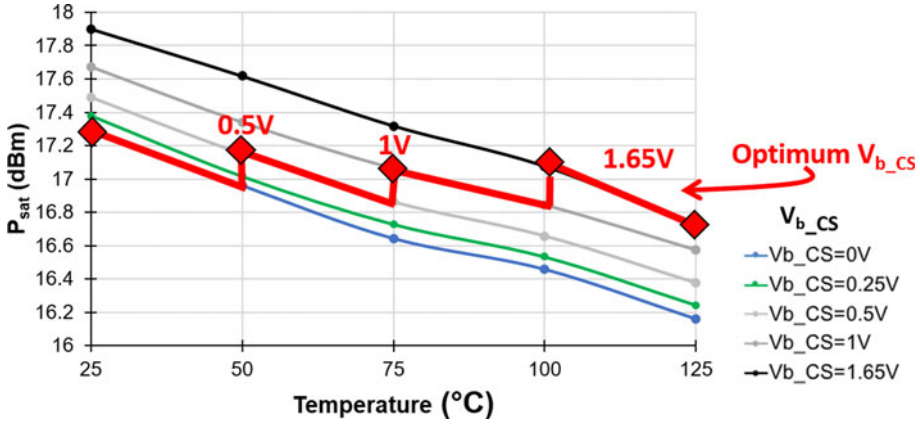

Fig. 22. P_{sat} VS temperature at 31 GHz with optimum V_{b_CS} temperature compensation curve.

It is also possible to take advantage of the body bias induced P_{sat} variation to tackle the effects of temperature. As depicted previously, for all operating modes a P_{sat} variation of around 1 dB is reported when the temperature varies from 25°C to 125°C. By adjusting the body-bias value depending on the temperature of operation, an optimal temperature compensation curve can be obtained as illustrated in Fig. 22. Therefore, P_{sat} variation is reduced to 0.4 dB. It is then possible to use the body-bias as a supplementary lever to overcome thermal-induced performance spread.

Small-signal analysis for several temperature conditions has also been carried out in order to determine the induced impact over S-parameters.

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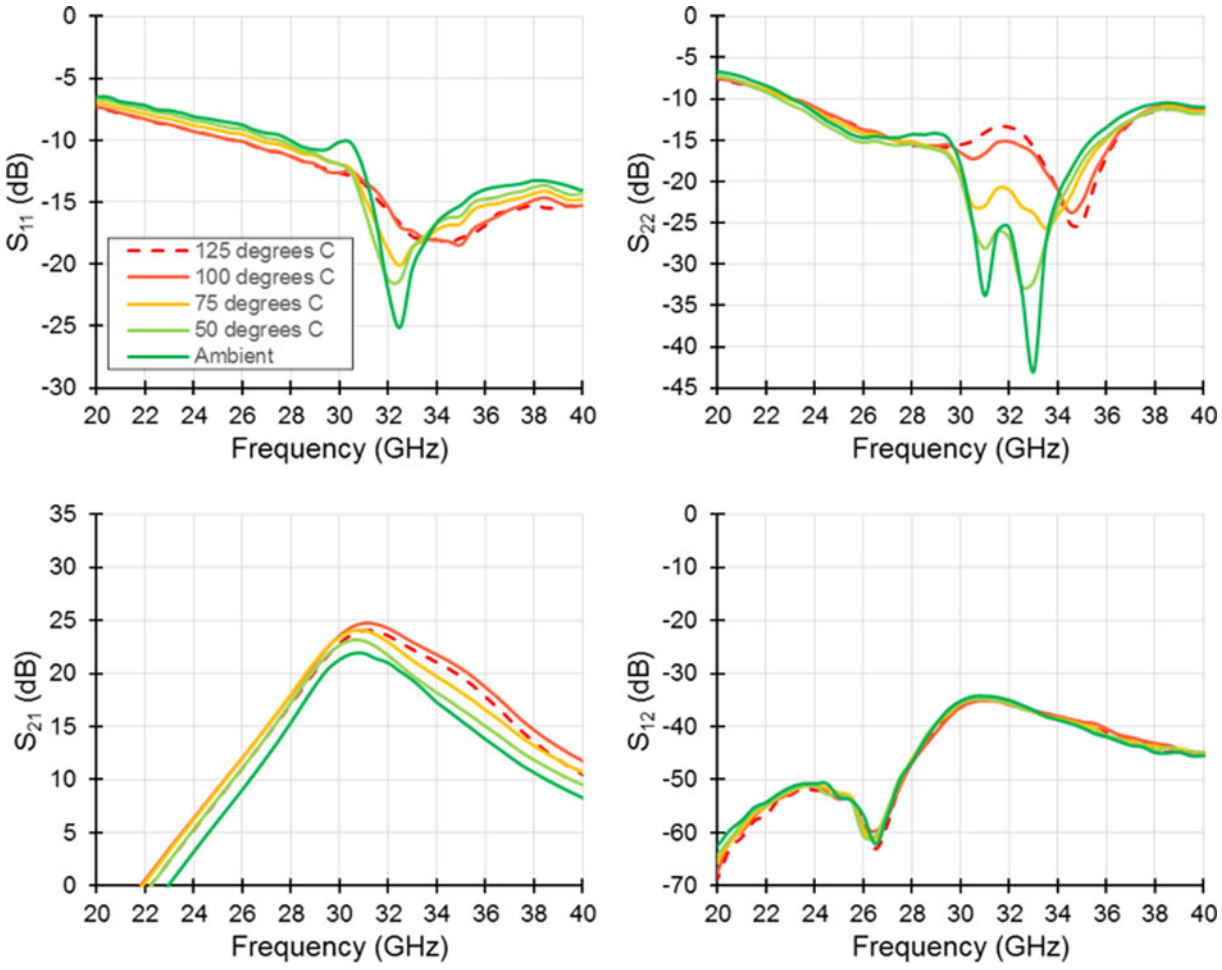

Fig. 23. Small-Signal measurements from 25°C to 125°C in high-linearity mode.

S-parameters curves in high-linearity mode and high-gain mode are exhibited in Figs 23 and 24, respectively. Each curve corresponds to a different temperature value from 25°C to 125°C.

In all temperature conditions, input and output stay well matched over the frequency range of interest in all modes. Both S_{11} and S_{22} temperature behaviors can be compared to S_{11} and S_{22} variations caused by body-bias tuning. It confirms the temperature-induced V_T variation behavior detailed previously in this section.

The S_{21} curves also confirm this behavior. As expected, higher power gain level and slightly improved $BW_{-3\,dB}$ are obtained with higher temperature levels for $V_{b\_CS} = 0$ V while the inverse tendency occurs for $V_{b\_CS} = 1.65$ V. S_{12} curve illustrates that the isolation is not impacted by temperature variations and remains higher than 35 dB under all temperature conditions. This is conferred by the balanced topology that provides a robust high reverse isolation.

State-of-the-art comparison

Table 3 summarizes the PA results in high-linearity and high gain modes and compares the proposed PA with recent mmW PA state-of-the-art.

Highly efficient, low consumption, linear PAs are required to fulfil 5 G applications requirements. As multiple amplification path will be used in FD-MIMO base-stations, the output power will be distributed. High P_{sat} for individual PAs is then not mandatory, while a high gain is expected. The performances achieved by the proposed PA meet these needs. A sufficient P_{sat} around 17.5 dBm is achieved with a limited power consumption of a maximum 140 mW. High gain is achieved even in high-linearity mode, comparable with the highest gain reported in [2]. The high-gain mode shows the highest reported gain around 30 GHz, leading to the highest ITRS FOM in the frequency of interest. Good linearity regarding $P_{1\,dB}$ is achieved in high-linearity mode, with 2 dBm between 1 dB compression point and saturation. Compared to previous design in 28 nm FD-SOI [4], efficiency levels are improved in all operating conditions with no degradation between modes. Balanced topology confers additional robustness to external conditions variations as in [8], also implemented in 28 nm FDSOI technology. Compared to [8], a higher power gain is achieved in our circuit and the power consumption is reduced. Efficiency levels at a peak, at 6 dB P_{sat} back off and at $P_{1\,dB}$ are improved.

In the state of the art, PAs achieving high output power levels present a limited gain and suffer from high power consumption even if efficiency levels are good [3]. High PAE PAs generally suffer from low P_{sat}, linked with low power consumption [2]. A trade-off generally exists between reported performances for the different targeted applications. This trade-off is relaxed in the

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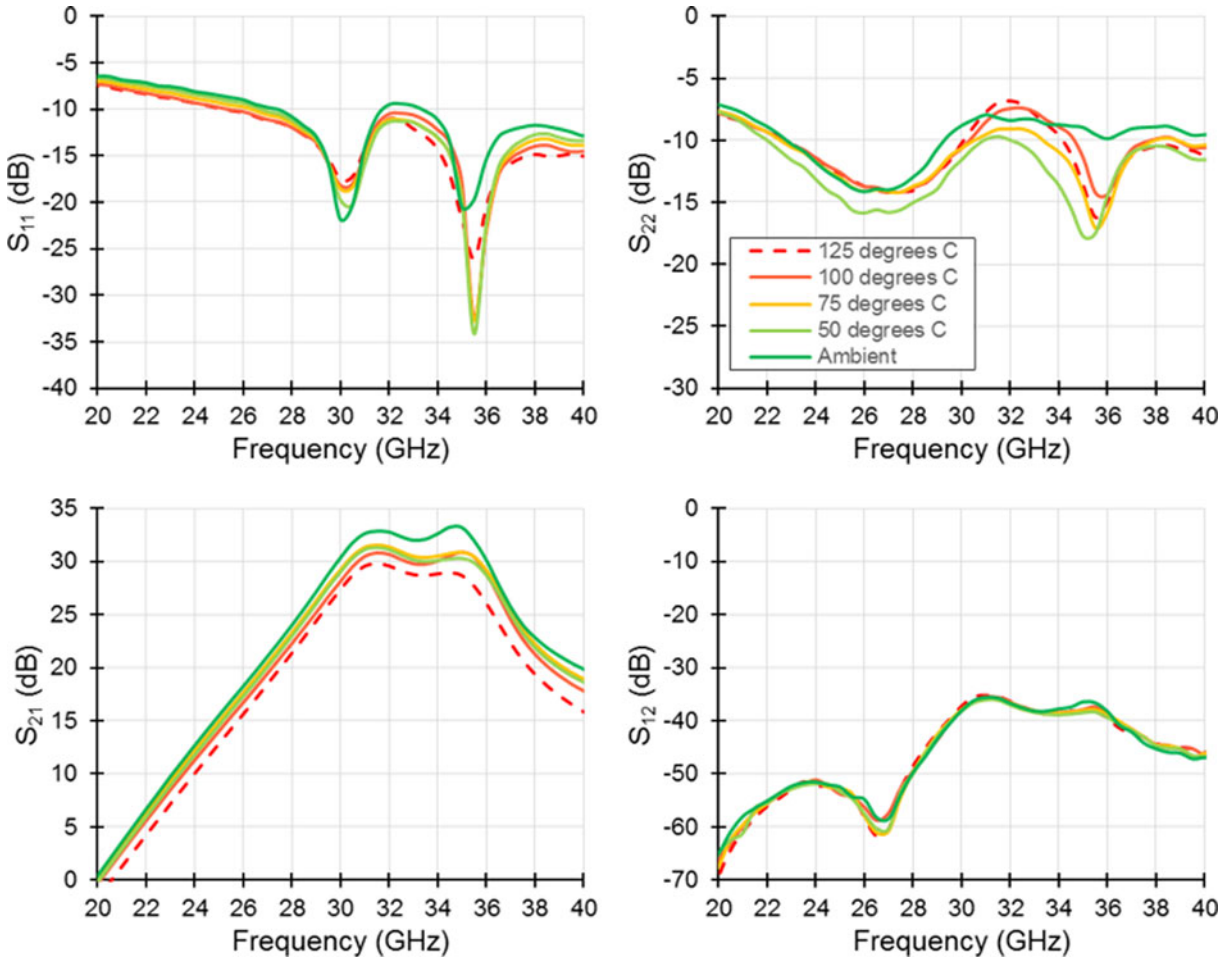

Fig. 24. Small-Signal measurements from 25°C to 125°C in high-gain mode.

Table 3. Comparison with mm-Wave silicon PA state-of-the-art

	This work						
	High-Lin.	High-Gain	[1]	[2]	[3]		[8]
Technology	28 nm FD-SOI CMOS		130 nm SiGe	40 nm CMOS	45 nm SOI CMOS		28 nm FD-SOI CMOS
Supply [V]	0.7#/1.98†	0.7#/1.98†	1.5	1.1	5.2	5.2	2
Frequency [GHz]	31	31	28	27	29	29	28
Power Gain[dB]	21.9	32.6	18.2	22.4	14[a]	13	17.5
P_{sat}[dBm]	17.3	17.9	16.8	15.1	23.7	24.8	18.4
P_{1dB}[dBm]	15.3	11.6	15.2	13.7	20	21	15.4
PAE_{max}[%]	24.7	25.5	20.3	33.7	29	26	12.4
PAE_{-1dB}[%]	21	10	19.5	27.5[a]	18[a]	17.5[a]	9.5[a]
PAE_{6dB} P_{sat} Backoff[%]	11.5	10.4	14[a]	15[a]	11[a]	15[a]	6[a]
P_{DC}[mW]	76.1	140.2	71[a]	30.3	448[a]	475[a]	154
Active Area [mm^2]	0.508		1.76[b]	0.23	0.24		0.66
ITRS FOM	1932	26925	503	1381	1436	1317	405

Supply: #1st stage (SI), †2nd stage (S2)
ITRS FOM [W.GHz^2] = P_{sat} (W).Gain (lin).Freq^2 (GHz$^{2)}$.PAE_{max}.
[a]Estimated from figures.
[b]Pads included.

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proposed PA as good efficiency and output power are reported, simultaneously with limited power consumption and a high gain.

Conclusion

In this article, a 5 G PA is presented, aiming for the 31.8–33.4 GHz frequency band. A very wide and fine grain gain dynamic over 10 dB is obtained thanks to body biasing flexibility. The specific output load optimization done as a compromise covering both Class A and Class AB enables quasi-constant PAE_{max} and P_{sat} under all operating modes. Robustness to both process-induced spread and industrial temperature range has been demonstrated thanks to design choices and optimizations. Temperature-induced P_{sat} degradation compensation, as well as AM-PM optimization regarding output power back-off, are enabled by extensive usage of body biasing. Compared to previous work in the same technology, PAE at 6 dB P_{sat} back-off has been significantly improved. Finally, the extreme gain of 32.6 dB achieved with only two stages in high-gain mode demonstrates an ITRS FOM of 26 925, the best in class reported around the frequency band of interest, to our best knowledge.

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