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RESEARCH PAPER

Design and model studies for solid-state power amplification at 210 GHz

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The high millimeter-wave (mmW) frequency range offers new possibilities for high-resolution imaging and sensing as well as for high data rate wireless communication systems. The use of power amplifiers of such systems boosts the performance in terms of operating range and/or data rate. To date, however, the design of solid-state power amplifiers at frequencies about 210 GHz suffers from limited transistor model accuracy, resulting in significant deviation of simulation and measurement. This causes cost and time consuming re-design iterations, and it obstructs the possibility of design optimization ultimately leading to moderate results. For verification of the small-signal behavior of our in-house large-signal transistor model, S-parameter measurements were taken from DC to 220 GHz on pre-matched transistors. The large-signal behavior of the transistor models was verified by power measurements at 210 GHz. After model modification, based on process control monitor (PCM) measurement data, the large-signal model was found to match the measurements well. A transistor model was designed containing the statistical information of the PCM data. This allows for non-linear spread analysis and reliable load-pull simulations for obtaining the highest available circuit performance. An experimental determination of the most suitable transistor geometry (i.e. number of gate fingers and gate width) and transistor bias was taken on 100 nm gate length metamorphic high electron mobility transistor (mHEMT) transistors. The most suitable combination of number of fingers, gate width and bias for obtaining maximum gain, maximum output power, and maximum power added efficiency (PAE) at a given frequency was determined.

Keywords: modelling, simulation, characterizations of devices, circuits power amplifiers, linearizers

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I. INTRODUCTION

Low-noise amplifiers (LNAs) are a field of research in the millimeter-wave (mmW) frequency range for many years and outstanding results have been reported [1, 2]. As in an LNA, where the input is matched to obtain simultaneous power and noise match, a power amplifier (PA) has an output matching that allows for maximum output power and/or maximum efficiency. This is done by optimizing the current/voltage swing at the output of the device. The most suitable means is a load-pull analysis. The major difference of a LNA and a PA is not only the matching, but also the input and output signal amplitude. Within a PA signals of large amplitudes are amplified and hereby experience some non-linear behavior like compression.

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At the atmospheric window around 210 GHz, free-space signals suffer from little attenuation and therefore systems with large absolute bandwidth can be realized. Bandwidth is the key to applications such as high-resolution imaging and high data-rate wireless communication. Moreover, systems in the mmW frequency range offer the capability of sufficient transmission through all adverse conditions, such as fog and rain. Additionally, fabric, paper, and plastic are also transparent. This allows for applications such as imaging radar for detection of concealed weapons and high data-rate wireless communication systems, which are non-sensitive to weather conditions.

Applications in the high mmW frequency range are highly dependent of the PA performance. The key element is transmit power since the working range is highly dependent on it. To avoid signal distortion, intermodulation and harmonic distortion, the most important property of amplifiers, suitable for communication, is linearity. Since cooling and power consumption are critical points where amplifiers are concerned, efficiency is also an important design criterion. This is why more and more publications focus on the design of (PAs) in the high mmW frequency range [3, 4].

Only the high electron mobility transistor (HEMT) based on InGaAs/InAlAs heterostructures is capable of delivering both output power and gain at frequencies about 210 GHz. These heterostructures can be grown either directly on InP

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wafers or by using a metamorphic buffer to adapt the lattice constant on GaAs substrates. Since GaAs wafers offer high crystal quality at low cost and are robust compared to InP wafers, the metamorphic approach is advantageous. The drawback of the metamorphic HEMT (mHEMT) is the lower thermal conductivity of the metamorphic buffer and the additional growth effort.

Often, in publications a deviation between the simulated results and the measurements of the devices can be seen. This deviation becomes even more pronounced when working in the high mmW frequency range. For state-of-the-art results and less design iterations, there is a need for accurate CAD models. Only with accurate models reliable load-pull simulations can be done, and the output power can be optimized in addition to the optimization of maximum gain. Despite this knowledge and need, there are only few publications available dealing with model verification [5].

In the following, this verification is done for the in-house large-signal mHEMT transistor models developed at the Fraunhofer IAF. Starting with a small-signal verification, power measurements are taken on pre-matched transistors at 210 GHz to verify the model's large-signal accuracy.

Furthermore, the most suitable transistor geometry and bias for various PA applications at frequencies about 210 GHz are determined experimentally. The results presented in that chapter are based on the work published in [6].

II. TECHNOLOGY

The research and development of the mHEMT is ongoing and different mHEMT technologies exploiting different gate length have been developed at the Fraunhofer IAF. For the sake of clarity, in this work only the 100 nm gate-length transistor technology is investigated. The 100 nm gate-length transistors are grown via molecular beam epitaxy on 4-inch semi-insulating GaAs wafers. To adapt the lattice constant, a metamorphic buffer is grown in a linear $In_yAl_{0.48}Ga_{0.52-y}As$ transition in composition. The transistor mesa is wet-etched, and GeAu is deposited for ohmic contacts. The T-shaped Pt–Ti–Pt–Au gate, which is defined by e-beam lithography, is the key element of the mHEMT devices. Finally a passivation with 250 nm, chemical vapor deposited (CVD), silicon nitride for good reliability and robustness is done. The 100 nm gate-length technology makes use of an $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ composite channel to increase the breakdown voltage, which is very important for power amplification. This results in an f_T of more than 200 GHz and a very high transconductance of $g_{m,max} = 1300$ mS/mm. A detailed description of the IAF mHEMT technologies can be found in [6, 7]. The electrical DC and RF parameters of the 100 nm gate-length transistor technology are summarized in Table 1.

Due to the high isolation between adjacent lines, the low source inductance of the active devices, the very compact transmission line dimensions, and the suppression of parasitic substrate modes, all passive structures are realized in grounded coplanar wave-guide technology, making use of a full backside wafer process, including wafer-thinning down to 50 μm thickness and substrate through vias. The coplanar transmission lines are built by an electron beam evaporated Au-based interconnection layer, and a 2.7 μm thick plated Au layer in air-bridge technology.

Table 1. Electrical DC and RF parameters of the 100 nm gate-length IAF mHEMT technology.

Parameter	Symbol (unit)	Value
Gate-length	l_g (nm)	100
Source resistivity	R_s (Ωmm)	0.23
Maximum drain current	$I_{DS,max}$ (mA/mm)	900
On-state breakdown	V_{BDS} (V)	3.0
Max. transconductance	$g_{m,max}$ (mS/mm)	1300
Current gain cut-off freq.	f_t (GHz)	220
Max. freq. of oscillation	f_{max} (GHz)	300

III. PRE-MATCHED TRANSISTORS

Stand-alone transistors have poor matching at 210 GHz, and low gain can be obtained. Therefore, transistors with additional input and output matching networks have to be investigated. The matching makes use of transmission lines of different lengths and characteristic impedances, connected in series.

All pre-matched transistor circuits are in a 50 μm ground-to-ground environment. The chip-layout of a 2 × 30 pre-matched transistor is depicted in Fig. 1. The pre-matched devices have a conjugate-complex matching to obtain maximum gain and no load-line matching for maximum output power. Thus, the measured output power is not necessarily the maximum output power, but the maximum output power with conjugate-complex matching.

In the following a pre-matched transistor is called e.g. 210 GHz pre-matched transistor, when it is matched for a frequency of 210 GHz.

All transistors have a good output matching and an acceptable input matching at their matching frequency (better than −10 dB). This allows for a comparison of different measurements without any correction of the measurement results due to power mismatch. Nevertheless, the exact quantitative measurement results depend on many factors, such as system calibration and set-up. Within this work, comprehensive measurements on a complete set of transistors are performed, which allow for an exact qualitative comparison of transistor devices. All pre-matched transistors have varying matching networks and therefore varying losses in access lines i.e. the matching networks. The overall losses of the matching networks are listed in Table 2. The non-perfect matching and the varying losses have to be kept in mind when comparing the measurements. It has to be pointed out, however, that matching for maximum output power will affect the evaluation.

Due to effects, like finite processing tolerances, aging of the machinery and other changes, such as changes in photo-resist

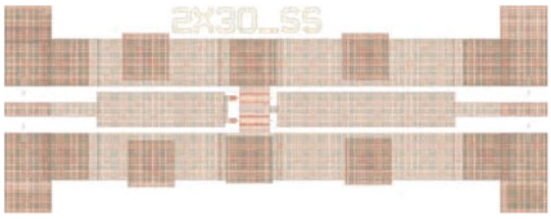

Fig. 1. Layout of a 2 × 30 pre-matched transistor in coplanar environment with 50 μm ground-to-ground spacing.

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Table 2. S-parameter and power measurements are taken at the listed pre-matched device geometries and frequencies.

Gate length	Frequency (GHz)	Transistor geometry	Losses
100	195	2 × 15, 2 × 30, 2 × 45	0.7 dB
	200	2 × 10, 4 × 15, 4 × 20, 4 × 30	
	205	4 × 10	

composition and properties, there is always a variation of transistor performance within a wafer run. The variation is even more pronounced when transistors of different wafer runs are compared. That is why all investigated transistors are located on the same wafer and are chosen carefully.

A DC analysis of many transistor samples is carried out and only the devices with a characteristics, which is typical for the chosen wafer are investigated further. The selection criteria are for example pinch-off drain current ($I_{DS,min}$), maximum transconductance ($g_{m,max}$), and maximum drain current ($I_{DS,max}$). For every transistor geometry only one device is considered for further investigation.

IV. POWER MEASUREMENT CONFIGURATION

Power measurements are performed on the 210 GHz pre-matched transistors, listed in Table 2. The term power measurements here stands for a scalar power measurement, as depicted in Fig. 2. A W-band (75–110 GHz) source module generates a signal, which is amplified by two in-house W-band PAs and then doubled by a commercially available frequency multiplier. The output power is measured on-wafer with all power levels normalized to the probe–tip plane. The power meter is commercially available and Schottky barrier diode based. With this measurement set-up it is possible to drive the transistors far beyond the −1 dB compression point but not in saturation. The measurement configuration has the following properties:

- Power level accuracy: ± 0.25 dB.
- Frequency range: 195–220 GHz by steps of 5 GHz.
- Power at DUT input (P_{in}): −18 to 4 dBm.

V. TRANSISTOR MODEL VERIFICATION

A) Model Description

The behavior of the large-signal transistor models, developed at the Fraunhofer IAF and described in [8], is investigated and the model accuracy is verified. This is necessary for various reasons. First, the transistor models are created upon measured DC and S-parameter data up to 110 GHz. This means that, when a design is done at frequencies higher than 110 GHz, an extrapolation of parameters is trusted. To verify this extrapolation, transistors at much higher frequencies are investigated by doing S-parameter measurements. Second, it is necessary to check whether the models are able to predict the non-linear behavior correctly. This is not self-evident, since the large-signal models are created by using a set of DC and small-signal measurements, i.e. S-parameter measurements. To test whether the large-signal models are able to perform properly, power measurements as described in Section IV are performed.

Most models are built in a way that the intrinsic transistor and its surrounding parasitic shell are separated (cf. Fig. 3). The extrinsic parasitics are assumed to be linear series and shunt resistances and reactances. The properties and values of the parasitic shell depend on whether the transistor is in two- or four-finger geometry and on whether it is in common-source or common-gate configuration, for example. The intrinsic transistor is based on a semi-empirical modeling approach for transistors, making use of the state-space approach, which is usually used for modeling dynamic systems [8]. In this approach, slow and fast memory effects are described by first-order linear differential equations for internal state variables with state functions that depend on the terminal voltages in a non-linear manner. The model includes state functions for the currents, an energy function for the gate charges, and fast delays for gate charging and carrier transit. The electrostatic energy function warrants reciprocity of the capacitance matrix and charge conservation. The presence of thermal self-heating as well as slow drain-lag dispersion effects were evident, and were taken into account in the model by introduction of the channel temperature, and a lag voltage as internal system variables. Virtual drain–source symmetry was taken into account in the model by choice of state functions with appropriate symmetry properties, and resulted in a proper description of the data, in particular, in the range of negative drain voltage.

To separate the intrinsic transistor and the parasitic shell, S-parameters for a single operating point and various transistor geometries are measured and a parameter fit, using a

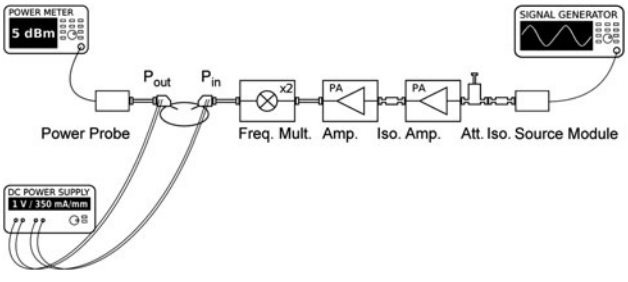

Fig. 2. Set-up for the G-band (140–220 GHz) power measurement.

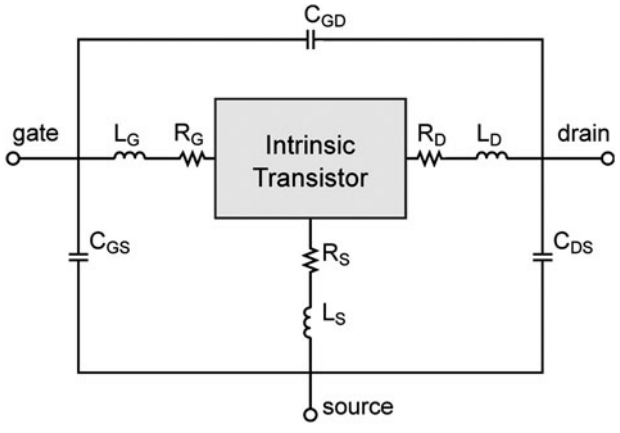

Fig. 3. Simplified equivalent circuit of a mHEMT. A parasitic shell embeds the intrinsic transistor, which is based on state-space equations, not on equivalent circuit elements.

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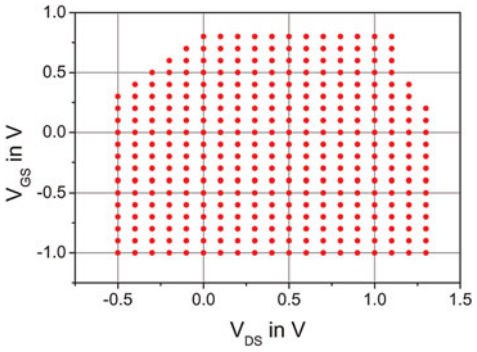

Fig. 4. Each dot marks a S-parameter measurement at the indicated voltage bias, carried out for transistor model extraction.

single-step linear regression algorithm to match the measurements, is carried out. This is sufficient to separate the parasitic shell from the intrinsic transistor and thereby create a parasitic shell model, which is scalable over the number of transistor fingers and the gate width. The intrinsic transistor is determined by doing a parameter fit to match a set of S-parameter measurements. The measurements are done for many DC bias points lying in the IV bias plane as depicted in Fig. 4. The extraction of the intrinsic transistor is done for one transistor geometry using the scalable parasitic shell. The intrinsic model uses a simple linear scaling rule to scale the intrinsic parameters.

B) Small-signal verification

The first step in large-signal transistor model verification is to perform on-wafer S-parameter measurements of the pre-matched transistors via a vector network analyser. This is done from DC up to 220 GHz on three measurement systems. In the following their properties and their range of operation is listed:

- Coaxial from 0.25 to 110 GHz.
- WR-7 wave-guide from 110 to 170 GHz.
- WR-5 wave-guide from 140 to 220 GHz.

All S-parameter measurements are performed at a bias were the transistor delivers maximum gain. The measurements are performed by doing drain–source voltage (V_{DS}) and drain–source current (I_{DS}) bias. The values for V_{DS} and I_{DS} are determined by PCM measurement data.

The small-signal accuracy of the large-signal transistor model is verified for all transistor geometries listed in Table 2. Figure 5 stands for the whole small-signal verification cycle and show the measurement and simulation results of a mHEMT with a gate length of 100 nm. It is a two-finger device with a gate width of 30 μm each (2 × 30). It is matched to a frequency of 195 GHz. The simulated and the measured data show good matching from DC to 220 GHz, considering the limited measurement accuracy in the high mmW frequency range. Moreover, the transistor model modification as supposed in the following section has no influence on the model's small-signal behavior.

C) Large-signal verification

After having verified that the large-signal transistor model accurately predicts the small-signal behavior, its non-linear behavior has to be investigated. In order to do so, power measurements are taken on the 210 GHz pre-matched transistors listed in Table 2.

Again, the large-signal accuracy of the transistor model is verified for all transistor geometries but only the verification for a 2 × 30 pre-matched transistor is shown. Figure 6

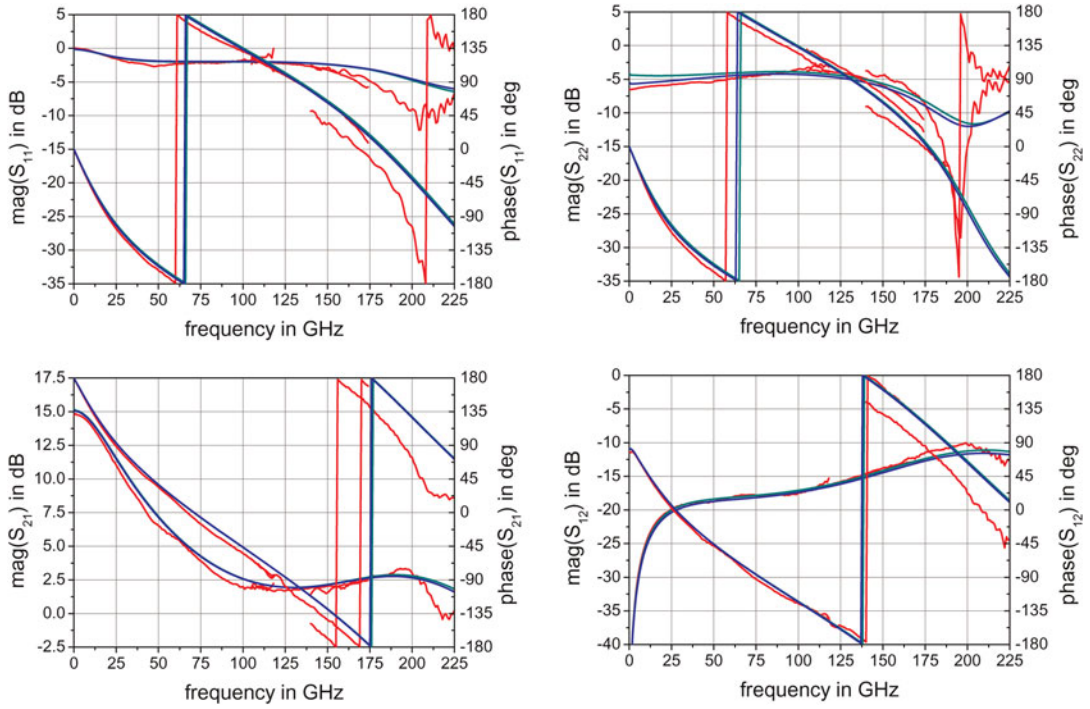

Fig. 5. S-parameter measurements of a 100 2 × 30 pre-matched transistor. red line: measurements taken on three measurement stations. green/blue: original/modified large-signal model.

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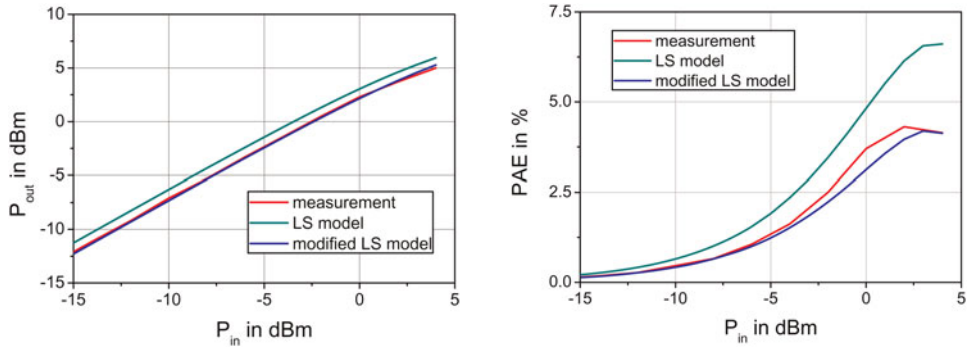

Fig. 6. Power measurements of a 100 2 × 30 transistor at 195 GHz ($V_{DS} = 1$ V and I_{DS} is set for maximum gain).

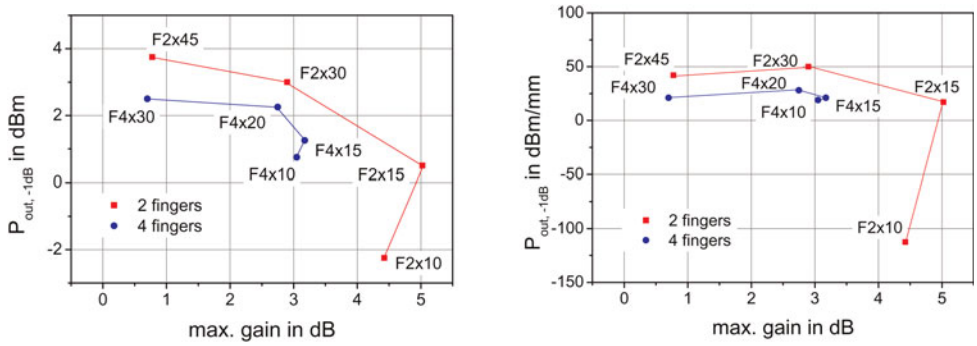

Fig. 7. Regular and normalized −1 dB compression output power versus maximum gain for varying transistor geometries ($V_{DS} = 1$ V, $I_{DS} = 350$ mA/mm).

makes clear that the simulation of the large-signal model is in good accordance with the corresponding measurement, where output power and PAE are concerned. The parameters experience a shift along the axis of ordinate, only.

As previously mentioned, there is always a small variation in transistor parameters within a wafer run and a larger variation between the runs. These changes in transistor parameters have a direct impact on the large-signal transistor behavior. Therefore it is evident that a deviation between measurement and simulation is found, keeping in mind that a large-signal transistor is generated by using measurements of one transistor from any arbitrary run as basis.

To diminish the deviation between measurement and simulation, an update of the large-signal model is made. During this update transistor parameters such as $I_{DS,max}$, $g_{m,max}$ and threshold voltage (V_{th}) are changed to the values of a chosen run. The values are obtained from PCM measurement data. These data are based on measurements to characterize the single wafer runs, i.e. no additional measurement efforts are necessary. After the update the transistor model represents a virtual mean transistor from the chosen run. This allows for minimization of the deviation of power measurement and simulation as shown in Fig. 6.

The parameter spread, which can be observed within a wafer run and between different wafer runs, can be assumed to be Gaussian distributed. The mean value and standard deviation of parameters such as parasitic capacitance and resistance, $I_{DS,max}$, $g_{m,max}$, and V_{th} can be determined by analyzing the PCM measurement data. The parameter spread, easily can be implemented in our in-house large-signal transistor model, i.e. it is possible to create a transistor model that represents the average transistor and the standard deviation for some important transistor parameters. This enables the designer to do a Monte Carlo and a yield analysis and therefore to check how likely the simulated result is. Moreover, reliable load-pull simulations for obtaining the highest available output power become possible, as well as optimization of the design to be less vulnerable to process variation.

VI. EXPERIMENTAL DETERMINATION OF THE MOST SUITABLE TRANSISTOR

To determine the most suitable transistor geometry, the 100 nm gate-length transistors are measured at their matching frequency. They are biased to achieve maximum gain. Figure 7 shows that the −1 dB compression point output

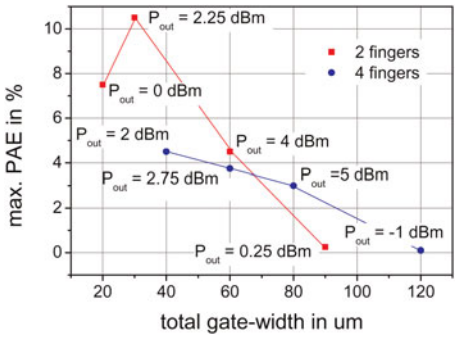

Fig. 8. Maximum PAE versus total gate width with achievable output power at the point of maximum added efficiency ($l_g = 100$ nm; bias: $V_{DS} = 1$ V, $I_{DS} = 350$ mA/mm).

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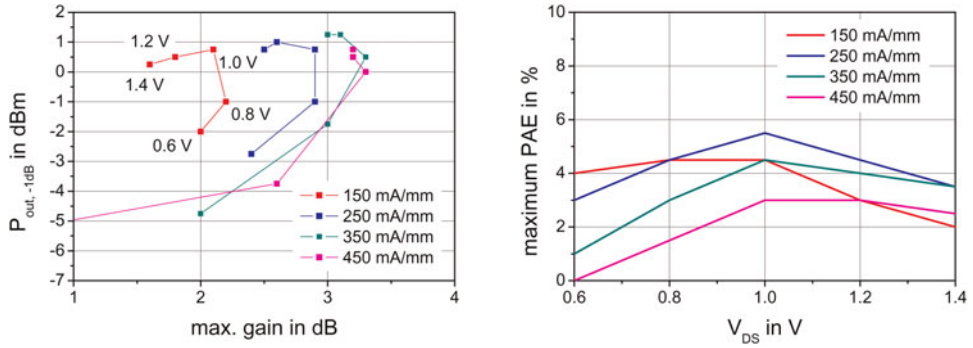

Fig. 9. −1 dB compression output power versus maximum gain and PAE versus drain voltage for varying drain current densities (l_g = 100 mm; gate width = 4 × 10 um).

power ($P_{out,-1\ dB}$) steadily rises with increasing total gate width. The increase is not unlimited but goes into saturation and the output power density even decreases (Fig. 7). Therefore, it is not sensible to use transistors with large total gate widths in the hope of reaching a high linear output power. Two finger devices deliver more output power at the −1 dB compression point than four-finger devices. The maximum achievable gain increases first, then has a maximum and decreases with the total gate width. At large total gate widths four-finger devices deliver more gain than two-finger devices of a comparable gate width. Whereas at small total gate widths two-finger devices deliver more gain than comparable four-finger devices. Figure 8 shows the maximum achievable PAE versus the total gate width i.e. number of fingers multiplied by the gate width. Additionally, the output power at maximum PAE is shown. The PAE constantly decreases with increasing total gate width. Moreover, a 2 × 30 and a 4 × 15 device, which have the same total gate width, almost have the same characteristics where PAE is concerned. But, as shown above, the 2 × 30 device delivers a higher output power than the 4 × 15 device. Please note that in Fig. 7 the linear power is plotted. Figure 6 clearly indicates that the saturated output power is much higher.

Measurements at different quiescent points are taken on a 100 nm 4 × 10 transistor to determine which bias provides the highest $P_{out,-1\ dB}$, gain and PAE. The measurements are taken at a frequency of 205 GHz. A bias of $V_{DS} = 1$ V and $I_{DS} = 350$ mA/mm is determined by PCM measurement data to be the bias of maximum gain. Measurements are taken in a range around this point to study the transistor properties. $P_{out,-1\ dB}$ is plotted versus the maximum achievable gain for varying bias in Fig. 9. First, it increases with V_{DS}, peaks, then decreases for every given drain current. A saturation effect can be observed, i.e. the maximum $P_{out,-1\ dB}$ is almost independent of the applied drain current. The maximum gain increases with V_{DS}, has a maximum and then starts to decrease, too. The position of the maximum shifts to high V_{DS} with increasing drain current. The magnitude of the maximum also increases with drain current. The point of maximum gain, determined through PCM data, equals the point determined through power measurements. It can be stated that small-signal amplification is possible down to $V_{DS} = 0.8$ V. At lower V_{DS}, the gain decreases significantly. Furthermore, it can be stated that a V_{DS} of at least 1 V is needed for a power application. Figure 9 shows that first the PAE rises with increasing V_{DS}, reaches a maximum at $V_{DS} = 1$ V and starts to decrease then. The best PAE can be obtained with $I_{DS} = 250$ mA/mm, which is equivalent to a class AB operating point.

VII. CONCLUSION

The large-signal transistor model, developed at the Fraunhofer IAF and used for PA design in the mmW wave frequency range, has been investigated with the help of pre-matched transistors. Its small-signal accuracy has been proven by S-parameter measurements from DC to 220 GHz. Its large-signal accuracy was verified by power measurements at 210 GHz. After readjustment of the model to the run specific parameters, based on PCM measurement data, the large-signal model was found to match the power measurements well. The transistor model was extended to include the statistical parameter spread obtained from run-specific PCM data. This allows for non-linear spread analysis and reliable load-pull simulations to obtain the highest available output power.

Moreover, an experimental determination of the most suitable transistor geometry and transistor bias for power amplification at 210 GHz was undertaken. Two-finger devices were found to offer more output power than four-finger devices of a comparable gate width. Whereas four-finger devices with large total gate widths offer more gain than two-finger devices of a comparable gate width. Furthermore, the most suitable bias for maximum gain, maximum output power, and maximum PAE was determined.

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REFERENCES

[1] Deal, W.; et al.: Demonstration of a S-MMIC LNA with 16-dB Gain at 340-GHz, in IEEE Compound Semiconductor Integrated Circuit Symp., October 2007, 1–4.

https://doi.org/10.1017/S1759078711000432 Published online by Cambridge University Press

[2] Tessmann, A.; Leuther, A.; Massler, H.; Bronner, W.; Schlechtweg, M.; and Weimann, G.: Metamorphic H-Band Low-Noise Amplifier MMICs, in IEEE/MTT-S Int. Microwave Symp., June 2007, 353–356.

[3] Radisic, V.; et al.: A 50 mW 220 GHz power amplifier module, in Microwave Symp. Digest (MTT), 2010 IEEE MTT-S Int., May 2010.

[4] Kallfass, I.; et al.: A 200 GHz monolithic integrated power amplifier in metamorphic HEMT technology, IEEE Microw. Wirel. Compon. Lett., **19** (6) (2009), 410–412.

[5] Martin, G. H.: On-wafer large-signal model verification, In 38th ARFTG Conf. Digest-Winter, vol. 20, December 1991, 5–14.

[6] Leuther, A.; et al.: 50 nm MHEMT technology for G- and H-band MMICs, in IEEE 19th Int. Conf. on Indium Phosphide and Related Materials, May 2007, 24–27.

[7] Tessmann, A.; Kallfass, I.; Leuther, A.; Massler, H.; Schlechtweg, M.; and Ambacher, O.: Metamorphic MMICs for operation beyond 200 GHz, in European Microwave Integrated Circuit Conf., October 2008, 210–213.

[8] Seelmann-Eggebert, M.; Merkle, T.; van Raay, F., Quay, R.; and Schlechtweg, M.: A systematic state-space approach to large-signal transistor modeling, IEEE Trans. Microw. Theory Tech., **55**(2) (2007), 195–206.

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