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Millimeter-wave dual-mode and dual-band switchable Gilbert up-conversion mixer in 65-nm CMOS process

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Abstract

In this paper, a millimeter-wave (MMW) dual-mode and dual-band switchable Gilbert up-conversion mixer in a commercial 65-nm complementary metal oxide semiconductor (CMOS) process is presented. By simply changing the bias, the proposed CMOS Gilbert up-conversion mixer can be switched between subharmonic and fundamental operation modes for MMW dual-band applications. With a low local oscillator pumping power of 3 dBm and low dc power consumption of 6 mW, the proposed CMOS Gilbert up-conversion mixer exhibits a measured conversion gain of -0.5 ± 1.5 dB from 37 to 50 GHz and 2.5 ± 1.5 dB from 17.5 to 32 GHz for the subharmonic and fundamental modes, respectively.

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Introduction

The current trend for millimeter-wave (MMW) wireless communication systems is toward high integration and high flexibility, which has led to an interest in developing multi-band and multi-standard transceivers. Traditional design strategies have adopted separate single-band radio-frequency (RF) front-ends in parallel for multi-band and multi-standard operations, which increase the power consumption and chip size. To alleviate this problem, the RF building blocks which can be shared among multiple frequency bands are highly required [1–3].

There have been several demonstrations of dual-band mixers. For instance, a 4/8 GHz dual-band up-conversion mixer was proposed by using two mixer cores followed by a combiner [4]. A 2.4/5.7 GHz dual-band Gilbert up-conversion mixer and a 2.45/5.2 GHz dual-band Gilbert down-conversion mixer using dual-band *LC* matching networks were proposed in [5] and [6], respectively. By reconfiguring the output waveform of the local oscillator (LO), dual-band mixing can also be achieved [7, 8]. All these mixers, however, were demonstrated below 12 GHz. Recently, an MMW dual-band switchable star mixer and an MMW fundamental and subharmonic hybrid ring mixer have been proposed in [9,10], respectively. However, the passive mixers suffer from high conversion loss and require high LO pumping power, especially in complementary metal oxide semiconductor (CMOS) technologies. An MMW dual-band CMOS down-conversion mixer with a modified Gilbert topology was demonstrated in [11], but the balun-based input stage is not suitable for an up-conversion mixer and the conversion gain is still unsatisfactory.

In this paper, an MMW dual-mode and dual-band switchable Gilbert up-conversion mixer in a commercial 65-nm CMOS process is presented. The proposed CMOS Gilbert up-conversion mixer can be switched between subharmonic and fundamental operation modes by simply changing its bias, and thus is suitable for dual-band applications. This is appealing for 5 G MMW systems to reduce the system size and increase the versatility.

Circuit design

Figure 1 shows the schematic of the proposed MMW dual-mode and dual-band switchable CMOS Gilbert up-conversion mixer. It is composed of three levels of sub-circuits. The lower-level sub-circuit (M_1–M_2) acts as a transconductance stage, which converts the intermediate frequency (IF) input signal to output current. The middle-level sub-circuit (M_3–M_8) is composed of a switching quad (M_3–M_6) and a differential common-gate stage (M_7–M_8). The bias voltages of the switching quad and the differential common-gate stage are provided through two switches, i.e. SW_1 and SW_2, which are controlled by the control voltage V_C. The upper-level sub-circuit (M_9–M_{12}) acts as another switching quad. The two stacked switching quads are driven by two quadrature LO signals, i.e. LOI and LOQ, respectively, which are generated by a 90° coupler and two Marchand baluns [11, 12]. By adding four bypass capacitors (C_4–C_7), the LO baluns could provide dc bias voltages (V_A and V_{G3}) for the top and bottom switching

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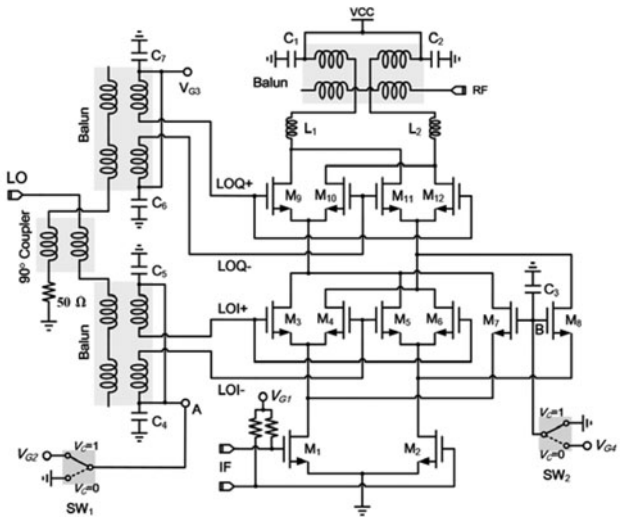

Fig. 1. Schematic of the proposed MMW dual-mode and dual-band switchable CMOS Gilbert up-conversion mixer.

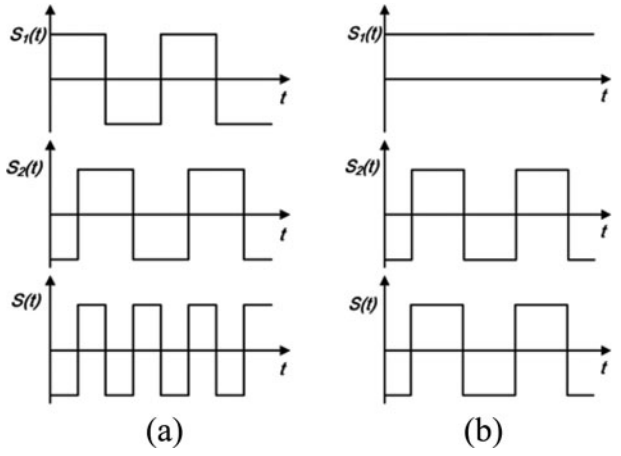

Fig. 2. Switching functions of the proposed CMOS Gilbert up-conversion mixer for (a) subharmonic operation mode and (b) fundamental operation mode.

quads without affecting the LO characteristics. The up-converted RF differential output signals are directed to a Marchand balun [13] for differential to a single output, while the inductors L_1 and L_2 are inserted between the RF balun and the top switching quad for RF impedance matching.

To better understand the operation of the proposed CMOS Gilbert mixer, let us define $S_1(t)$ as the switching function of the middle-level sub-circuit (M_3–M_8), and $S_2(t)$ as the switching function of the upper-level sub-circuit (M_9–M_{12}). Since the IF current is sequentially multiplied by $S_1(t)$ and $S_2(t)$, the equivalent switching function of the whole circuit can be expressed as $S(t) = S_1(t)S_2(t)$.

When $V_C = 1$ V, the differential common-gate devices M_7–M_8 are in off-state, while the gates of the transistors M_3–M_6 are biased at V_{G2} (i.e. $V_A = V_{G2}$), which is around the turn-on voltage of the bottom switching quad. In this case, $S_1(t)$ equals to the switching function of the bottom switching quad. On the other hand, $S_2(t)$ equals to the switching function of the top switching quad. Assuming hard switching of the transistors, $S_1(t)$ and $S_2(t)$ can be represented as two square waves aligned with the two LO signals (i.e. LOI and LOQ), as illustrated in Fig. 2(a). Since LOI and LOQ are in quadrature, the switching frequency of $S(t)$ is doubled, as shown in Fig. 2(a). Thus, subharmonic mixing is obtained. Specifically, the whole circuit operates as a Gilbert stacked-LO subharmonic mixer [14], which has the advantages of high conversion gain and high port-to-port isolation while requiring a low LO pumping power.

When $V_C = 0$ V, the differential common-gate devices M_7–M_8 are activated, while the gates of the transistors M_3–M_6 are biased at 0 V. The bottom switching quad is in the off-state during both the positive and negative excursions of LOI as long as $V_{LOI} < V_{DT} + V_{TH}$, where V_{LOI} is the voltage amplitude of LOI, V_{DT} is the drain voltage of the IF transconductance stage, and V_{TH} is the threshold voltage of the transistor. In this case, $S_1(t)$ equals to the switching function of the differential common-gate stage and therefore can be represented as a constant in the time diagram. Therefore, the switching frequency of $S(t)$ equals to that of $S_2(t)$, as shown in Fig. 2(b). Since $S_2(t)$ still equals to the switching function of the top switching quad, fundamental mixing is obtained. In particular, since the lower- and middle-level sub-circuits are acting as a differential cascode amplifier, the conversion gain of the mixer can be improved. It should be noted that the condition $V_{LOI} < V_{DT} + V_{TH}$ is necessary during the operation of the fundamental mode, otherwise, the bottom switching quad will be activated during the positive excursion of LOI and the conversion gain of the mixer would drop rapidly. The simulation indicates that the LO pumping power should be lower than 8 dBm for the operation of fundamental mixing mode.

By exploiting these two distinct mixing modes of operation, the proposed CMOS Gilbert up-conversion mixer can be adopted to cover two different MMW bands for dual-band applications.

For the mixer design, the selection of device size and bias point is critical. Theoretically, larger devices have a higher transconductance and hence should result in a higher conversion gain. However, they also suffer from larger parasitic capacitances and higher dc power consumption. Therefore, a trade-off should be concerned during the device selection. In this design, the gate width is 20 μm for M_3–M_{12} and is 40 μm for M_1–M_2. The bias voltages are first investigated to make sure that the devices are in saturation, and then are optimized for each mode to obtain sufficient conversion gain and low dc power consumption. The final bias voltages are $V_{G1} = 0.45$ V, $V_{G2} = 0.7$ V, $V_{G3} = 0.9$ V, and $V_{G4} = V_{CC} = 1$ V.

An Agilent ADS corresponding to a Taiwan Semiconductor Manufacturing Company design kit was employed for circuit simulation. The passive structures, including the inductors, capacitors, coupler, and Marchand baluns, were simulated by ADS Momentum, and the whole circuit was simulated by ADS harmonic-balance simulator.

Experimental results

The proposed MMW dual-mode and dual-band switchable Gilbert up-conversion mixer is designed and fabricated in commercial 65-nm CMOS technology. The chip photo is shown in Fig. 3. The chip size is 0.5 mm^2, including all pads and dummy metal. The measurements of the circuit are performed via on-wafer probing with 150 μm pitch coplanar ground-signal-ground probes. The input IF signal is generated by a vector signal generator (Agilent E8267D), the LO source is generated by an analog signal generator (Agilent E8257D), and the up-converted RF signal (the upper sideband) is measured by a spectrum analyzer (Agilent N9030A). The

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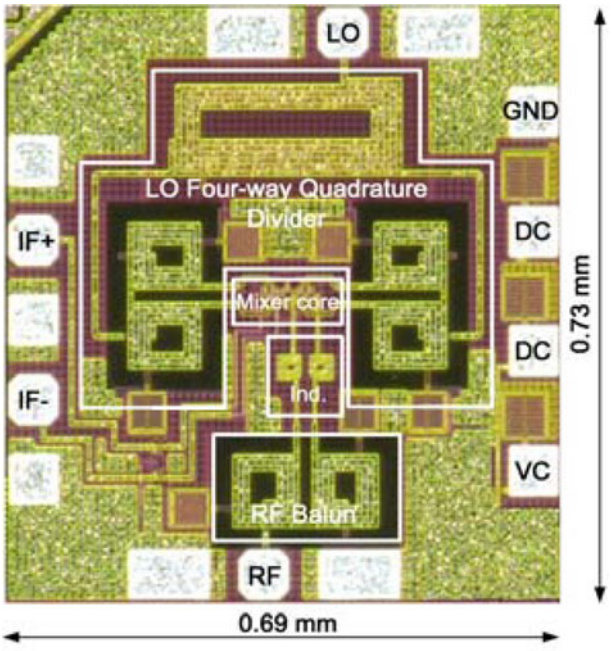

Fig. 3. Chip photo of the proposed CMOS Gilbert up-conversion mixer.

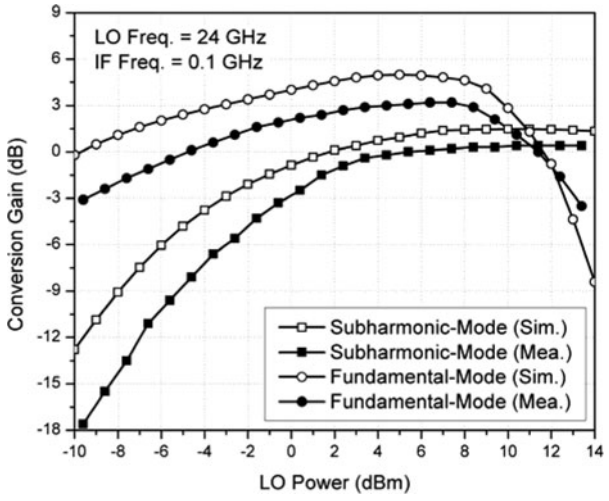

Fig. 4. Simulated and measured conversion gains versus LO power for both subharmonic and fundamental modes.

insertion losses of the probes and cables were measured by a PNA-X network analyzer (Agilent N5245A) and de-embedded from the measured results. Under 1-V supply voltage, the proposed CMOS Gilbert mixer draws 6 mA of dc current in both subharmonic and fundamental operation modes.

Figure 4 shows the simulated and measured conversion gain of the proposed CMOS Gilbert up-conversion mixer for both subharmonic and fundamental modes versus LO power. The LO frequency is fixed at 24 GHz and the IF frequency at 0.1 GHz. As can be observed, an LO power of 3 dBm is required to achieve a good conversion gain for both subharmonic and fundamental modes. In addition, as expected, the measured conversion gain of the mixer in the fundamental mode drops rapidly when the LO power is higher than 8 dBm. In the following measurements,

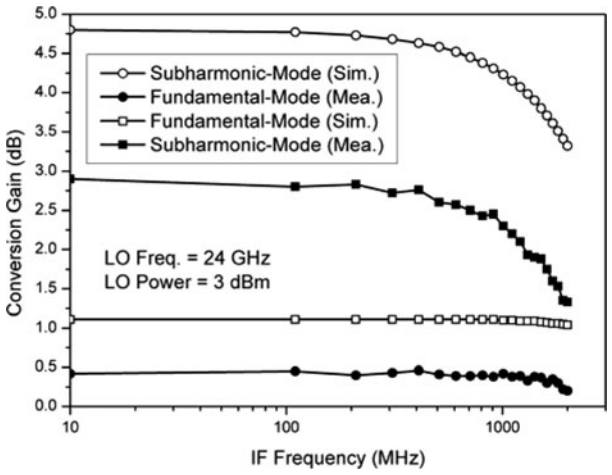

Fig. 5. Simulated and measured IF bandwidth for both subharmonic and fundamental modes.

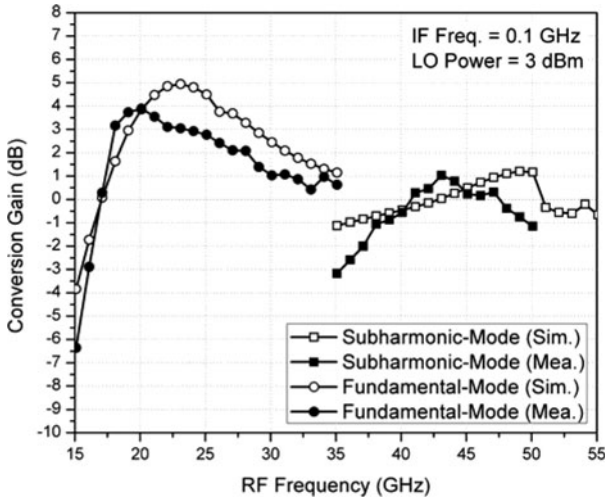

Fig. 6. Simulated and measured conversion gains for both subharmonic and fundamental modes.

the LO pumping power (i.e. the output power at the tips of the LO probe) is fixed at 3 dBm. To level the LO power with frequency variation, the insertion losses of the probe and cable on the LO path versus LO frequency, which have been measured by PNA, should be compensated at the output of the LO signal generator.

Figure 5 shows the simulated and measured IF bandwidth of the proposed CMOS mixer for both operation modes. As can be observed, the IF bandwidth is larger than 2 GHz and 1.5 GHz for the subharmonic and fundamental modes, respectively. Without loss of generality, a single tone with the frequency of 0.1 GHz is used for the IF input signal in the following measurements.

Figure 6 shows the simulated and measured conversion gains versus RF frequency for both operation modes. The proposed CMOS Gilbert up-conversion mixer exhibits a measured conversion gain of -0.5 ± 1.5 dB from 37 to 50 GHz and 2.5 ± 1.5 dB from 17.5 to 32 GHz for the subharmonic and fundamental modes, respectively. The two operation bands cover the 24.75-27.5 GHz and 37-42.5 GHz bands for 5 G MMW applications.

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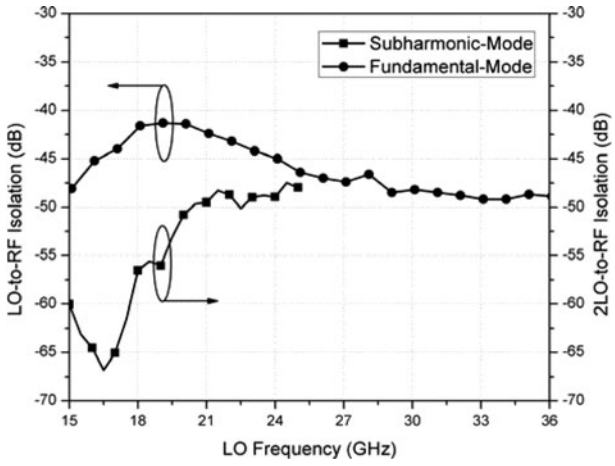

Fig. 7. Measured LO-to-RF and 2LO-to-RF isolations.

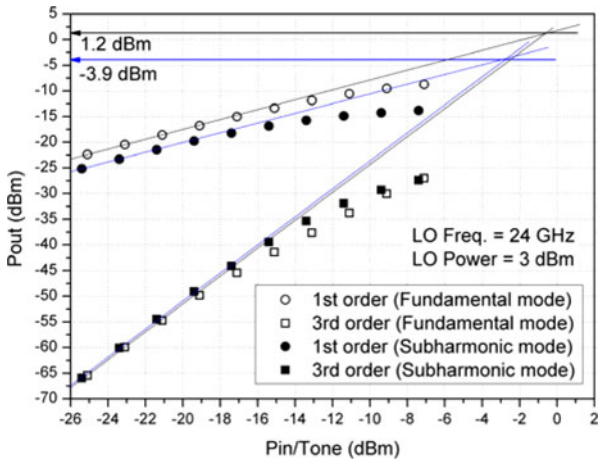

Fig. 9. Measured OIP_3 for both subharmonic and fundamental modes.

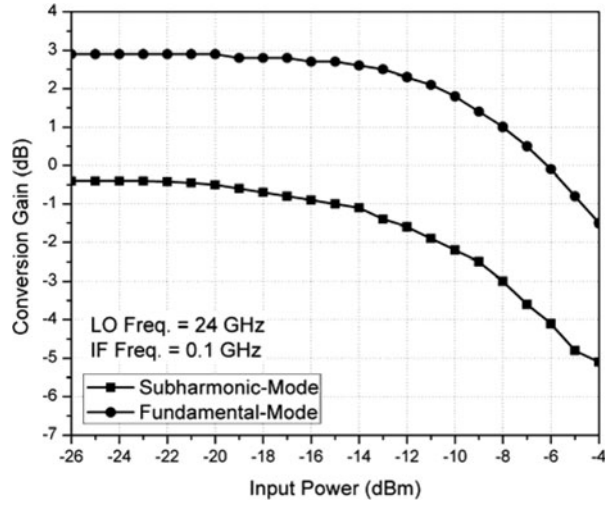

Fig. 8. Measured conversion gains versus the IF input power for both subharmonic and fundamental modes.

The discrepancy between the simulation and measurement shown in Figures 4–6 is mainly due to the inaccurate modeling of the transistors, non-predictable parasitic effects of the layout, and inaccurate extraction of the effective relative permittivity of the multi-layered substrate. In fact, general device models provided by foundry are not guaranteed above a certain frequency range (e.g. <30 GHz) and do not include the parasitic effects due to the interconnects within the transistors, which can be very significant at MMW frequencies. The pads and lossy substrate also introduce considerable high-frequency parasitic effects. Besides, unwanted coupling effects between neighboring structures are not accurately predicted. Additionally, the inaccurate effective relative permittivity of the multi-layered substrate used in the layout simulation may cause frequency offset between the measured and simulated results.

Figure 7 shows that the measured 2LO-to-RF isolation for the subharmonic mode is higher than 47 dB and the measured LO-to-RF isolation for the fundamental mode is higher than 41 dB, respectively. Figure 8 shows the measured conversion gains for both operation modes versus the IF input power. The output 1 dB power compression point (OP_{1dB}) of the proposed CMOS Gilbert up-conversion mixer is −14.4 and −8.1 dBm for the

Table 1. Comparison of MMW CMOS subharmonic up-conversion mixer dies.

	[15]	[12]	[16]	This work
RF frequency (GHz)	35–65	18–26	36–42	17.5–32 & 37–50
Dual-band?	No	No	No	Yes
Harmonic order	2	2	2	1 & 2
Conversion gain*** (dB)	−6 ± 1.5*	−12 ± 0.5	5.3 ± 1.2**	2.5 ± 1.5 & −0.5 ± 1.5
LO power (dBm)	7*	7	5	3
dc power (mW)	75.9*	0	21.2**	6
OP_{1dB} (dBm)	−19*	−8	−10	−8.1 & −14.4
2LO-to-RF isolation (dB)	>50	>40	>50	>47
Chip area (mm^2)	0.78*	0.41	0.85	0.5
Tech.	0.13-μm CMOS	0.13-μm CMOS	65-nm CMOS	65-nm CMOS

*I/Q Modulator. **With RF buffer. ***Single sideband value.

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subharmonic and fundamental modes, respectively. To investigate the linearity of the mixer, an IF two-tone with frequency offset of 10 MHz is generated for the input. Figure 9 shows that the measured output third intercept point (OIP_3) of the proposed mixer is −3.9 and 1.2 dBm for the subharmonic and fundamental modes, respectively when the LO frequency is 24 GHz.

Table 1 shows the performance of the proposed CMOS Gilbert up-conversion mixer along with several other MMW CMOS subharmonic up-conversion mixer dies. The proposed CMOS Gilbert up-conversion mixer achieves good conversion gain in dual bands and high port-to-port isolation with a low LO pumping power and a low dc power consumption.

Conclusion

In this paper, an MMW dual-mode and dual-band switchable Gilbert up-conversion mixer using a commercial 65-nm CMOS process is presented. With a 3-dBm LO power and a 6-mW dc power consumption, the proposed CMOS up-conversion mixer exhibits a conversion gain of -0.5 ± 1.5 dB from 37 to 50 GHz and 2.5 ± 1.5 dB from 17.5 to 32 GHz for the subharmonic and fundamental modes, respectively. Both the 2LO-to-RF and LO-to-RF isolations are higher than 40 dB. The measured OP_{1dB} is −14.4 and −8.1 dBm for the subharmonic and fundamental modes, respectively. Compared with previously reported MMW CMOS subharmonic up-conversion mixers, the proposed CMOS Gilbert up-conversion mixer achieves good conversion gain and isolation performances for dual operation modes and dual frequency bands.

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