RESEARCH PAPER

Analysis and design of a high-gain 100–180-GHz differential power amplifier in 130 nm SiGe BiCMOS

FAISAL AHMED¹, MUHAMMAD FURQAN¹, KLAUS AUFINGER² AND ANDREAS STELZER¹

This paper presents the design and measurement results of a high-gain D-band broadband power amplifier (PA) implemented in a 130 nm SiGe BiCMOS technology. The topology of the PA is based on four differential cascode stages with interstage matching networks. A detailed analysis of the frequency behavior of the transimpedance-gain of the common-base stage of the cascode is presented by means of small-signal equivalent circuits, when the proposed four-reactance wideband matching network is used for output matching to the subsequent stage. The effect of the size of the active devices, in achieving a desired gain, bandwidth, and output power, is investigated. The fabricated D-band amplifier is characterized on-wafer demonstrating a peak differential gain and output power of about 25 dB and 11 dBm, respectively, while utilizing a DC power of 262 mW from a 2.7 V supply. The 3-dB small-signal bandwidth of the PA spans from 100 to 180 GHz (limited by the measurement setup), making it the first SiGe-based PA to cover the entire D-band frequency range. The PA achieves a state-of-the-art differential gain-bandwidth product of around 1.4 THz and the highest GBW/P_{DC} ratio of 5.2 GHz/mW among all D-Band Si-based PAs.

Keywords: Circuit design and applications, Modeling, Simulation and characterizations of devices and circuits

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I. INTRODUCTION

Many current and future applications such as high-speed communication services, software-defined radio, point-topoint wireless backhauls, instrumentation systems, highresolution radars, medical and security imaging systems, all strongly rely on broadband circuits and amplifiers. To enable these broadband building blocks and systems, technologies with high enough transit frequency (f_T) and maximum oscillation frequency (f_{max}) are required. Keeping in mind sufficient margins for reliable product development f_T and f_{max} should be at least three times higher than the maximum fundamental frequency of operation. However, with special techniques, accurate modeling and careful implementation, one can endeavor to design broadband amplifiers with cut-off frequencies reaching up to and even beyond $f_T/2$. Furthermore a sufficient enough breakdown voltage of the active device is also required to accommodate the required output voltage swing. One of the most technology demanding building blocks at these frequencies are millimeter-wave broadband power amplifiers (PAs), because of their simultaneous high f_{max} and breakdown voltage requirements.

¹Johannes Kepler University Linz, Altenberger Str. 69, 4040 Linz, Austria. Phone: +43 732 2468 6409 ²Infineon Technologies, Am Campeon, 85579 Neubiberg, Germany

Corresponding author:

F. Ahmed

Email: f.ahmed@nthfs.jku.at

Currently there are some technologies, which are able to provide such features, among which Indium Phosphide (InP) double heterojunction bipolar transistor (DHBT), InP high-electron mobility transistor (HEMT), and SiGe BiCMOS HBT are certainly at the fore-front. Recently, 30-nm InP HEMT devices reaching f_T and f_{max} beyond 0.6 and 1.2 THz, respectively, have been reported [1], with InP DHBTs not lagging much behind at f_T and f_{max} beyond 0.52 and 1.1 THz, respectively [2]. These III-V-technologies, keeping in view their higher breakdown voltages (especially for high-speed drivers) together with their cut-off frequencies are certainly best suited for standalone circuits such as PA modules in mobile phones. However, SiGe HBTs provide an unequivocal advantage of integration of high-speed bipolar devices with advanced CMOS, allowing for area/cost effective systems-on-chips (SoCs) and system-in-packages (SiPs) [3], with lower power consumption and high-temperature performance [4]. Furthermore, in terms of cut-off frequencies advanced SiGe devices by significantly reducing the external base resistance have achieved peak f_{max} of 700 GHz [5–8].

II. BROADBAND AMPLIFICATION APPROACHES: DISTRIBUTED VERSUS LUMPED

Broadband performance of both low-frequency and millimeter-wave (mm-wave) amplifiers has been achieved in

general by using two different design approaches, namely the distributed integrated circuits and the conventional lumped circuits [9, 10]. One major advantage of the distributed approach is that the parasitic capacitance of the transistors can be designed to be absorbed as part of the transmission line's parameters; and as the effective highest frequency of operation of a technology is much lower than its f_T on account of the parasitics associated with the active and passive components, this results in avoiding a sharp frequency roll-off and in achieving a gain-bandwidth product much larger than the conventional lumped circuit design. However, the bandwidth extension achieved through a distributed approach is inherently linked to larger time delays between input and output and hence a circuit with higher group delays. Furthermore, on account of usage of transmission lines and higher number of gain stages, the physical size of the circuits becomes significantly larger than the lumped architectures. The distributed circuit design approach has been utilized in both Si/SiGe and III-V semiconductors. In [11] a fully-integrated 250 nm, InP HBT based distributed amplifier (DA) was presented, which was designed using four cascode gain stages with inductive peaking. The amplifier achieved 10 dB gain, a 3-dB bandwidth of 182 GHz (40-222 GHz), and a P_{SAT} of 8.5 dBm at 134 GHz. Using 35 nm mHEMT process a 3-dB bandwidth of 96 GHz from 50 to 146 GHz was achieved with a P_{SAT} of 13 dBm at 140 GHz [12]. In [13], one of the highest reported bandwidths of 235 GHz was achieved in InP DHBT, but no large signal characterizations were presented. Recently, in 130 nm SiGe BiCMOS process a 3-dB bandwidth of 180 GHz with a peak gain of 18.7 dB has been demonstrated using cascaded DAs with electrically trimmable resistors. However, a measured output power of only 2.5 dBm is achieved at 100 GHz [14]. On the other hand, achieving high bandwidths/power in mm-wave using lumped circuit approach is strongly dependent on technology parameters. Bandwidths of up to 30 GHz [15], and 40 GHz [16] have been demonstrated for D-band medium PAs based on CMOS and SiGe HBT technologies. Thus so far, no Si-based amplifier capable of delivering more than 5 dBm output power over the entire D-band has been reported. This paper is an extension of the reported PA in [17].

III. ANALYSIS OF BROADBAND MULTISTAGE MATCHING BASED ON CASCODE AMPLIFIERS

Although a common-base (CB) or a common-gate (CG) amplifier provides a wide input match with an input impedance (approximately given by $1/g_m$), which can be directly matched to a 50- Ω source, the gain-per-stage is quite low, and for achieving reasonable gains the CB stage is followed by a common-emitter (CE) or a cascode stage [18]. However, the CE or the cascode stage significantly limits the bandwidth. This paper presents a method to overcome this limitation, while taking advantage of high-gain and output power capability of the cascode stage. A single cascode stage with the input/ output matched to a real impedance can provide a relatively broader frequency response, when using a higher number of reactive elements [16]. However, when more stages are cascaded, the bandwidth of the amplifier starts to suffer. Furthermore, when operating in mm-wave region the additional loss occurring at each input and output matching network becomes non negligible. The input impedance of the cascode stage is considerably less reactive as compared to its output impedance, and with a proper device size selection a fairly good wideband input match can be attained even using a simple two-reactance matching network. Furthermore, for multistage designs the gain and bandwidth is strongly determined by the interstage matching. For a multistage cascode amplifier, the interstage matching is between the output of a CB stage and the input of the subsequent CE stage. The highfrequency equivalent π -model of a cascode stage showing the input matching to a source, and the interstage matching to the CE-stage is presented in Fig. 1(a). The input matching consists of a simple L-type matching network, while the interstage network is designed using four reactances. The input impedance of the next stage is denoted by $Z_{\pi 2}$ being composed of $C_{\pi 2}$ and $r_{\pi 2}$. As mentioned earlier the input matching does not play a major role in determining the gain profile over frequency, and as such the transimpedance-gain (v_0/i_1) of the CB stage plays the most significant role in defining the overall frequency response. A model for determining the transimpedance-gain is shown in Fig. 1(b), where the input current is represented by a current source i_1 . This model can be further simplified if it is considered that $\beta + 1 \approx \beta$, which means that the base current is neglected. This consideration is especially valid when the circuit is operated at a high collector voltage, in which case the positive base current is compensated by the reverse current of the base-collector junction, a point known as base-current-reversal (BCR). Furthermore, on neglecting the collector output resistance $r_{\rm o}$, the model is further simplified (as shown in Fig. 1(c)), and the calculated transimpedance function is given by

$$\frac{\nu_o}{i_1} = -\frac{Z_{L2}Z_{\mu_1}Z_{\pi_2}}{Z_{L2}(Z_{L3} + Z_{\mu_1}) + Z_{L3}Z_{\mu_1} + Z_{C1}(Z_{L1} + Z_{L2} + Z_{\mu_1})}, + (Z_{L2} + Z_{\mu_1})Z_{\pi_2} + Z_{L1}(Z_{L2} + Z_{L3} + Z_{\pi_2})$$
(1)

where Z_{L_1} , Z_{L_2} , Z_{L_3} , Z_{C_1} , Z_{μ_1} and Z_{π_2} are the impedances associated with L_1 , L_2 , L_3 , C_1 , C_{μ_1} , and $C_{\pi_2} || r_{\pi_2}$, respectively. This transfer function has two poles, given by

$$\omega_p^2 = \frac{B \pm \sqrt{B^2 - 4AC}}{2A},\tag{2}$$

where

$$A = C_1 C_{\mu 1} C_{\pi 2} (L_1 L_2 + L_1 L_3 + L_2 L_3),$$
(3)

$$B = C_{\mu_1}L_1(C_1 + C_{\pi_2}) + C_1L_2(C_{\mu_1} + C_{\pi_2}) + C_{\pi_2}(C_{\mu_1}L_2 + C_1L_3),$$
(4)

$$C = C_1 + C_{\pi_2}.$$
 (5)

As seen by the equations the location of these two poles can be adjusted by means of the matching elements and the device parameters, most significantly by C_{μ_1} and C_{π_2} , as r_{π_2} has a very weak effect and can be neglected. A simulated plot



Fig. 1. (a) High-frequency equivalent π -model of the cascode stage with the proposed output interstage broadband matching network. (b) Model for calculating the transimpedance transfer function. (c) Simplified model when the CB base current and r_0 is ignored.

(using the Spectre RF Gummel-Poon model) of the transimpedance-gain is shown in Fig. 2(a) $(L_1 = 35 \text{ pH},$ $L_2 = 35$ pH, $L_3 = 60$ pH, $C_1 = 23$ fF, and emitter-size of both CB and CE stage = $0.13 \times 10 \ \mu m^2$). The presence of two peaks in the transfer function is clearly visible, which helps to extend the bandwidth. Another graph is plotted using the exact analytical expression derived from Fig. 1(b) and shows an excellent match with the simulation. The smallsignal equivalent circuit parameters for the calculated plots are directly extracted from the Gummel-Poon model of the HBT following the procedure described in [19] ($C_{\mu_1} = 14$ fF, $C_{\pi_2} =$ 60 fF, $r_{\pi 2}$ = 50 Ω, r_0 = 1.5 kΩ, and f_T = 270 GHz). The much simplified model (cf. Fig 1(c)) also shows a very good correlation with the simulated plots, which confirms the validity of the zero-base-current assumption. Thus, equations (1)-(5)can be used for initial design steps of designing a wideband response. Proper device size selection remains a critical part of both LNA and PA design procedures, especially in mm-wave frequency range. The variation of C_{μ} and C_{π} with increasing HBT device size is plotted in Fig. 2(b), which shows that C_{π} varies more strongly with device size as compared with C_{μ} and therefore should be carefully considered while designing. For LNA design usually smaller size HBTs are preferred because of their higher gain and better noise performance [20, 21]. The smaller size translates into lower bias currents and lower power consumption, considering that in mm-wave operation the current density is usually kept close to peak- f_T current density. However, smaller devices have much limited output power capability, which is especially important for PA designs. The effect of device size selection on the frequency response of the transimpedance-gain is investigated by varying the device size of the CB-stage and the CE-stage individually, and is plotted in Figs 2(c) and 2(d) using (1). It is seen in Fig. 2(c) that as size of the CB-stage is decreased (which translates to a decrease in $C_{\mu 1}$), the poles of the transfer-function move apart with a decrease in the overall gain. On the other hand, the location of the poles is not much affected when the device size of the CE-stage is varied, but there is an increase in gain-peaking with larger device areas, accompanied with a drop in mid-band gain. This gives us an insight that while using the four-reactance matching network, larger fractional bandwidths can be attained using smaller HBTs. The presented analysis has shown how a wideband frequency response can be achieved using the transimpedance-gain profile of two cascode stages. However, there is a drop in the midband gain with increased bandwidth. This decrease in gain can be compensated using staggered-gain tuning of multiple stages. This approach will be further explained in the circuit design section.

IV. CIRCUIT DESIGN

The broadband PA is designed in Infineon's advanced SiGe BiCMOS technology B11HFC. The process features HBTs with a minimum effective emitter width of 130 nm, which has an f_T/f_{max} of 250/370 GHz and a collector–emitter breakdown voltage BV_{CEO} of 1.5 V. Two thick copper layers are available for RF transmission lines and additional four thin layers for interconnections. The major goal of the design was to achieve a 3-dB bandwidth covering at least the entire D-band (110–170 GHz). Secondary goals were high-gain, good output power, and noise figure. Such performance metrics make the design and the amplifier especially suitable to be used both as an input and/or output amplifier for high-resolution radar sensors. The schematic of the designed PA is shown in Fig. 3(a). Following the approach outlined in the analysis, first a wideband transimpedance-gain profile is



Fig. 2. (a) Transimpedance-gain of the CB-stage when matched to the next CE-stage, plotted using the high-frequency analytical model (cf. Fig. 1(b)), the simplified model (cf. Fig. 1(c) and (1)), and Spectre RF simulation. (b) Simulated C_{μ} and C_{π} of the high-frequency HBTs as a function of their device size. The effective emitter-width is kept constant at 0.13 μ m, while the emitter-length is varied (1 μ m, 5 μ m, 10 μ m, 7 × 2 μ m², and 10 × 2 μ m²). (c) The analytical plots for the variation of the transimpedance-gain over frequency as a function of device size of the CB-stage (C_{µ1}), size of CE-stage is 0.13 × 10 μ m².

designed using the first two cascode stages and the fourreactance matching network. HBTs with 6 µm emitter-length with double-base, double-collector configuration are selected for the first stage. The device size allows for a wideband input match to a 100- Ω source with a simple L-type matching network, while simultaneously allowing for a high-gain and good noise performance. The multiple base and collector contacts help in reducing the series resistance and achieving a uniform contact current. The transimpedance-gain profiles for the four stages are plotted in Fig. 3(b). These profiles are very similar to the power-gain profiles presented in [17]. The second- and third-stage transimpedance is designed such that the bandwidth is further increased. The size of the devices is also increased to have total emitter length of 8 and 10 µm, respectively, which helps to increase output power. However, as shown in Fig. 2(d), the increased C_{π} of the subsequent stage, leads to a drop in midband gain. This midband gain is then compensated using the last stage (emitter length, 12 µm) with a tuned gain maximum around 150 GHz. The effect of this staggered tuning is evident in Fig. $_{3}(c)$. The first two stages provide a relatively uniform gain over a wide bandwidth, the third stage increases the bandwidth further but the gain ripple is much more pronounced, and the final stage with the largest device size, achieves the desired bandwidth and gain flatness. A carefully designed layout is one of the most critical aspect of highfrequency circuit design. This is especially important when designing in the mm-wave range. The placement of the active/passive devices, the layout of the transmission lines and the via stacks should be done in a way to reduce unwanted coupling and parasitics (e.g. using non-parallel lines, using large inter-line spacing, etc.) and the overall layout to be as symmetric as possible. The layout of the first two stages of the amplifier is presented in Fig. 4(a). All the contact and via parasitics have been simulated in Sonnet. In order to characterize the broadband amplifier a modified wideband Marchand balun was designed in CST Microwave Studio (cf. Fig. 4(b) following the approach presented in [22]. The balun is based on three folded symmetric coupled lines each of 2.4 μ m width with a spacing of 3.3 μ m. The open-ended $\lambda_{g}/2$ line is about 445 μ m. The symmetric coupled line reduces the phase velocity difference by means of increased mutual capacitance, which leads to an improved amplitude imbalance over a wide bandwidth.

V. MEASUREMENTS

The chip micrograph of the D-band PA including the input/ output modified Marchand balun is shown in Fig. 5(a). The



Fig. 3. (a) Schematic representation of the D-band broadband PA. (b) Simulated transimpedance-gain of the individual stages (calculated from the CB-stage to the input of the next CE-stage) of the D-band broadband amplifier. (c) Combined power-gain profiles of the amplifier emphasizing the effect of staggered-gain tuning.

core amplifier is highly compact and occupies an area of only 0.1 mm². Because of the very high operation bandwidth the small- and large-signal measurements are performed over the W- and D-bands. Measurements beyond 180 GHz could not be performed because of lack of signal-source in this frequency range. Frequency extenders from R&S and OML were used in the W- and D-band frequency range, respectively, in conjunction with R&S ZVT20 VNA. Additionally, because of limited output power of the D-band converters, an external F-band (90–140 GHz) frequency multiplier from RPG was used to conduct large signal measurements. The Marchand balun was characterized separately on a cut-out, as shown in Fig. 5(b). Because of the unavailability of three-port measurements, the single balun was integrated with on-chip 50- Ω tantalum based load resistors together with aluminum fuses, to measure amplitude and phase imbalance at both ports. The simulated and measured results are shown in Fig. 6(a), with a 2-dB insertion loss bandwidth of more than 60 GHz. Some differences in simulation and measurements (especially in the return-loss) are expected due to the non-ideal and frequency-dependent behavior of the on-chip tantalum resistor and the fuse (which are not accounted for in CST while using waveguide ports). Another measurement was performed on a back-to-back balun for calculating the total loss. The



Fig. 4. (a) Layout design of the first two cascode stages of the PA in Sonnet. (b) Perspective view of the D-band modified Marchand balun simulated in CST.



Fig. 5. Chip micrographs. (a) Differential D-band broadband PA with integrated baluns. Chip size including pads: $0.7 \times 0.6 \text{ mm}^2$. (b) D-band wideband modified Marchand balun. Chip size including pads: $0.425 \times 0.4 \text{ mm}^2$.

differential small-signal gain of the PA with a peak gain of 24.8 dB (balun loss is de-embedded) while drawing 97 mA from a 2.7 V supply, is shown in Fig. 6(b). The measured 3-dB bandwidth extends from 100 GHz to more than 180 GHz and

shows a fairly good correlation with the simulation. Simulations show a minimum noise figure of < 10 dB and a very flat response throughout the D-band. Measurements could not be performed because no D-band noise source was



Fig. 6. Small-signal measurements (solid lines) and simulations (dotted lines). (a) Insertion loss and input reflection coefficient of the modified Marchand balun. (b) Small-signal gain and NF of the PA. (c) Input/output reflection coefficients and isolation of the PA. (d) μ -factor and group-delay of the PA.



Fig. 7. Large-signal measurements (solid lines) and simulations (dotted lines). (a) Saturated output power and 1-dB output compression point of the PA versus frequency at a constant 2.7 V supply. (b) Output power, power-gain and PAE of the PA as a function of input power at 160 GHz. (c) Saturated output power, and (d) PAE, as a function of supply voltage and two different biasing conditions adjusted for optimal power efficiency (bias 1) and optimal output power (bias 2) at 160 GHz.

available. Input/output reflection coefficients and the reverse isolation of the PA are shown in Fig. 6(c). The measured μ -factor of >1 shows unconditional stability of the amplifier throughout the operating range. The group delay response of the PA is presented in Fig. 6(d) and shows an average value of about 40 ps with a group delay variation of about ± 15 ps within the entire D-band, which is a reasonable performance for full-band highspeed broadband communications. The first set of large-signal measurements (cf. Figs 7(a) and 7(b)) were taken at a supply voltage of 2.7 V and with the same biasing as in the case of smallsignal results. The measured differential P_{SAT} is greater than 7.6 dBm over the entire D-band. The P_1 dB is also quite flat over frequency and varies around 3.9 dB in the D-band. The behavior of the output power, gain and PAE versus input power is plotted in Fig. 7(b), showing a peak differential output power of 11 dBm at 160 GHz. Using the external bias

Table 1. Performance comparison of Si-based PAs in Si/SiGe processes.

Technology	Frequency (GHz)	BW* (GHz)	Gain (dB)	GBW (GHz)	OP _{peak} (dBm)	P_{DC} (mW)	GBW/P _{DC} (GHz/mW)	Area (mm ²)	Ref.
65 nm CMOS	125-155	30	15	168.7	13.2(@140 GHz)	143	1.18	0.38	[15]
65 nm CMOS	135-165	30	16	189.3	12.2(@150 GHz)	137	1.38	0.38	[15]
130 nm SiGe†	135-170	35	17	247.8	8(@170 GHz)	320	0.77	0.58	[23]
90 nm SiGe	110-134	24	15	135	20.8(@126 GHz)	1520	0.09	4.95	[24]
130 nm SiGe†	154-159	5	35.4	294	14(@162 GHz)	504	0.58	0.06‡	[25]
90 nm SiGe	107-142	35	7.7	84.9	22(@120 GHz)	2220	0.04	0.62	[<mark>26</mark>]
130 nm SiGe†	140-180	40	20	400	7(@165 GHz)	132	3.0	0.37	[16]
130 nm SiGe†	100-180	80	24.8	1390	11(@160 GHz)	262	5.2	0.42	This
					9(@170 GHz)				work

*Small-signal 3-dB.

†Differential results.

‡Core-area only.

pads available on chip (V_{B_1} to V_{B_4} as shown in Fig. 5(a)), two further sets of power measurements were carried out at a frequency of 160 GHz. For Bias 1 (V_{B_1} to V_{B_4} optimized for high PAE), a current density slightly lower than the recommended peak- f_T current density at a V_{CC} of 2.7 V is selected. When V_{CC} is raised, the voltage and the current swing is increased until reaching its maximum value about 2.9 V, at which output power is increased by 0.5 dB at the expense of reduced PAE. For Bias 2 (V_{B_1} to V_{B_4} optimized for high output power), the current density is reduced much further, so that this time the maximum current swing limit is reached around 3.1 V (cf. Fig. 7(c)) and achieves the highest output power of about 12 dBm with a PAE of about 4.5%. The designed PA is compared with the published state-of-the-art Si-based PAs working in the D-band in Table 1.

VI. CONCLUSION

This paper presented the analysis and design of the first full D-band Si-based PA. Relying on high-frequency π -model of a cascode stage, analytical expressions for transimpedancegain are developed which help in understanding the behavior, dependencies, and best method of achieving wideband frequency response. Following the procedure four cascode stages are staggered tuned to realize a 57% 3-dB bandwidth of 80 GHz, the highest for any lumped circuit design operating in the D-band. The design also achieves the highest GBW/ P_{DC} ratio of 5.2 for D-band PAs. Based on its characteristics, the PA finds its use in many applications such as very high-resolution radars, wideband instrumentation systems, and ultrahigh-speed communications systems.

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Faisal Ahmed (S'15) received the B.E. degree in electronic engineering from N.E.D. University of Engineering and Technology, Karachi in 2006, and the Master's degree in Microwave Engineering from Technical University of Munich, Germany in 2009 (both with Distinctions). Currently he is working toward the Ph.D. degree at the Institute

for Communications Engineering and RF-Systems, Johannes Kepler University, Linz, Austria. His research focuses on analog integrated circuit and system design for millimeter and terahertz waves for radar sensors, and microwave imaging.



Muhammad Furqan (S'12) received the B.E. degree (with Distinction) in Electronic Engineering from N.E.D. University of Engineering and Technology, Karachi in 2006, and the Master's degree (with Distinction) in microwave engineering from Technical University of Munich, Germany in 2009. Currently he is working toward the Ph.D. degree at

the Institute for Communications Engineering and RF-Systems, Johannes Kepler University, Linz, Austria. His research interests include circuit and system design for millimeter-wave communication systems and microwave radar sensors.



Klaus Aufinger (M'09) was born in Kirchbichl, Austria, in 1966. He received the Diploma and Ph.D. degrees in Physics from the University of Innsbruck, Innsbruck, Austria, in 1990 and 2001, respectively. From 1990 to 1991, he was a Teaching Assistant with the Institute of Theoretical Physics, the University of Innsbruck. In 1991, he joined

Corporate Research and Development, Siemens AG, Munich, Germany, where he investigated noise in

submicrometer bipolar transistors. He is currently with Infineon Technologies AG (the former semiconductor group of Siemens), Neubiberg, Germany, where he is involved in the field of device physics, technology development, and modeling of advanced SiGe technologies for high-speed digital and analog circuits.



Andreas Stelzer (M'oo)) received the Diploma Engineer degree in Electrical Engineering from the Technical University of Vienna, Vienna, Austria, in 1994, and the Dr. techn. degree (Ph.D.) in mechatronics (with honors sub auspiciis praesidentis rei publicae) from the Johannes Kepler University Linz, Austria, in 2000. In 2003, he became the Associ-

ate Professor with the Institute for Communications Engineering and RF Systems, Johannes Kepler University Linz. Since 2008, he has been a key researcher for the Austrian Center of Competence in Mechatronics (ACCM), where he is responsible for numerous industrial projects. In 2007, he was granted a Christian Doppler Research Laboratory for Integrated Radar Sensors and since 2011 he has been a full Professor at the Johannes Kepler University Linz, heading the Department for RF-Systems. He has authored or coauthored over 360 journal, conference, and workshop contributions. His research is focused on microwave sensor systems for industrial and automotive applications, integrated radar sensor concepts, SiGe-based circuit design, microwave packaging in eWLB, RF and microwave subsystems, surface acoustic wave (SAW) sensor systems and applications, as well as digital signal processing for sensor signal evaluation. Dr. Stelzer is a member of the Austrian ÖVE. He has served as an associate editor for the IEEE MICROWAVE AND WIRELESS COM-PONENTS LETTERS. Currently he serves as Chair for MTT-27 Wireless-Enabled Automotive and Vehicular Applications. He was recipient of several awards, including the 2008 IEEE Microwave Theory and Techniques Society (IEEE MTT-S) Outstanding Young Engineer Award and the 2011 IEEE Microwave Prize. Furthermore, he was recipient of the 2012 European Conference on Antennas and Propagation (EuCAP) Best Measurement Paper Prize, the 2012 Asia Pacific Conference on Antennas and Propagation (APCAP) Best Paper Award, the 2011 German Microwave Conference (GeMiC) Best Paper Award, as well as the EEEfCOM Innovation Award, and the European Microwave Association (EuMA) Radar Prize of the European Radar Conference (EuRAD) 2003. He is a member of the IEEE MTT, IM, and CAS Societies and he serves as IEEE Distinguished Microwave Lecturer for the period 2014-2016.