International Journal of Microwave and Wireless Technologies, 2012, 4(2), 233–239.
doi:10.1017/S1759078711001073

RESEARCH PAPER

Design of high transformation ratio millimeter-wave integrated transformers

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A novel topology for millimeter-wave-integrated transformers is proposed. The windings are stacked and secondaries are designed with different trace widths and different diameters from that of the primary, in order to obtain relatively high-inductance transformation ratios. Measurement and simulation results of 65 nm Complementary Metal Oxide Semiconductor (CMOS) and 130 nm combination of Bipolar and CMOS (BiCMOS) transformers present the impact of this structure on the inductances, quality factor, coupling coefficient, and minimum insertion loss. Within certain limits on the trace widths, it is shown that the proposed topology not only increases the transformation ratio but also improves its overall performance.

Keywords: Transformers, integrated circuits, millimeter-wave, impedance matching

Received 24 March 2011; Revised 8 November 2011; first published online 5 January 2012

I. INTRODUCTION

Integrated transformers represent an important component on the design of RF integrated circuits. They have been extensively used as part of wireless transceivers which comply with communications standards operating in frequencies inferior to 10 GHz, such as Wi-Fi, Bluetooth, and Universal Mobile Telecommunications System (UMTS). Some important studies concerning the design and modeling of transformers at those frequencies are included in [1–4].

More recently, some relevant new applications have emerged in the millimeter-wave (mm-wave) range. Among them, one can mention the high data rate Wireless Personal Area Network (WPAN) and Wireless Local Area Network (WLAN) exploiting the unlicensed band in the vicinity of 60 GHz, the automotive radar at 77 and 79 GHz, and imaging at 94 GHz. At these frequencies, as well, the use of transformers has shown very useful properties [5–8].

Transformers can perform different functions in an integrated circuit. They are frequently employed as a balanced to unbalanced modes conversion element (balun). Their advantage over traditional transmission-line-based structures consists mostly on the lesser surface occupation and their wideband behavior. Transformers are also often included in matching networks within or between circuits in transceivers. They are also known to constitute effective power combiners, which are especially useful for parallel power amplifier topologies, and to perform DC decoupling and be part of feedback and resonant networks.

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As aforementioned, the use of transformers for impedance matching may be very interesting in an integrated circuit. In order to accomplish this task as efficiently as possible, it is important that the component provide a suitable impedance transformation from its primary to secondary coil.

Previous works have reported different techniques used to obtain the desired impedance ratios on integrated transformers. For RF transformers operating in lower frequencies, the adopted topology is usually based on multiturn spirals. The transformation ratios are hence obtained through the choice of a convenient turn ratio between primary and secondary. In those cases, the number of turns of a particular winding is generally limited to five [4, 9].

Nevertheless, even for those frequencies, different topologies have been proposed to achieve higher impedance ratios. In [4], for instance, all turns of one of the windings are connected in parallel in order to decrease its overall effective inductance. Lim *et al.* [10] extrapolate this idea by connecting the different primary turns several times in parallel. Moreover, a multi-layer approach is used to further increase secondary inductances.

At mm-waves, on the other hand, we cannot design transformers with more than two turns in a winding. A superior number of turns would imply a considerably low resonant frequency, so that proper mm-wave operation would not be possible, and higher losses would appear. For this reason, most of the transformers currently used in mm-wave-integrated circuits present stacked single-turn primaries and secondaries so that their inductance ratios are close to 1 [6, 11]. Hence, they are mostly suited to work as baluns.

Some transformers that perform impedance transformation at mm-waves can be seen in [5, 8]. Those transformers present a 1:2 turn ratio and an interleaved topology (primary and secondary implemented on the same metal layer). Additionally, in all those cases, the trace width of primary conductors is the same as that of the secondary.

A different approach is presented in [12]. For this transformer, the primary is placed within the secondary, i.e., the secondary completely encloses the primary both horizontally and vertically. In this case, the primary, which has two turns, presents narrower traces than the single-turn secondary.

In this paper, we propose a novel topology based on a stacked configuration, for which primaries and secondaries present different trace widths and diameters in order to achieve higher transformation ratios for frequencies inferior to 90 GHz in the mm-wave spectrum [13]. In Section II, the structure of the transformers is introduced and detailed. Section III reports the characteristics of the technologies that were employed in this study and specifies the adopted model and measurement setup. Finally, Section IV summarizes and discusses the obtained results.

II. TRANSFORMERS DESIGN

Our design employs a stacked topology, as shown in Fig. 1. The primary is implemented on the top copper metal layer available in the technology and the secondary on the layer immediately beneath. This allows the conductors to be as far as possible from the substrate, which reduces the associated capacitance. It also reduces the metallic losses, since, for many current technologies, the two top metal layers are considerably thicker than the others. Also, the choice of a stacked topology permits a smaller surface occupation and a stronger magnetic coupling between windings, as long as metal layers are sufficiently close in the vertical direction – as it is the case for the considered technologies. Moreover, in order to minimize losses, no shield is inserted between the conductors and the substrate [14] and the windings present an octagonal shape.

The proposed topology is based on two well-known principles of transmission lines and lumped inductances. First of all, the longer a line is, the higher its inductance will be. Considering the geometric parameters we adopt in our transformer design, it means that larger diameters will lead to higher inductances. Also, the wider a conductor trace is, the lower its respective inductance will be. Moreover, we also employ the number of turns as a parameter to obtain the desired impedance ratios. An inductor with two turns will present a higher inductance value not only for being electrically longer, but also due to the mutual inductance between turns.

The partial inductance of a conductor can be expressed by equation (1). It depends linearly on the length ℓ, and logarithmically on the width W and thickness t. This expression is derived from a fundamental formula for the mutual inductance between filaments, for which the distance separating them is replaced by the geometric mean distance among the points within a section of the conductor [15], and their length is considered much greater than the other dimensions:

$$L(\ell, W, t) = \frac{0.42\mu_0\ell}{\pi}\left[\ln\left(\frac{2\ell}{0.2235(W+t)}\right) + \frac{0.2235(W+t)}{\ell} - 1\right]. \quad (1)$$

Hence, we design a transformer presenting its primary and secondary with different conductor widths and different diameters. The dimensions should be comprised between the cases when inner diameters and outer diameters of the windings coincide, so that vertical coupling can take place. The minimum and maximum trace widths, on the other hand, should be determined by metal density rules, which are specific to each technological process.

Therefore, in order to achieve a transformation ratio as high as possible, the primary traces should be made as wide and the secondary traces as narrow as possible. Additionally, the primary must be single turn and the secondary would present two turns. Finally, the outer diameters of the windings should coincide, as in Fig. 1(b).

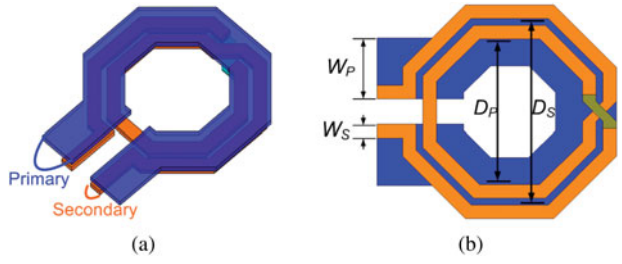

Fig. 1. Layout of stacked transformer with different diameters (D) and trace widths (W).

III. MODELING AND MEASUREMENT SETUP

A) Technologies

We designed integrated transformers applying the topology described in Section II, using two different technologies from STMicroelectronics. The 65-nm CMOS technology we used presents a moderate substrate resistivity (between 10 and 20 Ω·cm) and seven copper metal layers. The two top copper layers are thicker than the others. We also designed with a SiGe 130-nm BiCMOS technology optimized for mm-wave operation [16]. Its substrate resistivity is comparable to the one observed in the CMOS. The most important difference concerning transformer design between these technologies is related to their back-ends. This BiCMOS technology presents six copper layers, including the two top layers, which are 3-μm thick; significantly thicker than its other layers and CMOS top metal layers. These metals are also placed in a higher position, so that substrate losses tend to be less expressive. The distance between top metals is greater for the BiCMOS, nevertheless, which tends to weaken magnetic coupling. Additionally, this SiGe technology allows the use of wider metal traces.

B) Modeling

The mm-wave transformers are represented by the electrical model of Fig. 2. It consists of a $2-\pi$ configuration for which the series resistances are frequency-dependent in order to account for the skin effect. The calculation of the self-inductances follows equation (1) to which the respective positive and negative mutual inductances are included. Their computation follows the procedure described in [17], and their contribution is negative for the feed lines and

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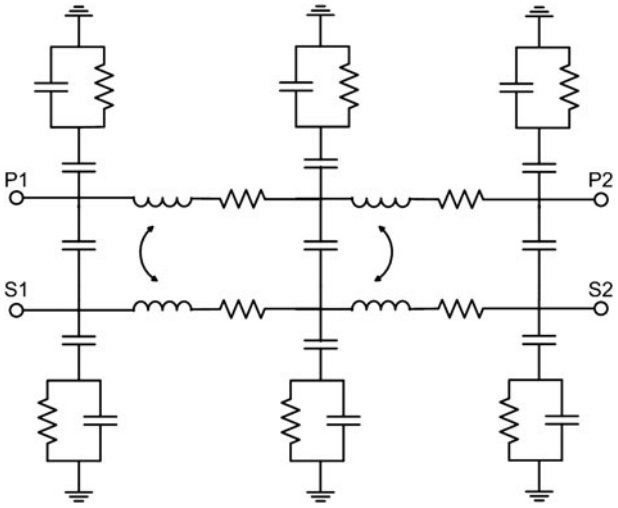

Fig. 2. Electric model of the mm-wave transformer.

opposite sides of the loop and positive for the coupling between turns in the case of a two-turn winding.

In addition to the series components, this model contains substrate branches and inter-winding coupling elements. Coupling is represented by mutual inductance and capacitance between windings whereas substrate branches contain a combination of an oxide capacitance, and silicon capacitance and resistance. As a portion of the primary is shielded from the substrate by the secondary, only their unshielded area is considered in the capacitance calculation. All elements in the model are calculated through physics-based expressions depending on their geometrical and technological factors.

C) Measurement

A 65-nm CMOS and a 130-nm BiCMOS chip including a set of transformers were fabricated in order to validate the techniques described in this paper. A micrograph of these transformers is shown in Fig. 3. The on-wafer *S*-parameter measurements of the fabricated transformers were performed using an Agilent E8361A network analyzer between 0.5 and 110 GHz. For these measurements covering the mm-wave range, a three- or four-port test bench was not available. For this reason, all the transformers were designed in a two-port configuration, grounding one terminal of each winding. De-embedding of pad and feed lines was carried out through an *open-short* procedure.

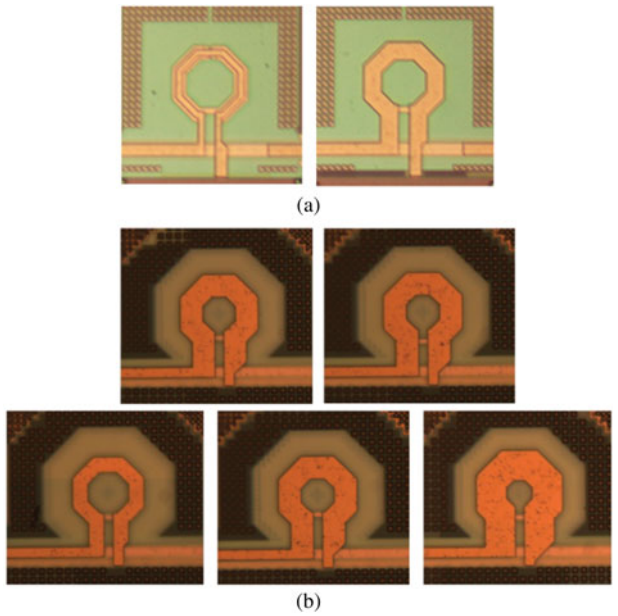

Fig. 3. Micrograph of the fabricated (a) CMOS, and (b) BiCMOS transformers.

D) Parameter extraction

The purpose of this study is to investigate the attainable inductance ratios using the proposed topology while evaluating the impact it presents on the performance measures of the transformer. Thus, we extract the inductance values from the measured impedance parameters as in (2). In order to evaluate the overall performance of the component, we choose the minimum insertion loss (IL_m) as a figure of merit, which considers simultaneously the quality factors Q_P and Q_S and coupling coefficient k of the transformer. Its value in decibels is extracted by (5) and (6), and is defined as the insertion loss of the two-port component in the best possible case, i.e., when both ports are perfectly matched. An overview of the attainable values for the minimum insertion loss found in the literature is presented in Table 1:

$$L_P = \frac{\mathrm{Im}(Z_{11})}{\omega},\ L_S = \frac{\mathrm{Im}(Z_{22})}{\omega},\ n_L = \frac{L_S}{L_P}, \tag{2}$$

$$Q_P = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})},\ Q_S = \frac{\mathrm{Im}(Z_{22})}{\mathrm{Re}(Z_{22})}, \tag{3}$$

$$k = \sqrt{\frac{\mathrm{Im}(Z_{21})^2}{\mathrm{Im}(Z_{11})\mathrm{Im}(Z_{22})}}, \tag{4}$$

$$IL_m = -10\log\left[1 + 2\left(x - \sqrt{x^2 + x}\right)\right], \tag{5}$$

$$x = \frac{\mathrm{Re}(Z_{11})\mathrm{Re}(Z_{22}) - [\mathrm{Re}(Z_{12})]^2}{[\mathrm{Im}(Z_{12})]^2 + [\mathrm{Re}(Z_{12})]^2}. \tag{6}$$

E) Different trace widths

1) CMOS MEASUREMENT

The first comparison we perform concerns the impact of presenting different trace widths for the primary and secondary. The structure of the considered CMOS transformers is shown in Fig. 4. They present the same secondary geometry consisting of a two-turn winding, with a 4-μm trace width, 1.5-μm

Table 1. Measured minimum insertion loss of integrated transformers at 60 GHz.

Ref.	Impedance transformation	IL_m (dB) (60 GHz)
[6]	No	0.9
[7]	No	0.8
[8]	Yes	1.3

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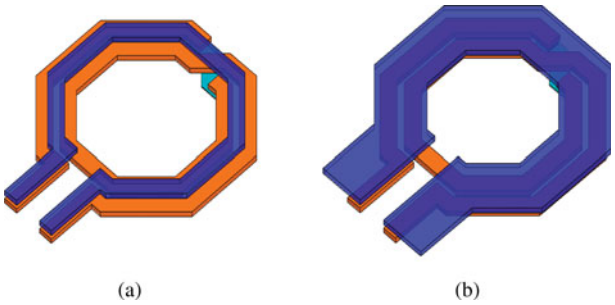

Fig. 4. 3-D view of CMOS transformers with (a) $W_P = 4$ μm, and (b) $W_P = 12$ μm.

spacing between turns, and a 42-μm average diameter. Primaries, on the other hand, present a 42-μm average diameter, so that they are centered above the secondaries. In the first case, as for a traditional design, the trace width is the same as for the secondary, i.e., 4 μm, and in the second case the primary is 12-μm wide, which corresponds to the maximum allowed width for this technology.

The measurement results of these transformers are depicted in Fig. 5. It is observed that the proposed topology allows an increase from 3.1 to 4.2 on the inductance ratio at 60 GHz, as predicted by model simulation. On the other hand, the resonant frequency of the component is reduced, due to the augmentation of its effective capacitance. Nevertheless, mostly as a result of the stronger magnetic coupling, a better minimum insertion loss is achieved. Indeed, using the proposed topology, the minimum insertion loss is reduced from 1.3 to 1 dB at 60 GHz. Thus, we observe that the use of a wider primary above the secondary not only allows a higher transformation ratio, but also a better performance at mm-waves.

2) BICMOS MEASUREMENT

In order to further evaluate this topology, we have designed three other transformers in the SiGe technology. This technology allows metal widths up to 30 μm, whereas the maximum allowed by the CMOS process is 12 μm. The secondaries of these transformers present two turns, with a 45-μm diameter, 4-μm trace width, and a 2-μm interturn spacing. Their primary diameter is equal to 45 μm, while the metal widths are, respectively, 12, 18, and 24 μm (Fig. 6).

The obtained results (Fig. 7) confirm how transformation ratios are increased as primaries are wider. Hence, the

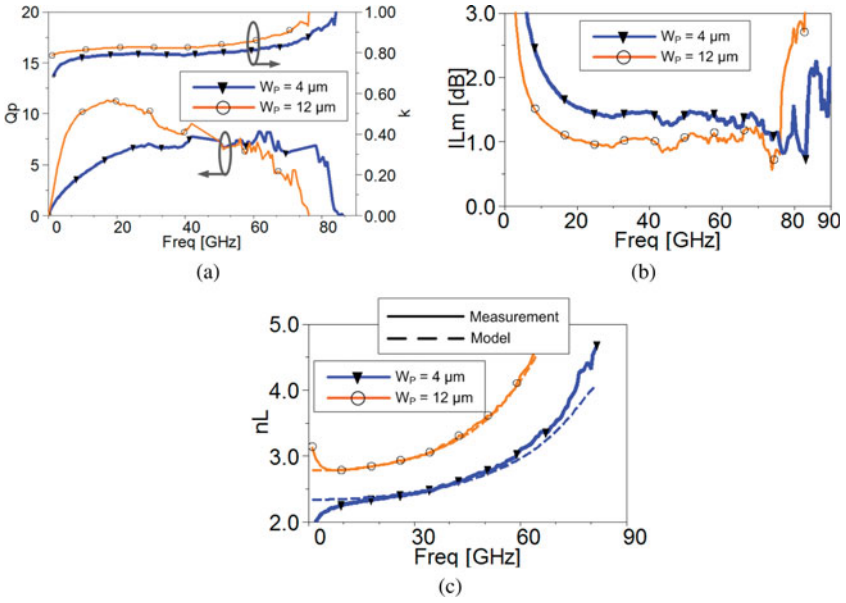

Fig. 5. (a) Primary quality factor and coupling coefficient, (b) minimum insertion loss, and (c) inductance ratio of CMOS transformers for different primary widths.

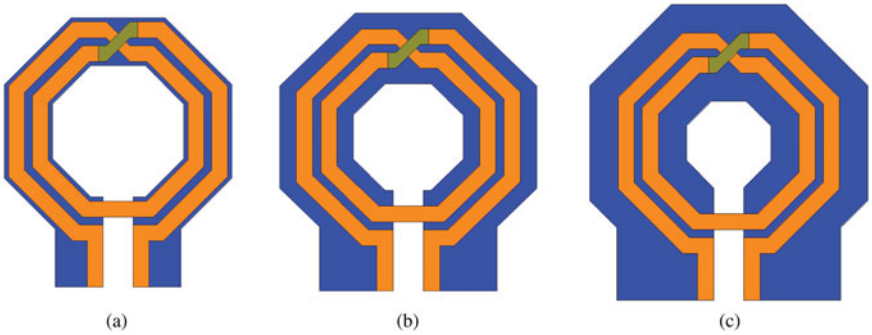

Fig. 6. Layout of BiCMOS transformers with (a) $W_P = 12$ μm, (b) $W_P = 18$ μm, and (c) $W_P = 24$ μm.

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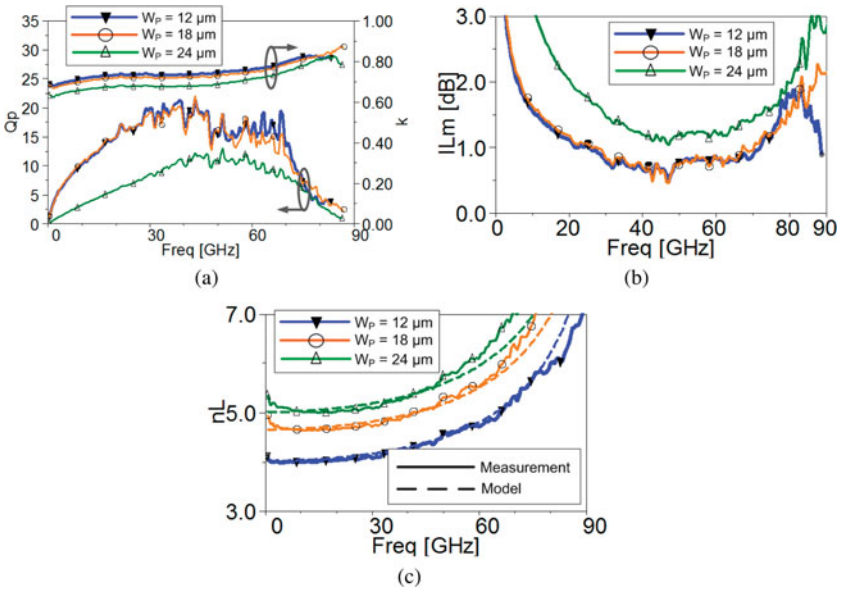

Fig. 7. (a) Primary quality factor and coupling coefficient, (b) minimum insertion loss, and (c) inductance ratio of BiCMOS transformers for different primary widths.

obtained ratios at 60 GHz are as high as 4.8, 5.5, and 6.1 for respective primary widths of 12, 18, and 24 μm. In these cases, the resonant frequency is not strongly affected. Unlike the previous observation for CMOS transformers, widening the primary traces leads to a weaker magnetic coupling. This is due to the fact that the mutual inductance between the coils depends directly on the overlapping area between primary and secondary, which in this observation becomes proportionally lower as primaries are enlarged. The performance of the 12- and 18-μm transformers is very similar in terms of coupling and quality factor, and as a consequence, minimum insertion losses are equivalent for 12- and 18-μm primaries (IL_m about 0.8 dB), and higher for the 24-μm transformer (1.2 dB). These results show that there is a limit on improving the performance of the transformers as transformation ratios are increased using the trace widths of the windings.

F) Different diameters

1) BICMOS MEASUREMENT

We have also investigated the impact of designing transformers with different average diameters on the primary and secondary. Their layouts are presented in Fig. 8. We have taken advantage of the greater widths allowed for this process, so that the primary traces of the designed transformers are 18-μm wide. The primary diameter D_P is 45 μm, secondary trace width is 4 μm, and secondary inter-turn spacing is 2 μm. The first transformer presents both primary and secondary with the same inner diameter ($D_S = 37$ μm), for the second one the secondary is perfectly centered under the primary ($D_S = 45$ μm), and for the third one outer diameters coincide ($D_S = 53$ μm).

Measured results are shown in Fig. 9. As expected, it is observed that greater diameters provide higher secondary inductances and hence higher transformation ratios. At 60 GHz, the inductance ratio is equal to 4 for the coincident inner diameters, 5.5 for the average diameters, and 7 for outer diameters. As it is observed that geometries presenting better coupling provide lower quality factors, we notice an equivalent minimum insertion loss in the three cases (IL_m around 0.8 dB), when sufficiently distant from their resonant frequencies. It is moreover observed that resonant frequencies are lower for greater secondary diameters due to the increased equivalent capacitance to the substrate.

These results prove that, for the metal width range allowed for this BiCMOS technology, it is possible to achieve a substantial increment on the inductance ratio by defining the relative diameter of the secondary under the primary without impacting on its losses.

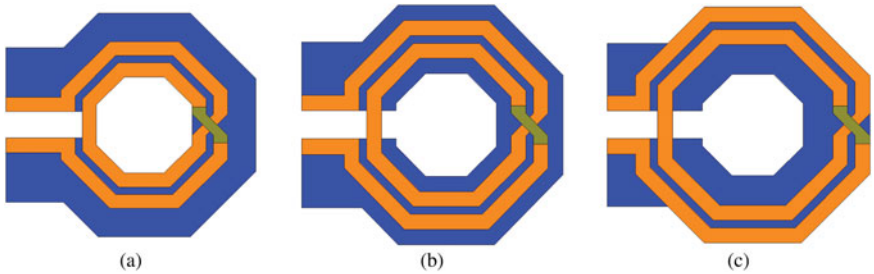

Fig. 8. Layout of BiCMOS transformers with (a) $D_S = 37$ μm ($D_{Sin} = D_{Pin}$), (b) $D_S = 45$ μm ($D_S = D_P$), and (c) $D_S = 53$ μm ($D_{Sout} = D_{Pout}$).

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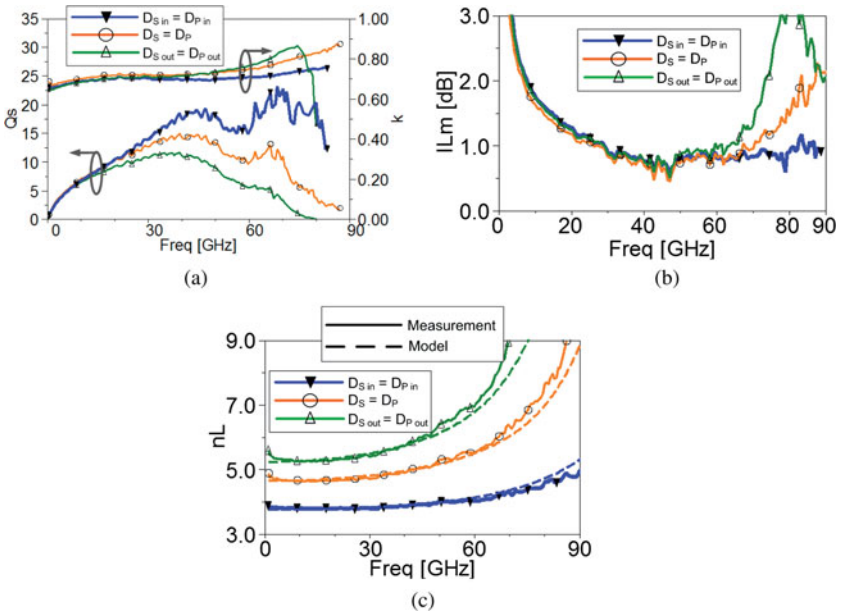

Fig. 9. (a) Secondary quality factor and coupling coefficient, (b) minimum insertion loss, and (c) inductance ratio of BiCMOS transformers for different secondary diameters.

IV. CONCLUSION

A novel layout topology to design transformers with high transformation ratios and compatible with mm-wave constraints was presented. This topology consists of defining different trace widths and different diameters for the stacked primaries and secondaries of the transformers. Experimental results of STMicroelectronics 65-nm CMOS and 130-nm SiGe BiCMOS components have been presented in order to support this study. The proposed electric model was shown to supply an accurate representation of the transformers' inductances. The obtained results proved the proposed transformers effective at providing higher inductance ratios than traditional topologies while reducing insertion losses, which are as low as state-of-the-art 1:1 transformers. Indeed, inductance transformation ratios as high as 7 at 60 GHz have been reported in our investigation. Such designs are simple to implement and constitute an interesting alternative to take advantage of the transformer properties to integrate matching networks within wireless communication-integrated circuits. Future developments could include investigating the impact of metal slotting in order to extend the achievable width ranges as well as differential characterization of the transformers.

REFERENCES

[1] Niknejad, A.M.; Meyer, R.G.: Analysis, design, and optimization of spiral inductors and transformers for Si RFIC's. IEEE J. Solid-State Circuits, **33** (10) (1998), 1470–1481.

[2] Long, J.R.: Monolithic transformers for silicon RF IC design. IEEE J. Solid-State Circuits, **35–39** (2000), 1368–1382.

[3] Ng, K.T.; Rejaei, B.; Burghartz, J.N.: Substrate effects in monolithic RF transformers on silicon. IEEE Trans. Microw. Theory Tech., **50** (1) (2002), 377–383.

[4] El-Gharniti, O.; Kerherve, E.; Begueret, J.B.: Modeling and characterization of on-chip transformers for Silicon RFIC. IEEE Trans. Microw. Theory Tech., **55** (4) (2007), 607–615.

[5] Dickson, T.O.; LaCroix, M.A.; Boret, S.; Gloria, D.; Beerkens, R.; Voinigescu, S.P.: 30–100-GHz inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits. IEEE Trans. Microw. Theory Tech., **53** (1) (2005), 123–133.

[6] Chowdhury, D.; Reynaert, P.; Niknejad, A.M.: Design considerations for 60 GHz transformer-couple CMOS power amplifiers. IEEE J. Solid-State Circuits, **44** (10) (2009), 2733–2744.

[7] Chen, C.-Z.; Lin, Y.-S.; Chen, C.-C.; Yeh, P.-F.; Chang, J.-F.: High-coupling and ultra-low-loss interlaced stacked transformers for 60–100 GHz CMOS RFIC applications, in IEEE Radio and Wireless Symp., Orlando, FL, USA, 2007.

[8] LaRocca, T.; Liu, J.Y.-C.; Chang, M.-C.F.: 60 GHz CMOS amplifiers using transformer-coupling and artificial dielectric differential transmission lines for compact design. IEEE J. Solid-State Circuits, **44** (5) (2009), 1425–1435.

[9] Rotella, F.M.; Cismaru, C.; Tkachenko, Y.G.; Cheng, Y.; Zampardi, P.J.: Characterization, design, model validation of silicon on-wafer M:N balun components under matched and unmatched conditions. IEEE J. Solid-State Circuits, **41** (5) (2006), 1201–1209.

[10] Lim, C.C. et al.: An area efficient high turn ratio monolithic transformer for silicon RFIC, in IEEE Radio Frequency Integrated Circuits Symp., Atlanta, GA, USA, 2008.

[11] Chan, W.L.; Long, J.R.; Spirito, M.; Pekarik, J.J.: A 60 GHz-Band 1 V 11.5 dBm power amplifier with 11% PAE in 65 nm CMOS, in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, San Francisco, CA, USA, 2009.

[12] Cheung, T.S.D.; Long, J.R.: Design and modeling of mm-wave monolithic transformers, in IEEE Bipolar/BiCMOS Circuits and Technology Meeting, Maastricht, Netherlands, 2006.

[13] Belot, D.; Leite, B.; Kerhervé, E.; Bégueret, J.-B.: Millimeter-wave transformer with a high transformation factor and a low insertion loss, U.S. Patent Application 12/787,782, May 26, 2010.

https://doi.org/10.1017/S1759078711001073 Published online by Cambridge University Press

[14] Leite, B.; Kerhervé, E.; Bégueret, J.-B.; Belot, D.: Shielding structures for millimeter-wave integrated transformers, in 16th IEEE Int. Conf. Electronics, Circuits and Systems, Yasmine-Hammamet, Tunisia, 2009.

[15] Grover, F.W.: Inductance Calculations, *Van Nostrand*, Princeton, NJ, 1946.

[16] Avenier, G. et al.: 0.13 μm SiGe BiCMOS technology fully dedicated to mm-wave applications. IEEE J. Solid-State Circuits, **44** (9) (2009), 2312–2321.

[17] Unterweissacher, M.; Brandtner, T.; Pribyl, W.: Inductance formulas adapted for direct use in Spice simulators. IET Electron. Lett., **44** (2) (2008), 92–93.

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