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Nonlinear modeling of InP devices for W-band applications

DAVIDE RESCA[1], VALERIA DI GIACOMO[2], ANTONIO RAFFO[2], RAFAEL CIGNANI[1], ALBERTO SANTARELLI[1], GIORGIO VANNINI[2], FABIO FILICORI[1], DOMINIQUE SCHREURS[3], FARID MEDJDOUB[4], NICOLAS THOUVENIN[5] AND CHRISTOPHE GAQUIÈRE[5]

A recently proposed technique for the distributed modeling of extrinsic parasitic effects in electron devices is used for the very first time in conjunction with a lumped equivalent circuit model for the intrinsic device.

Nonlinear modeling of 0.1 μm InP HEMTs for W-band applications is considered here, leading to extremely accurate predictions of harmonic distortion and power added efficiency at the fundamental frequencies of 27 and 94 GHz.

The distributed parasitic network is identified through accurate electromagnetic simulations up to the upper frequency limit of the millimeter-wave band (300 GHz), while standard pulsed I/V and S-parameter measurements up to 67 GHz are used for the identification of the intrinsic device model.

Keywords: Semiconductor device modeling, Field-effect transistors (FETs), Electromagnetic analysis, Semiconductor device measurements

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I. INTRODUCTION

Many applications have recently emerged in the W-band, such as automotive collision-prevention systems, communication satellites, radiometry, and radio-astronomy systems.

These and other applications require electron devices capable of operation at very high frequencies. InP-based HEMTs represent a typical example of devices with operation capability at W-band. In fact, they have been successfully employed for both low-noise and high-power applications at these frequencies [1–3]. InP-based devices exhibit higher gain, higher cutoff frequency, lower source resistance, higher maximum current densities, and higher substrate thermal conductivity compared to similar transistors based on GaAs technology [4, 5].

Accurate small- and large-signal characterizations and modeling are thus required in this frequency range for the optimal design of W-band system components [6, 7]. Unfortunately, the frequency limits of the measurement instrumentation lead to the need for nonlinear models that are also capable of good extrapolations of the electrical characteristics with respect to the identification frequency range. For instance, the accurate prediction of device behavior under strong nonlinear operation at 94 GHz, besides requiring very good prediction capability at the fundamental frequency (which, in the present case, lies in the extrapolation region), also depends on a reasonable (at least physical) behavior at the second and third harmonics (188 and 282 GHz, respectively).

From this point of view, the intrinsic device model should guarantee physical frequency extrapolations of differential parameters. Classic equivalent circuit models [8–12] tend to respect this constraint, and therefore are a potentially good candidate for accurate predictions at extremely high frequencies.

However, the prediction accuracy in this range of frequencies also strongly depends on the modeling of the extrinsic parasitic network, since distributed effects and coupling phenomena may strongly affect the transistor performance. Such a behavior is not easily described by standard lumped parasitic elements identified through optimization-based [13–15] or direct extraction techniques [16–19]. Either distributed effects should be taken into account in the device model or rather complicated structures have to be considered [20–24].

In this paper, a distributed parasitic network description based on electromagnetic (EM) simulation is adopted and used in conjunction with a classical nonlinear equivalent circuit approach in order to model a 0.1 μm InP HEMT for W-band applications. The distributed modeling of the extrinsic parasitic network is described in section II, together with the identification procedure of the intrinsic equivalent-circuit model. The model, identified on the basis of EM simulations, pulsed I/V characteristics, and small-signal S-parameter measurements up to 67 GHz, is then validated in section III.

[1]Department of Electronics Information and Systems, The University of Bologna, Viale C. Pepoli 3/2, 40123 Bologna, Italy, Emails: davide.resca3@unibo.it, alberto.santarelli@unibo.it, rafael.cignani@unibo.it, ffilicori@deis.unibo.it

[2]Department of Electronics, The University of Ferrara, Via Saragat 1, 44100 Ferrara, Italy, Emails: antonio.raffo@unife.it, valeria.digiacomo@unife.it, giorgio.vannini@unife.it

[3]Katholieke Universiteit Leuven, The Electronic Engineering Department, B-3001 Leuven, Belgium, Email: dominique.schreurs@esat.kuleuven.be

[4]Department of Electron Devices and Circuits, The University of Ulm, Albert-Einstein-Allee 45, 89081 Ulm, Germany, Email: farid.medjdoub@uni-ulm.de

[5]The I.E.M.N/III V lab/TIGER, U.M.R.-C.N.R.S. 8520, U.S.T.L., Avenue Poincaré, B.P. 69, 59652 Villeneuve D'Ascq Cedex, France, Emails: christophe.gaquiere@iemn.univ-lille1.fr, nicolas.thouvenin@ed.univ-lille1.fr.

Corresponding author:
D. Resca
Email: davide.resca3@unibo.it

Small-signal extrapolation up to 300 GHz and experimental validation under large-signal operation at 27 and 94 GHz fully outline the model prediction capabilities.

II. INP DEVICE MODELING

The modeled device is a 0.1 μm InP HEMT having a total gate width of 80 μm (two gate fingers). It exhibits state-of-the-art performances, thanks to the large band-gap InP channel associated with the optimized gate recess process on the composite barrier. Details on the device process and fabrication are reported in [5], while the device layout, which is in coplanar waveguide technology, is shown in Fig. 1.

The approaches adopted for the identification of the extrinsic parasitic network as well as for the intrinsic device modeling are described in the following.

A) Compact distributed modeling of the extrinsic parasitic network

To accurately model all the possible parasitic effects that may occur at W-band frequencies, a distributed approach is adopted here for the extraction of the extrinsic parasitic network, instead of identifying conventional topologies based on lumped elements.

The distributed description of the parasitic network is obtained through accurate EM simulation of the device passive structure shown in Fig. 1.

According to [20–23], the active region of the electron device is partitioned in two elementary intrinsic devices (EIDs), each of them placed in the middle of the gate fingers. Access points for the EIDs are defined in the EM simulation by using the *internal ports* provided by commercial software [25, 26].

The EM simulation results in a six-port network, characterized by an admittance matrix $\mathbf{Y}_{EM}$ [6 × 6]. Such a network accounts for parasitic effects due to the gate and drain accesses to the active area, for those along the device fingers and for possible transverse couplings between fingers. A schematic representation of this six-port parasitic description is shown in Fig. 1, where V_1, V_2, I_1, and I_2 are the phasors of extrinsic gate-source and drain-source voltages and extrinsic gate and drain currents, respectively. Analogously, V_3, V_4, V_5, V_6, I_3, I_4, I_5, and I_6 are the phasors of the EID voltages and currents defined according to Fig. 1.

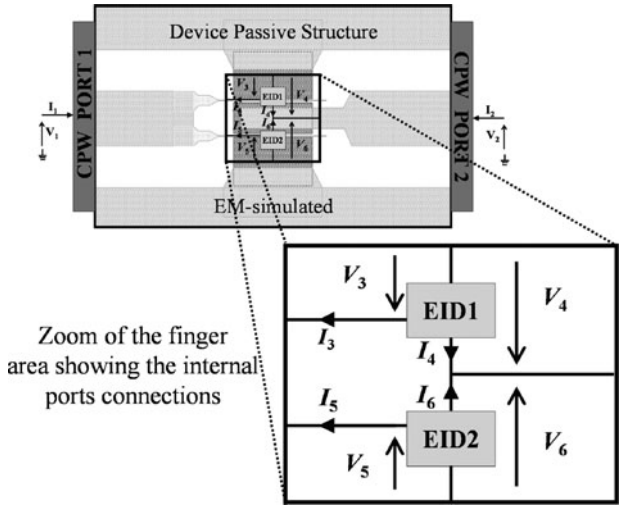

Fig. 1. Layout of the 2 × 40 μm InP HEMT (L = 0.1 μm). The set-up of the EM simulation is also shown. The extrinsic ports are defined for the CPW modes excitation. Internal ports are used for the definition of the two EIDs.

The distributed six-port parasitic network shown in Fig. 1 is adopted in [20, 21] for a fully distributed model of the extrinsic parasitic effects, suitable for scalable linear device modeling. Instead, an approach for the more general nonlinear case is proposed in [22]. According to this procedure, a single equivalent intrinsic device (EqID) is introduced in order to limit the computational cost during harmonic-balance-based circuit analyses, otherwise extremely high when adopting purely distributed "sliced" models [20, 21]. The approach [22] leads to the definition of a compact but still distributed four-port parasitic network, described by an admittance matrix $\mathbf{Y}_C$ [4 × 4]. This can be obtained by considering any EID equal to each other (both from the geometrical and electrical points of view) and equally excited. The second hypothesis means that both attenuation and delay of signals traveling across the fingers are assumed to be negligible. This is quite reasonable in "well-designed" medium power devices, since either non-uniform current densities along the fingers or out-of-phase current combinations from different device fingers would correspond to sub-optimal device performance.

The hypothesis of "equally excited EIDs" can be relaxed by introducing a multi-bias iterative procedure as shown in [23], but the upper frequency limit of the identified compact distributed parasitic network is restricted by the maximum frequency ratings of the adopted measurement system.

In the case of the InP device-under-test, we use the simpler approach [22] for two reasons. First, owing to the symmetry of the two-finger device, the same excitation is actually applied to EID1 and EID2. Second, the EM simulation can be extended at the upper mm-wave frequency limit (300 GHz), in order to achieve better frequency extrapolation capabilities of the final model.

By adopting the layout set-up shown in Fig. 1, the EM simulation of the device passive structure is performed in the frequency range from DC to 300 GHz. Because of the planar structure of the device, a commercial 3D planar EM simulator, such as [25, 26], is the best trade-off between accuracy and simulation time.

According to [22], the six-port distributed parasitic network in Fig. 1 (represented by the $\mathbf{Y}_{EM}$ matrix) is compacted into a four-port description of parasitic effects, by imposing

$$\begin{array}{ll} \mathrm{V}_1 \doteq V_1 & \mathrm{I}_1 \doteq I_1 \\ \mathrm{V}_2 \doteq V_2 & \mathrm{I}_2 \doteq I_2 \\ \mathrm{V}_3 \doteq V_3 = V_5 & \mathrm{I}_3/N \doteq I_3 = I_5 \\ \mathrm{V}_4 \doteq V_4 = V_6 & \mathrm{I}_4/N \doteq I_4 = I_6 \end{array}, \qquad (1)$$

where V_j, I_j ($j = 1, \ldots, 4$) are the phasors of voltages and currents at the ports of the yet-unknown compact parasitic network (see Fig. 2).

The admittance matrix $\mathbf{Y}_C$ of the compact distributed parasitic network can be evaluated on the basis of (1) after simple

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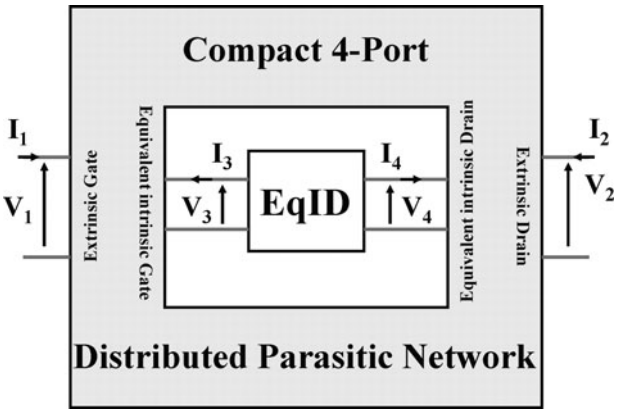

Fig. 2. Electron device model composed of the single, EqID and the compact four-port distributed parasitic network directly identified from the electromagnetic simulation through (2).

algebraic manipulation, through

$$\mathbf{Y}_C = \begin{pmatrix} y_{11} & y_{12} & y_{13}+y_{15} & y_{14}+y_{16} \\ y_{21} & y_{22} & y_{23}+y_{25} & y_{24}+y_{26} \\ y_{31}+y_{51} & y_{32}+y_{52} & y_{33}+y_{35}+ \\ & & +y_{53}+y_{55} & y_{34}+y_{36}+ \\ & & & +y_{54}+y_{56} \\ y_{41}+y_{61} & y_{42}+y_{62} & y_{43}+y_{45}+ & y_{44}+y_{46}+ \\ & & +y_{63}+y_{65} & +y_{64}+y_{66} \end{pmatrix}, \quad (2)$$

where y_{ij} $(i, j = 1, \ldots, 2N + 2)$ are the elements of the $\mathbf{Y}_{EM}$ matrix.

The adopted distributed description of the device parasitic network is intrinsically fashioned for HB-based circuit simulators, thus convergence problems may occur when time-domain simulations are involved. However, either compact lumped network synthesis techniques [27] or EM-based lumped extrinsic parasitics identification procedures [28] can be adopted in order to obtain a model fully compatible with time-domain analysis.

B) Intrinsic device modeling

The conventional nonlinear model of the intrinsic device shown in Fig. 3 is extracted. To this aim, standard pulsed *I*/*V* measurements are carried out in order to characterize the low-frequency *I*/*V* behavior. Negligible thermal self-heating effects and negligible dependence on quiescent conditions are observed among different pulsed *I*/*V* curve sets.

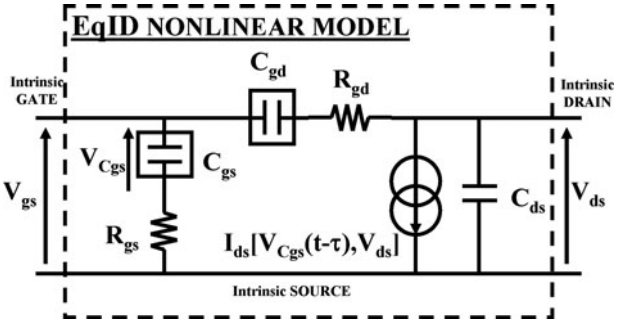

Fig. 3. Intrinsic device nonlinear model adopted for the EqID.

Thus, a single look-up-table-based *I*/*V* characteristic, pulsed from the nominal quiescent condition ($V_{go} = -0.3$ V; $V_{do} = 2$ V), is used for the modeling of the nonlinear drain current source I_{ds}.

Further device characterization is carried out by means of standard CW *S*-parameter measurements in the frequency range (0.5–67 GHz), over a dense bias grid ($V_{go} = -0.8$–0 V, step 50 mV; $V_{do} = 0$–3 V, step 100 mV). Multi-frequency closed-form de-embedding of the small-signal measurements from the parasitic network (2) directly leads to the multi-bias, multi-frequency linear model of the EqID of Fig. 2.

The bias-dependent gate-source and gate-drain capacitances, C_{gs} and C_{gd}, are obtained through a linear regression of the imaginary parts of the multi-bias intrinsic *Y*-parameters at relatively low frequency (0.5–10 GHz) [29].

All the nonlinear elements are nonlinearly controlled by the voltage drop across the gate-source capacitance, V_{Cgs} and the intrinsic drain-source voltage, V_{ds}. The nonlinear capacitive elements are also implemented as look-up table-based components.

The remaining bias-independent elements C_{ds}, R_{gs}, R_{dg}, and τ are extracted by means of optimization procedures based on the best fit of the measured intrinsic *Y*-parameters at the nominal bias voltages ($V_{go} = -0.3$ V; $V_{do} = 2$ V). In particular, C_{ds} is obtained from the fitting of the imaginary part of Y_{22} in the frequency range 0.5–10 GHz corresponding to an almost quasi-static behavior, while R_{gs}, R_{gd}, and τ are obtained from the fitting up to 67 GHz.

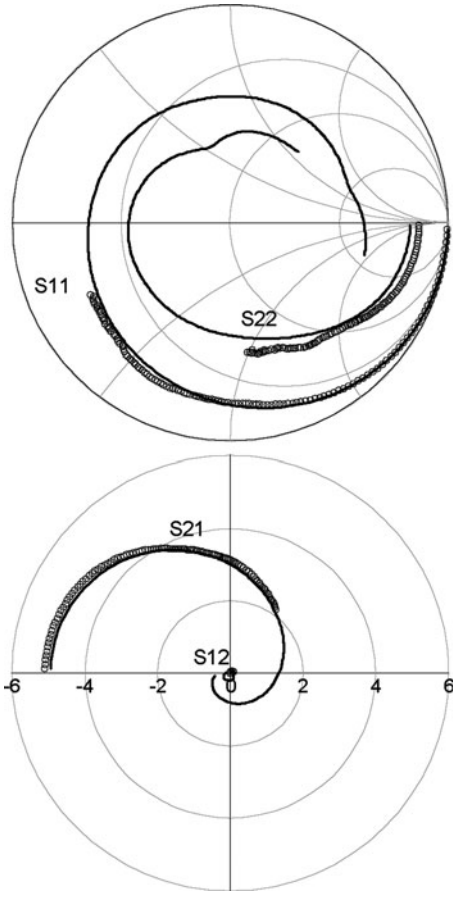

Fig. 4. Extrinsic *S* parameters at $V_{go} = -0.3$ V and $V_{do} = 2$ V. Measurements (circles) are up to 67 GHz, while model predictions (line) are extended up to 300 GHz.

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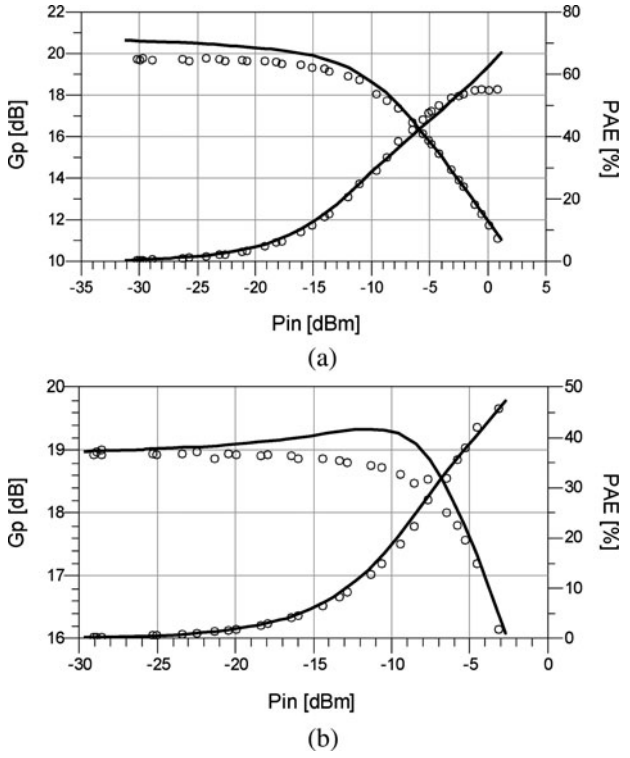

Fig. 5. Power gain and PAE measured at 27 GHz (circles). The model predictions are marked by solid lines. (a) $V_{go} = -0.3$, $V_{do} = 2$, $\Gamma_L = 0.33 + j \times 0.304$ and (b) $V_{go} = -0.3$, $V_{do} = 3$, $\Gamma_L = 0.47 + j \times 0.34$.

III. SMALL- AND LARGE-SIGNAL MODEL VALIDATION

The extrinsic *S*-parameters evaluated at the nominal bias point ($V_{go} = -0.3$ V; $V_{do} = 2$ V) are compared with measurements up to 67 GHz in Fig. 4. However, the model predictions are here extended up to 300 GHz, in order to outline the device behavior under frequency-extrapolated conditions. The combination of an almost resistive intrinsic device (due to the equivalent circuit approach) along with the physically consistent distributed description of the extrinsic parasitic network guarantees a quite regular and reasonably expected device behavior, even at the higher frequencies considered.

The model is further validated under large signal operation by means of two different set-ups.

First, active load-pull measurements are carried out at 27 GHz, at different quiescent conditions and by adopting near-optimal load impedances for maximum output power. A standard 50 Ω source impedance is used at the input port.

Model predictions of power gain and power added efficiency (PAE) versus input power are reported in Fig. 5 at two different bias and loading conditions.

Finally, an innovative set-up for power measurements at 94 GHz is used in order to complete the model validation [7]. This set-up consists of a diode IMPATT oscillator with a nominal power of about 300 mW at 94 GHz (used as microwave power source), a mechanical tuner to match the device output, and three power-meters, which acquire the injected/reflected power at the input and output device ports. Harmonic distortion measurements are carried out at two different bias points and with two different loading

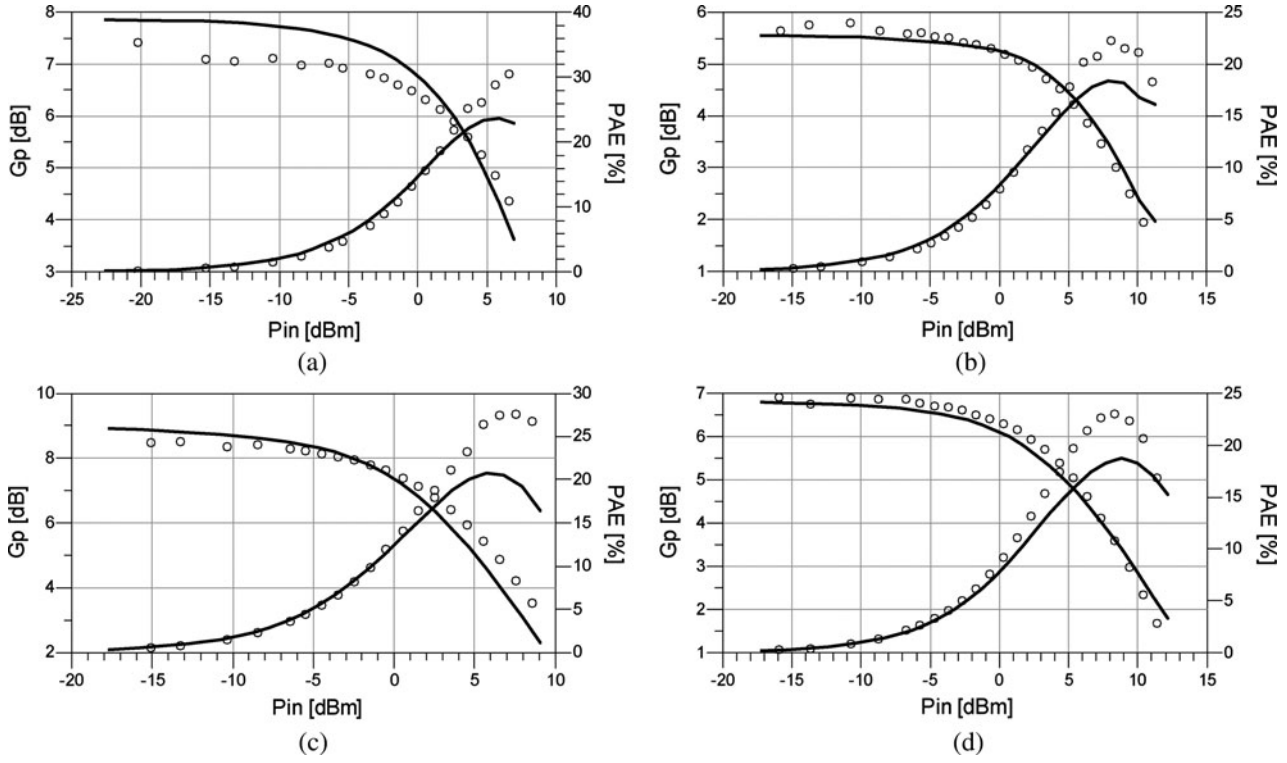

Fig. 6 Predicted Gp and PAE at 94 GHz (solid lines) compared with measurements (circles). (a) $V_{go} = -0.3$, $V_{do} = 2$, $\Gamma_L = -0.057 + j \times 0.53$, (b) $V_{go} = -0.3$, $V_{do} = 2$, $\Gamma_L = -0.108 - j \times 0.17$, (c) $V_{go} = -0.2$, $V_{do} = 2$, $\Gamma_L = -0.057 + j \times 0.53$, and (d) $V_{go} = -0.2$, $V_{do} = 2$, $\Gamma_L = -0.108 - j \times 0.17$.

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impedances, both selected near the optimal matching condition for maximum output power.

Model predictions of power gain and PAE are compared with measurements in Fig. 6. The accurate identification and the consistent frequency extrapolation of the distributed parasitic network play for sure an important role in obtaining the good agreement achieved.

IV. CONCLUSION

A 0.1 μm InP HEMT for W-band applications is characterized and modeled. To this aim, an EM-simulation-based distributed description of the extrinsic parasitic network is adopted in conjunction with a classic nonlinear equivalent circuit approach for the intrinsic device.

Even though the identification is carried out on the basis of small-signal *S*-parameters up to 67 GHz only, the model provides very accurate harmonic distortion predictions at 94 GHz, mainly due to the physically consistent frequency extrapolation guaranteed by the distributed parasitic network.

The obtained results prove that this model can be reliably adopted in operations, where strong frequency extrapolation is required.

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Davide Resca was born in Bologna, Italy, in 1979. He received the Laurea degree in electronic engineering in 2004 from the University of Ferrara. Since then he has been with the Department of Electronics, Computer Science and Systems (DEIS – University of Bologna), where he received a Ph.D. degree in electronic computer science and communication systems in 2008. His research activity is mainly oriented to linear and nonlinear device modeling and circuit design techniques for nonlinear micro- and millimeter-wave applications.

Valeria Di Giacomo was born in Salerno, Italy. She received the Laurea degree in electronic engineering from the University of Bologna, Italy, in 2005. Since then, she has collaborated with the Department of Electronics of the same university, and in 2006 she joined the Engineering Department of the University of Ferrara as a Ph.D. student. Her research activity is mainly oriented to nonlinear electron device modeling for microwave applications.

Antonio Raffo was born in Taranto, Italy, in 1976. He received an M.S. degree (with honors) in electronic engineering and a Ph.D. degree in information engineering from the University of Ferrara, Ferrara, Italy, in 2002 and 2005, respectively.

Since 2002, he has been with the Electronic Department, University of Ferrara, Italy, where he is currently a Contract Professor of Electronic Instrumentation and Measurement.

His research activity is mainly oriented to nonlinear electron device characterization and modeling and circuit-design techniques for nonlinear microwave and millimeter-wave applications.

Dr. Raffo is a member of the Italian Association on Electrical and Electronic Measurements.

Rafael Cignani was born in Ravenna, Italy, in 1975. He received the Laurea degree in telecommunications engineering in 2000 from the University of Bologna. During his Ph.D. studies, he has collaborated with the Department of Electronics, Computer Science, and Systems (DEIS – University of Bologna). In 2004, he received a Ph.D. degree in information engineering from the University of Ferrara. He is currently a Graduated Technician in the Laboratory of Electronics for Communications (DEIS – University of Bologna). His research activity is mainly oriented to MMIC design and nonlinear circuit modeling, and design techniques.

Alberto Santarelli received the Laurea degree in electronic engineering in 1991 and a Ph.D. in electronics and computer science from the University of Bologna, Italy, in 1996. He was a Research Assistant from 1996 to 2001 with the Research Center for Computer Science and Communication Systems of the Italian National Research Council in Bologna. In 2001 he joined the Department of Electronics, Computer Science, and Systems (DEIS – University of Bologna), where he currently is an Associate Professor. His main research interests are electron device nonlinear modeling and circuit design for microwave applications.

Giorgio Vannini received the Laurea degree in electronic engineering and a Ph.D. degree in electronic and computer science engineering, from the University of Bologna, Bologna, Italy, in 1987 and 1992, respectively. He joined the Department of Electronics of the University of Bologna as a Research Associate in 1992. From 1994 to 1998, he has also been with CSITE, Bologna (Research Centre on Electronics, Computer Science and Telecommunication Engineering, National Research Council), where he has been responsible for the MMIC testing and CAD laboratory. In 1998, he joined the University of Ferrara as an Associate Professor and since 2005 as a Full Professor of Electronics. Currently, he is Head of the Engineering Department. During his academic career he has been a Teacher of applied electronics, electronics for communications, and industrial electronics. He has co-authored over 160 papers devoted to electron device modeling, computer-aided design techniques for MMICs, and nonlinear circuit analysis and design. He was the recipient of the best-paper awards at the 25th European Microwave Conference, GAAS98 and GAAS2001 conferences. Giorgio Vannini is a member of GAAS (Gallium Arsenide Application Symposium) association and IEEE.

Fabio Filicori received the Dr. Ing. degree in electronic engineering in 1974 from the University of Bologna, where he joined the Faculty of Engineering as Assistant Researcher and later as Associate Professor. In 1990, he became Full Professor of Electronics at the University of Perugia. In 1991, he moved to the University of Ferrara, where he was coordinator of the degree course in electronic engineering. Currently, he is Full Professor at the University of Bologna,

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where he has been coordinator of the Ph.D. course in Electronics, Computer Science, and Telecommunications. He has been the coordinator of research projects in electronic engineering promoted by the Ministry of University and Research. In 2007, he was appointed member of the Technology Commission of the Italian Space Agency. He has been workpackage leader for the European NoE TARGET. He has been TPC chairman for the EUMIC Conference and editorial board member for MTT Transactions. He is the author of about 200 papers concerning his research in nonlinear microwave circuit design, electron device modeling, electronic measurements, and industrial electronics.

Dominique Schreurs received an M.Sc. degree in electronic engineering and a Ph.D. degree from the Katholieke Universiteit (K.U.) Leuven, Belgium. She is currently associate professor at K.U. Leuven. She has been a visiting scientist at Agilent Technologies, ETH Zürich, and NIST. Her main research interests concern the (non-)linear characterization and modeling of active microwave devices, and (non-) linear hybrid and integrated circuit design. D. Schreurs is senior member of IEEE and chair of the IEEE MTT-11 technical committee on microwave measurements. She was Steering Committee member of the Network of Excellence TARGET. She also serves as Education Chair on the Executive Committee of the ARFTG organization, and was General Chair of the 2007 Spring ARFTG Conference. She is co-chair of the 2008 EuMC and Workshop Coordinator of the 2008 EuMW.

Farid Medjdoub was born in Valenciennes, France, in 1977. He received the M.S. and Ph.D. degrees from the Institut d'Electronique de Microélectronique et de Nanotechnologie (IEMN), University of Lille, Lille, France, in 2001 and 2004, respectively. His research interests concern the conception and the realization of FETs for power amplification at W band. Currently, he works on GaN-based HEMT devices at the IMEC company.

Nicolas Thouvenin was born in Neufchâteau, France. He received the engineering degree from the Ensicaen of Caen, France and the master's degree from the University of Rouen, in 2006. He is currently a Ph.D. student at the Power Department of the IEMN Laboratory of Lille. His research activity is oriented to device characterization and the design of high-bandwidth GaN mixers.

Christophe Gaquière was born in Bailleul, France, in 1966. He received a Ph.D. degree in electronics from the University of Lille in 1995. He is currently Professor at the University of Lille (Polytech'Lille), and carries out research activity at the Institut d'Electronic de Microélectronique et de Nanotechnology (IEMN). His research topics include design, fabrication, and characterization of HEMT' devices. He works on GaAs, InP, metamorphic HEMTs and is now involved in GaN activities. His main activities are microwave characterizations (small and large signals between 1 and 220 GHz) in order to correlate microwave performances with technological and topology parameters. Christophe Gaquière is the author and co-author of more than 40 publications and 100 publications, respectively; he refereed research projects and review papers in four international journals. He has several collaborations with Russia, Germany, Italia, Tunisia, Austria, GB in the frame of contracts. He is responsible for the microwave characterization part of the common laboratory between Thales TRT and IEMN focus on wide band gap semiconductor (GaN, SiC, and diamond). Christophe Gaquière is also the contact for IEMN of the network of excellence (TARGET) focus on the power devices characterization themes (240 persons, 17 countries).

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