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INDUSTRIAL AND ENGINEERING PAPER

A high-power solid state amplifier for Galileo satellite system exploiting European GaN technology

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This paper describes the development of an L-Band ($f_o = 1.575$ GHz) high power and efficient solid state power amplifier (SSPA) designed for the European satellite navigation system (i.e. Galileo). The amplifier, developed in the framework of the European Project named SLOGAN, exploits the GH50-10 GaN technology available at United Monolithic Semiconductor foundry. The aim of the project is to offer, using as much as possible European technologies, a valid alternative to replace traveling wave tube amplifiers with more compact and reliable systems. All the SSPA functionalities, i.e. power supply, power conditioning and radio frequency amplification, are integrated in the developed architecture and accommodated in a single box with limited volume and mass. The required output power level is achieved by parallelizing several GaN die power bars of 12 and/or 25.6 mm. In continuous wave operating mode, the overall SSPA delivers an output power higher than 250 W at less than 2 dB of gain compression in the whole E1-band. Moreover, the registered gain and efficiency are higher than 67 dB and 54%, respectively.

Keywords: Solid state power amplifier, Galileo Satellite, GaN, Space qualified

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I. INTRODUCTION

Nowadays, satellite infrastructures are widely employed to supply a large variety of both civil and military services. The former span from digital video broadcasting to navigation and localization, passing through weather forecast and phone communications. The latter are mostly conceived for safety, intelligence gathering, and early warming operations. Thus, independently from their final use, satellite systems are more and more essential in our everyday life.

The realization of a satellite is always a challenge due to the unique characteristics of the environment in which it has to operate. Besides the harsh surroundings, requirements like the long-time mission, typically more than 12 years, and the awareness that redundancy is the only way to do hardware replacement, pose severe constraints for the employed electronic systems. In fact, the payload of a satellite is exposed to severe radiations and sharp temperature variations that can easily affect the performance of the electronic circuitry. Therefore, robustness and reliability of the embedded mechanical, electronic, and software systems are key features to guarantee high performance till the end of the mission. Furthermore, due to the high cost per kilogram of the payload, volume and mass of every space-borne equipment have to be reduced as much as possible to maximize the trade-off between cost and benefits of the mission. Additionally, since the available energy in a spacecraft is limited, due to the restricted number of solar panels and batteries, also the efficiency of every subsystem becomes a key feature. Therefore, the design of space-borne components is usually the result of a compromise among many aspects [1].

In a satellite payload, one of the most demanding equipment in terms of power consumption, mass, size, thermal, and mechanical management is the high-power amplifier (HPA). Essentially, space-borne HPAs can be categorized into two main families: either solid-state power amplifiers (SSPAs) or traveling wave tube amplifiers (TWTAs). Besides historical reasons, the latter are used in most of the already in-orbit satellites, also thanks to their relevant capabilities in terms of output power and efficiency, especially for high-frequency applications up to Ka-band and beyond [2].

However, drawbacks such as: the need of very high dc voltages, the large volume, especially in the lower frequency bands, and the expensive realization processes required to avoid multipaction and corona effects, are pushing the research and industrial communities toward the investigation of different solutions. On this way, the development of wide band-gap semiconductor materials, such as gallium nitride (GaN) and GaN-based alloys, offers today the ability to

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manufacture radio frequency (RF) active devices with significant improved output power performance. In fact, single power bars based on high-electron-mobility transistor (HEMT) structures capable of supplying an output power higher than 200 W up to C-band and above are nowadays easy to find in the portfolio of several companies [3, 4].

Therefore, GaN technology has made a remarkable breakthrough allowing the realization of solid state devices with excellent performance also in terms of robustness and reliability. Therefore, they can be exploited to replace TWTAs in those applications that require very high-power levels too. In fact, GaN SSPAs present several advantages with respect to TWTAs such as: lower operating voltages, reduced size and weight, less sensibility to hot electrons phenomena, and absence of heating time. Besides this, aspects such as the graceful degradation and the higher reconfigurability of SSPAs and consequently the possibility of achieving different power levels by combining a variable number of basic modules, further increase the interest in such a technology. Hence, GaN technology can make possible the realization of SSPAs with electric characteristics similar or even better than the ones of the TWTAs, but with smaller size, mass, and potentially higher reliability.

The design, realization, and test of a 230 W GaN SSPA operating in E1-Band (i.e. 1.575 GHz) and in continuous wave (CW) regimes for next generation Galileo satellites is described. The SSPA has been developed in the framework of the European project named SLOGAN [5]. It aims to realize a complete SSPA, including not only the RF unit (RFU), but also all the circuits required to interface the module with the satellite bus (i.e. the Power Supply Unit, PSU), and to control the SSPA functionalities by remote telecommand and telemetry (TC/TM) systems (i.e. the electronic power conditioner unit, (EPC)). The goal is to supply a potential recurring product ready to replace the current TWTAs with higher power, lower mass and volume as well as lower consumption exploiting, as much as possible, European technologies only.

The preliminary results of the power modules designed exploiting the available GaN die power bars have been summarized in [6]. This contribution expands the content of the conference paper describing the overall SSPA architecture and its integration together with more experimental results. It is organized as follows: the overall SSPA architecture and related subunits are discussed in Section II, together with the targeted requirements. Section III provides an in-deep description of the RFU of the SSPA, starting from the evaluation of the used GaN technology up to the realization of the overall RF-chain. Finally, the aspects related to the SSPA mechanical housing and subunits integration are described in Section IV, along with the preliminary SSPA experimental characterization.

Table 1. SSPA requirements.

Requirement	Unit	Value
Freq. band	–	E1
Center freq.	MHz	1575.42
Max. drain voltage	V	45
Bandwidth	MHz	50
Output power	dBm	53.6
Output power	W	230
Max. gain	dB	65
Gain step	dB	1/20
Min. input power	dBm	−23
Max. input power	dBm	−11
Efficiency	%	55
AM/PM	degree	<15
Mass	kg	<3
Size	mm	300 × 200 $H = 200$

II. SSPA ARCHITECTURE AND REQUIREMENTS

The main requirements on the SSPA are listed in Table 1. The requested output power is higher than 230 W with a bandwidth of 50 MHz and a desired efficiency of 55%.

For this purpose, the architecture shown in Fig. 1 was selected to realize the complete SSPA.

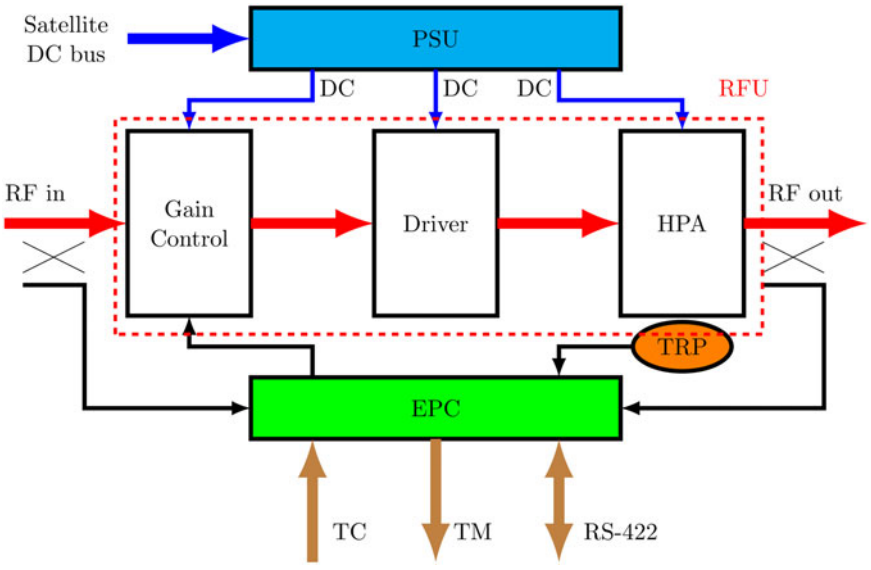

Fig. 1. SSPA architecture.

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It is composed of the following subsystems:

- RFU, aimed to amplify the RF signal from its input (SubMiniature version A (SMA) connected) to its output (Threaded Neill–Concelman (TNC) connected) delivering a minimum of 230 W from 1550.42 to 1600.42 MHz frequency range. This chain also implements a gain control unit (GCU) to properly manage the gain of the overall SSPA and to be able to compensate its variation over temperature and operating conditions.
- PSU, aimed to interface the satellite primary bus voltage (50 V dc) into the required secondary voltages inside the SSPA.
- EPC module, aimed to implement the required functionalities for controlling and monitoring the SSPA behavior.

Clearly, all the aspects related to space qualification constrains, such as mass, volume, temperature, vacuum, multipactor effects, outgassing, reliability, and so on have been accounted for in the design steps.

A) RFU module

For the RFU, and in particular for the power stages, the adopted technology is provided by united monolithic semiconductor (UMS). It is a GaN HEMT process with 0.5 μm of gate length, exhibiting a power density up to 5 W/mm when biased at 50 V of drain voltage. Presently, this technology is space evaluated (i.e. included in the European Preferred Parts List of European Space Agency) but within a limitation in power bar size of 12 mm of the total gate periphery. This power bar, whose photograph is reported in Fig. 2(a), is based on the parallel connection of six elementary cells of 2 mm each. Accounting for the high level of output power required to the RFU, for the final stage a larger power bar is needed. Thus, in this activity, a power bar with twice gate periphery (25.6 mm, 8 × 3.2 mm^2) was also considered, being its space evaluation in progress and expected to be completed within the end of the project. A picture of this bigger power bar is shown in Fig. 2(b).

The RFU, and therefore the entire SSPA, is terminated at the output with a TNC connector, while the input termination is realized through a SMA connector. The TNC connector has been selected because it is the only one capable to sustain such amount of power without generating multipaction and corona discharge. Inside the GCU, the input signal is coupled at −12 dB and detected by using an ADL5501 power detector from Analogue Device. The dc signal provided by the ADL5501 is then sent to the EPC unit that, every 2 ms registers the actual value of the injected RF input power (P_{in}). Similarly, before reaching the TNC connector, the output signal is sampled through a −40 dB coupler and detected by using another ADL5501 to check continuously the level of the delivered output power (P_{out}). Also in this case, the dc signal generated by the power detector is sent to the EPC unit that evaluates the overall gain and, if required, sets the analog attenuator in the GCU in a different state. The automatic gain control algorithm has a response time lower than 5 ms. Moreover it is able to actuate two distinct operating modes:

- *User attenuation:* the spacecraft main control can vary the SSPA gain through the implemented "Gain Up" or "Gain Down" commands in the range of 20 with 1 dB of step, depending on the TC input signal provided to the EPC.
- *Constant gain:* the variations of the gain of the SSPA due to temperature and aging issues are automatically compensated by the EPC that properly sets the attenuator in the GCU.

The temperature of the SSPA is monitored by placing a sensor close to the main heat sources, i.e. the RFU. It represents the temperature reference point (TRP) of the unit. The output signal is provided to the EPC unit that can switch off the power modules if the registered value exceeds the maximum allowed one.

Accounting for the P_{in} range reported in Table 1 (from −23 to −11 dBm), in order to provide the requested P_{out} level of 54 dBm, a power budget analysis of the RFU chain was performed, resulting in the final architecture shown in Fig. 3. In particular, to achieve the required output power level, the parallel combination of four 80 W power amplifiers was identified as the most suitable structure, thus resulting in a final stage (HPA) realized by cascading a 40 W power amplifier (PA) and a parallel combination of four 80 W PAs.

Thus, for the realization of the entire RFU chain, the following building blocks were identified:

- *GCU*, to implement the gain control functionalities;
- *Driver amplifier*, to increase the chain gain;
- *HPA*, to achieve the required output power.

The HPA is then divided in the following subcircuits:

- 40 W power module;
- Input power splitter (IPS 1–4);
- 80 W power module;
- Output power combiner (OPC 4-1).

B) PSU and EPC modules

The PSU purpose is to interface the SSPA to the satellite primary dc voltage and to generate the internal voltages required to the electronic circuits involved in the SSPA. It is based on several DC/DC converters, with the aim to pursue high efficiency and reliability facets, complying the electrical requirements and assuring low output ripple. In this unit, all the DC/DC converters are based on fly-back topology [7], to improve isolation, and have an ON/OFF switch controlled by EPC unit. Moreover, the PSU implements a primary

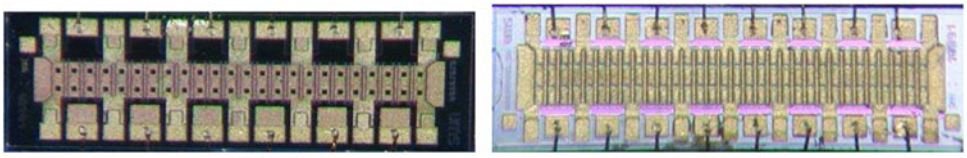

Fig. 2. Power bars provided by UMS, with a total gate periphery of (a) 12 mm (6 × 2 mm^2) and (b) 25.6 mm (8 × 3.2 mm^2).

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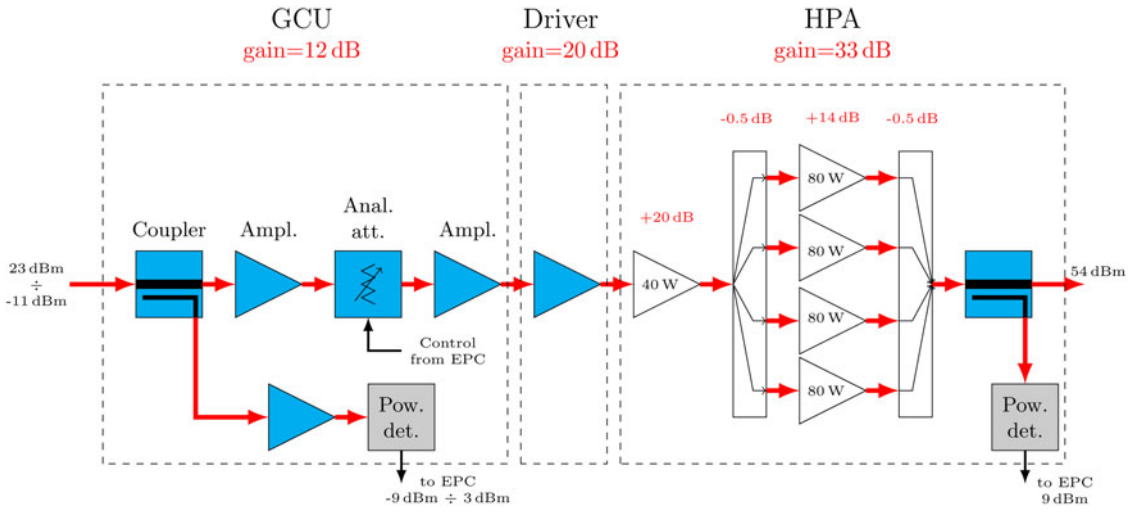

Fig. 3. RFU architecture.

power switch, based on a high-gain Darlington opto-coupler, that can be commanded remotely using an ON/OFF command. The overall architecture of the PSU is reported in Fig. 4.

This topology has been selected in order to improve the reliability of the unit. Indeed, it permits to introduce redundant modules of the most critical subsystems. The PSU main subsystems are:

- *Input filter and inrush limiter module:* this unit eliminates, or reduces as much as possible, the influence of the PSU over the regulated 50 V bus of the satellite, assuring electromagnetic interference compatibility/electromagnetic interference (EMI) compatibility to Galileo satellite power bus.
- *ON/OFF and auxiliary voltages circuit:* it is used either to activate or to deactivate the PSU. It is directly commanded by the payload remote terminal unit (RTU). It also provides auxiliary voltages to the PSU primary and secondary sides.
- *High-power DC module (HPDC):* it supplies the dc power (required voltage and current) to one 80 W power module of the HPA. Thus, four HPDC are integrated in the PSU.
- *Medium-power DC module (MPDC):* This converter supplies the dc power to the driver and the first stage of the HPA. Moreover, it provides the required dc voltage and current to the low-power DC (LPDC) module of the PSU.
- *LPDC:* This unit will supply the dc power to those elements (e.g. gain stages in the GCU, etc.) with positive biasing voltages (i.e. 15, 5, and 3.3 V) and low operating dc currents.

Regarding the EPC module, it is designed to permit the compensation of the RF variations over temperature, properly setting the parameter of the GCU in the RF chain, as well as to

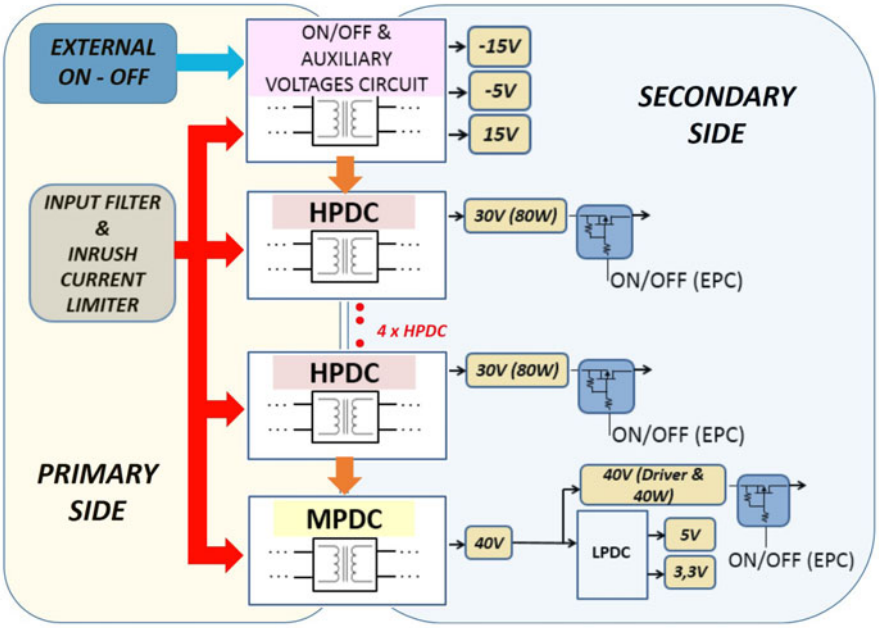

Fig. 4. PSU architecture.

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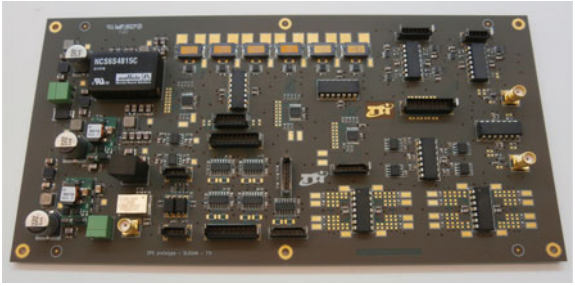


Fig. 5. Photograph of the realized EPC.

control currents and voltages applied to the RF power stages. The architecture of this subsystem is based on a field programmable gate array and a picture of the realized prototype is shown in Fig. 5. Such unit receives telecommands and offers telemetry services thanks to the sensors integrated in the SSPA, i.e. power detectors, temperature, current, and voltage sensors.

III. RFU DESIGNS AND RESULTS

As previously described, the RFU unit is composed of several submodules. In particular, the GaN power bars provided by UMS were adopted to realize the high-power section, as will be described in the following.

A) Evaluation of GaN technology

Before designing the final modules required for the RFU implementation, a preliminary evaluation of the technology has been performed. For this purpose, several single ended prototypes based on 12 and 25.6 mm power bars have been designed, realized, and tested as detailed in [8, 9]. In particular, both PAs have been measured in CW operation evaluating their performance in terms of output power, efficiency, and junction temperature of the device (T_J). The latter has been estimated through the following relation:

$$T_J = T_{BP} + P_{diss} \cdot R_{TH}, \quad (1)$$

where T_{BP} is the base plate temperature, P_{diss} is the power dissipated by the device, and R_{TH} is the overall junction-to-base-plate thermal resistance. The latter was provided by the foundry for each power bar resulting in 3 and 2.4°C/W for the 12 and 25.6 mm device, respectively. The values are different since the layout of the elementary cell used to realize each power bar is not the same, as visible in Fig. 2. Moreover, these R_{TH} values are referred to the carrier material and mounting process adopted by the foundry. In order to be able to extract the thermal resistance of the power bar only, i.e. from the junction to the back-side metallization of the die, one has to know precisely all the materials included at every "*z-section*" of the stack, with related sizes. Unfortunately, the information was not available at the time of the design. To overcome such limitation, a coarse structure of the bigger power bar has been derived from its layout, and by making several assumptions. Such approximated three-dimensional (3D) model of the power bar has been simulated in a thermal computer aided design to infer the channel-to-base-plate thermal resistance considering the actual base-plate material (i.e. copper–diamond) and mounting process (i.e. eutectic) adopted to assembly these prototypes. The resulting number in this case was $R_{TH} = 2.1$°C/W, thus lower than that provided by the foundry, due to the better material adopted for the base-plate (i.e. copper–diamond instead of pure copper) and mounting approach. However, to be conservative since there was no possibility to check the assumption done to extract the 3D model of the power bar, the same values provided by the foundry have been used to evaluate the junction temperature of the PAs during the overall test campaign (i.e. 3 and 2.4°C/W for the 12 and 25.6 mm device, respectively).

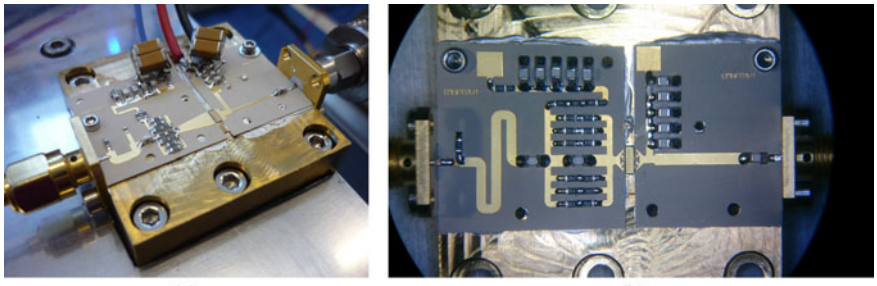
The photographs of the two prototypes are reported in Fig. 6.

The 12 mm PA prototype has been measured in CW operation at the center frequency $f_o = 1575.42$ MHz, for different drain bias voltages V_{DD} (from 35 to 45 V) and fixed $V_{GG} = -1.5$ V, while sweeping the input power and monitoring the output power, efficiency, and junction temperature T_j.

The measurements have been repeated for different base plate T_{BP} temperatures, ranging from 20 to 70°C (i.e. the maximum T_{BP} that is expected for Galileo satellite application). In Fig. 7 are reported the results obtained for $T_{BP} = 70$°C, from which it was concluded that the 12 mm power bar exceeds the maximum junction temperature of $T_j = 160$ at $T_{BP} = 70$°C when biased with a drain voltage of $V_{DD} > 40$ V.

Similar tests have been performed on the PA based on the 25.6 mm device. In this case, the results show that the drain bias voltage should be limited to $V_{DD} \leq 30$ V to be compliant with the maximum T_j of 160°C. In Fig. 8, are reported the measured performances for $V_{DD} = 30$ V and for different base plate T_{BP} temperatures.

The measured results of this prototype highlighted that the larger power bar should operate with a maximum V_{DD} of 30 V, resulting in a maximum output power of 55 W. For this reason, different solutions to implement the 80 W



(a) (b)

Fig. 6. Photograph of the realized prototypes for the technology evaluation, based on (a) 12 mm and (b) 25.6 mm power bars.

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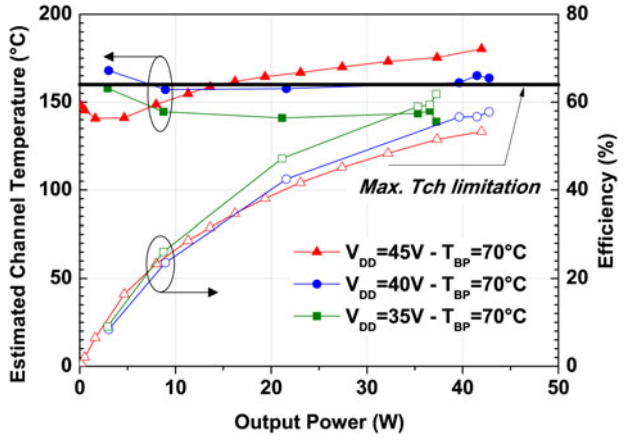

Fig. 7. Power sweep measurements on the 12 mm PA prototype for different V_{DD} bias voltages.

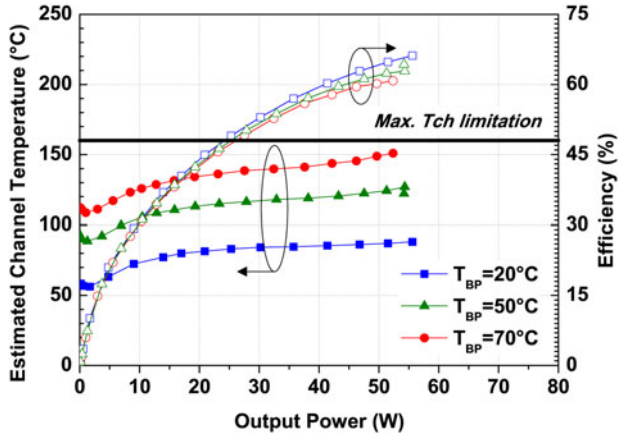

Fig. 8. Power sweep measurements on the 25.6 mm PA prototype for $V_{DD} =$ 30 V and different T_{BP}.

module have been elaborated (i.e. combination of more than one power bar).

B) The 80 W power module

The 80 W power module has been implemented in two different versions: the first one combining two power bars of 12 mm, in the following referred to as 80_V1, while the other one combining two power bars of 25.6 mm, referred to as 80_V2. For the design of these prototypes, the selection of suitable substrates has been preliminarily performed accounting for thermal, outgassing, and multipactor issues. As a results of this analysis, Roger duroid 6010.2 LM material ($H = 254$, $T = 17$ μm and dielectric constant of 10.7) has been selected to design the matching networks.

The designs have been performed exploiting large signal simulations on the available non-linear model provided by the foundry. The nominal dc drain voltage for both versions was selected according to the limitation previously discussed, i.e. $V_{DD} = 40$ V for 80_V1 and $V_{DD} = 30$ V for 80_V2, while a deep class AB bias condition has been assumed for both. The first step in the design was related to the identification of a proper stabilization network at the gate terminals, to assure an unconditional stability at all frequencies. The latter has been achieved by using a resistors' matrix, to account for the de-rating values of passive elements, inserted in series with the gate. Then, the device optimum output loads have been estimated through simulations, also controlling the higher harmonics to maximize the efficiency [10]. The resulting output network comprises a biasing stub, used also to compensate the device output capacitance, and a quarter wavelength transformer toward the 50 Ω load. Finally, the input network has been designed by using a distributed approach to complex conjugately match the device input, including the stabilizing network. The photographs of the realized prototypes are shown in Fig. 9, and the total size of both prototypes is 41 × 22 mm².

The power bars were mounted with eutectic process on a copper–diamond test-jig and both amplifiers have been tested in CW conditions, at center frequency f_o.

With 40 V drain voltage and a total I_{dc} current of 0.9 A, the first prototype 80_V1 shows an output power of 48.7 dBm with an efficiency of 61.5% at 3 dB of gain compression. Conversely, version 80_V2 shows a higher output power, up to 50.5 dBm, and an efficiency of 73% when biased with 30 V. The measured gain, efficiency, and channel temperature behaviors as a function of the output power at center frequency are shown in Fig. 10.

Also in this case T_j has been computed assuming the worst case thermal resistance value, i.e. $R_{TH} = 3$°C/W for the prototype based on 2 × 12 mm² power bars (80_V1), and $R_{TH} =$ 2.4°C/W for the prototype based on 2 × 25.6 mm² power bars (80_V2).

Considering a base plate temperature of 20°C, the maximum channel temperature reached by each power bar is <90°C in both cases. From the measured results, the prototype 80_V2 has been selected as the best solution to implement the 80 W power module in the final version of the RFU.

The measured AM/PM of such module is shown in Fig. 11, while the frequency sweep results measured at 3 dB of gain compression are reported in Fig. 12.

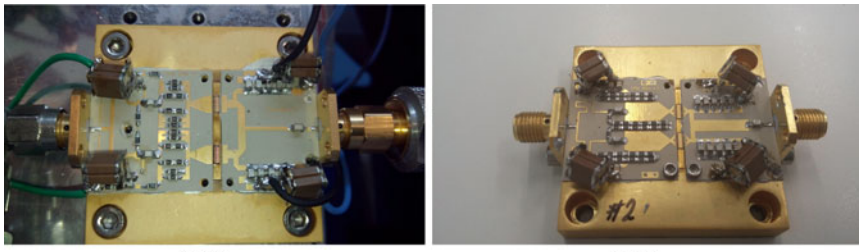

Fig. 9. Photograph of the realized 80 W power amplifiers: (a) based on 2 × 12 mm² (80_V1) and (b) based on 2 × 25.6 mm² (80_V2) power bars.

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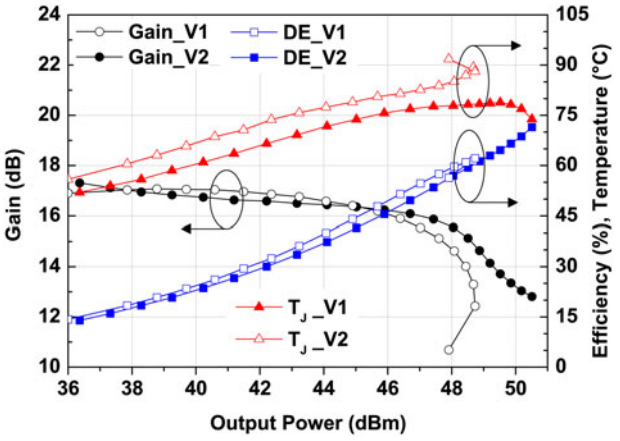

Fig. 10. Gain, efficiency and junction temperature versus output power of both 80 W PAs, for $T_{BP} = 20°C$.

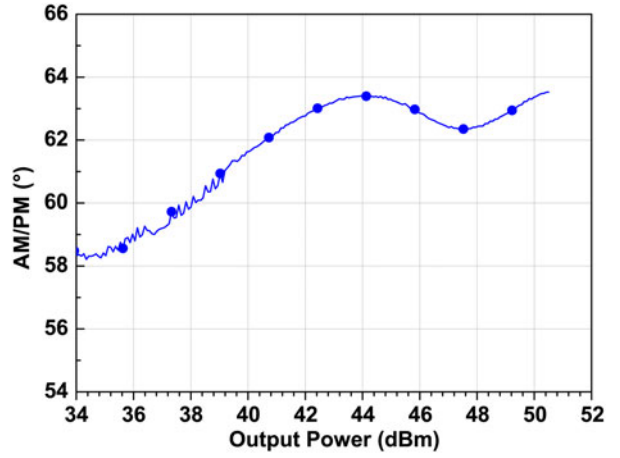

Fig. 11. AM/PM measured for 80_V2 PA prototype at center frequency.

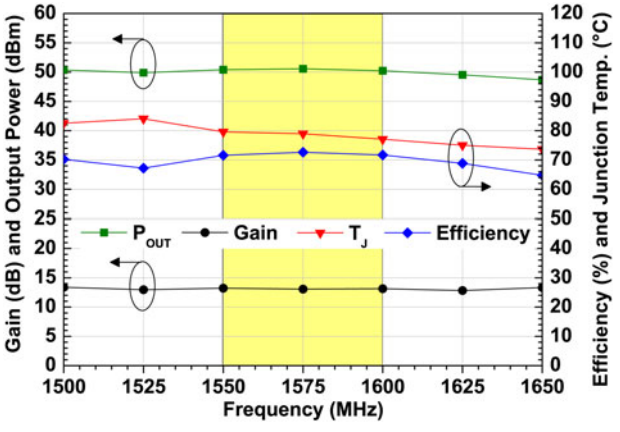

Fig. 12. Gain, efficiency and junction temperature versus frequency of 80_V2 PA prototype, measured at 3 dB of gain compression.

As can be noted, an output power level higher than 110 W (50.5 dBm) with a power gain of 13 dB have been obtained in the targeted bandwidth, with an efficiency larger than 70%, while the T_j does not exceed 80°C for a base plate temperature of 20°C. Moreover, the AM/PM distortion is limited to maximum 5°.

C) Input splitter and output combiner designs

The IPS and the OPC have been designed to implement a 1-to-4 splitting and a 4-to-1 combining function, respectively. Both designs employ two 50 Ω branch-line couplers combined through quarter-wave transmission lines at f_o with proper characteristic impedances. For these structures, a different substrate has been selected, considering the high-power level that has to be handled by the OPC. In particular, the Roger 6035 high-temperature coefficient material ($H = 254$, $T = 17$ μm and dielectric constant of 3.5) has been used.

Finally, the output power sampling functionality has been implemented inserting, in the OPC, a coupled line just before the TNC connection. As already discussed, the coupled signal is firstly detected and then sent to the EPC unit. The photograph of the realized prototypes is reported in Fig. 13, while Fig. 14 shows the measured S21 of the combination demonstrating losses lower than 1 dB, considering the contributions of connectors and adapters required for test purposes. Moreover, the isolation among ports at which the 80 W modules are connected is always better than 15 dB, in both splitter and combiner structures.

D) The 40 W and driver modules

Accounting for the results obtained during the evaluation of the GaN power bars, for the 40 W and driver modules, the

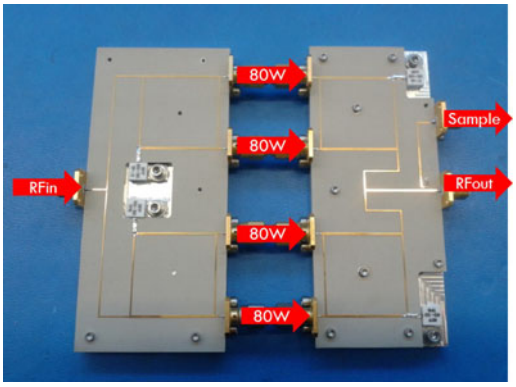

Fig. 13. Photograph of the input splitter and output combiner connected through SMA for test purposes.

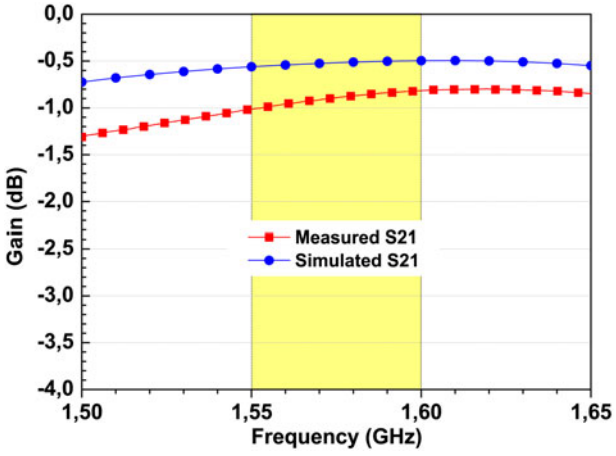

Fig. 14. Measured S21 of the input splitter – output combiner.

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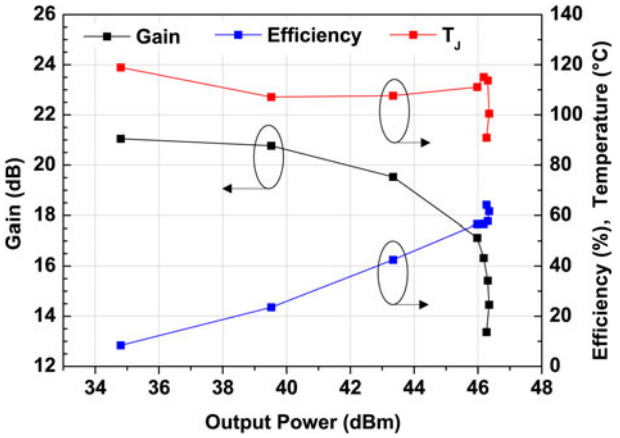

Fig. 15. Gain, efficiency and junction temperature versus output power of the 40 W power module.

same prototype shown in Fig. 6(a) has been used in the final implementation of the RFU. The best compromise among performance and channel temperature reached by the power bar has been registered at the nominal bias voltage of $V_{DD} = 40$ V. In this condition, a saturated output power of about 46.7 dBm at 3 dB of compression has been measured, with an efficiency of 60%, as shown in Fig. 15. In the same figure is also reported the estimated junction temperature, considering again an $R_{TH} = 3$°C/W. It is also worthy to note that, from the power budget reported in Fig. 3, the power required at the 40 W module output section is about 41 dBm. Therefore, the selected PA will work linearly due to the large back-off (i.e. 5 dB, output power reduced from 46 to 41 dBm). Of course, this operating condition is not the optimum one from the efficiency point of view, but, thanks to the high gain achieved by the final stage, the impact of the 40 W module efficiency onto the overall SSPA efficiency is negligible. Moreover, this choice assures the best linearity performance at the SSPA level, while providing enough margins to compensate for power degradation due to aging and temperature effects.

E) GCU

The GCU has been designed on the architecture shown in Fig. 16, and it is based on the adoption of commercial devices for the three gain stages (all from UMS, CHA3801-99F) and the variable attenuator (from Hittite, HMC3466MSBG), while the other blocks have been designed *ad hoc*.

The picture of the realized prototype of the GCU is reported in Fig. 17, while in Fig. 18 is shown the measured gain for several attenuation steps. As can be noted, the prototype provides more than 20 dB of attenuation range with very flat frequency response. The GCU has also been tested in nonlinear regime in order to evaluate its amplitude and phase distortions. Figure 19 shows the results at center frequency and when the attenuator is set to provide 16 dB of attenuation. The GCU is able to deliver an output power higher than 13 dBm without any significant compression and with an AM/PM lower than one. From the power budget analysis reported in Fig. 3, the required output power level at the interface between the GCU and the Driver is around 1 dBm. Therefore, there is a margin of 12 dB of gain that can be exploited to compensate the drift of the RF performance of the GaN devices due to temperature variations and aging effects.

IV. SSPA INTEGRATION AND EXPERIMENTAL RESULTS

All the subsystems previously described have been housed in a box to provide a ready-to-fly SSPA for space-borne transmitter. For this purpose, all the aspects related to space qualification constrains are accounted for, as for example the multipaction and corona effects, in particular for the output TNC connector. Moreover, a thermal analysis has also been performed to avoid hot spot in the SSPA and to assure proper heat dissipation for the power bars, in particular those used in the final stage (i.e. 80 W module). This analysis has been carried out using a simplified geometry of the SSPA box, and including the most relevant heat loads in the RFU subsystem. Figure 20 shows such model in which the modular base-plates of the driver, 40 and 80 W modules are indicated.

Essentially, the SSPA thermal design has to guarantee that the junction temperature of the power bars does not exceed 160°C and that the heat flux at the heat-sink level (i.e. at the interface between SSPA and satellite chassis) does not go over the value of 3.5 kW/cm². The last one is a Galileo system requirement. Considering a pure aluminum box for the SSPA, the resulting maximum junction temperature of every device was lower than 126°C, thus well below the upper bound. However, in this case, the heat flux was not compliant with the specification due to the low ability of the aluminum to spread the heat. To overcome the problem, an annealed pyrolytic graphite (APG) layer has been encapsulated into the aluminum box, just under the RFU high-power modules (see Fig. 20), in order to reduce the heat flux at the base. The APG layer has the capability to reduce the heat flux thanks to an anisotropic thermal conductivity, 1700 W/(m °C) in the x–y-plane and only 10 W/(m °C) along the z-axes, in our case. The optimal thickness of the APG layer has been identified through simulations, resulting in

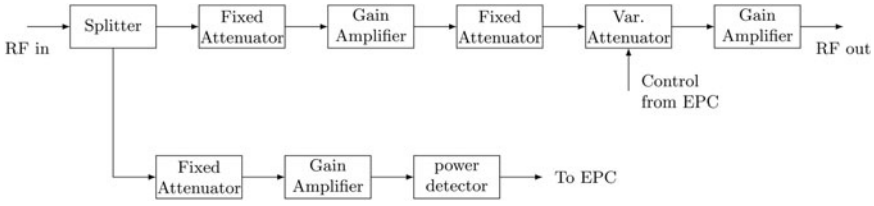

Fig. 16. Architecture of the designed GCU.

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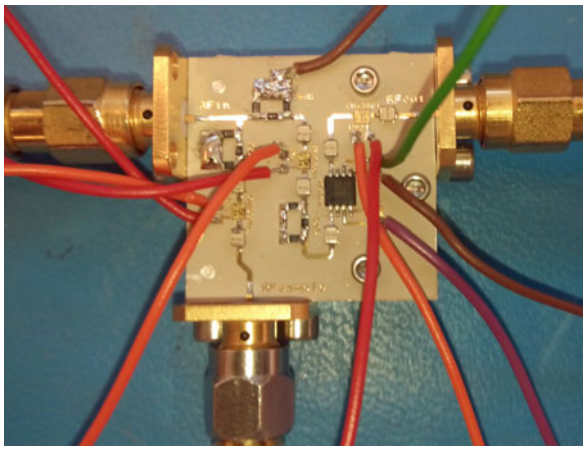

Fig. 17. Photograph of the realized prototype of the GCU.

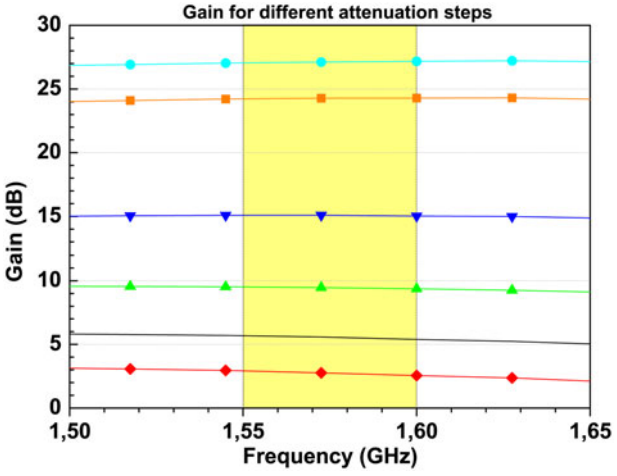

Fig. 18. Measured gain for several attenuation steps of the GCU.

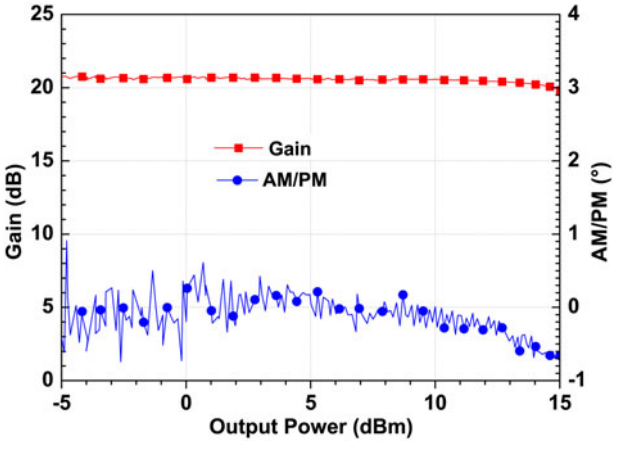

Fig. 19. Measured AM/AM and AM/PM of the GCU.

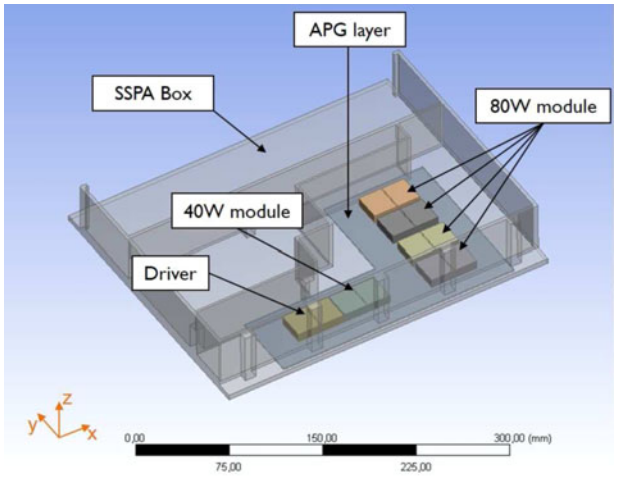

Fig. 20. Simplified model of the SSPA box used for thermal analysis.

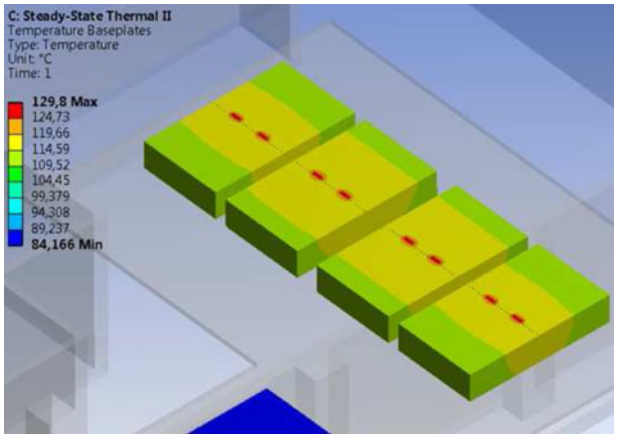

Fig. 21. Thermal analysis of the four 80 W power modules housed in the SSPA box.

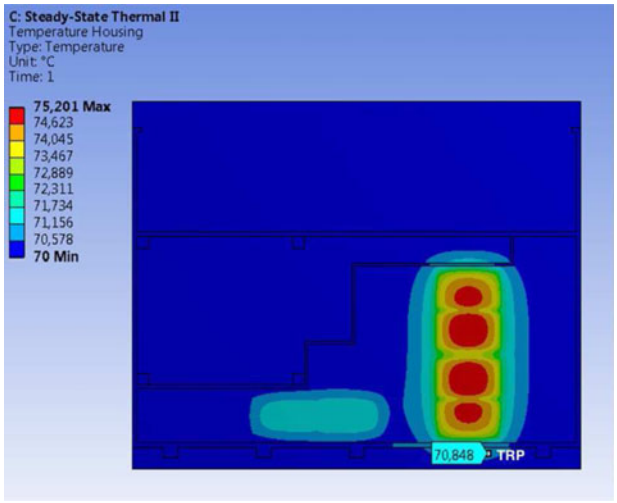

Fig. 22. Temperature distribution in the SSPA box.

1.5 mm. The integration of the APG layer in the aluminum box of the SSPA has reduced the maximum heat flux to 2.33 kW/cm^2, thus well below the requirement. However, it causes a little increase in the junction temperature of the devices from 126 to 130°C. Figure 21 shows the temperature in the 80 W modules when housed in the overall SSPA box with the APG layer. As already mentioned, the expected maximum junction temperature value is around 130. Whereas, the thermal map of the overall SSPA is reported in Fig. 22 showing the position of the TRP too.

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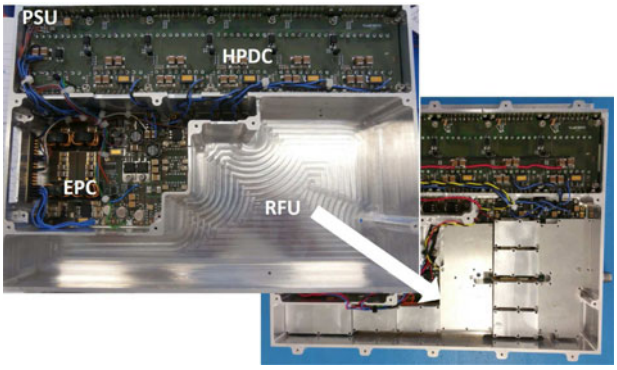

Fig. 23. Mechanical housing of SSPA subsystems.

A picture of the SSPA is reported in Fig. 23, where the location of each subsystem inside the mechanical box is also highlighted. The connections between adjacent modules in the RFU have been realized through ribbon wires, and each module has been singularly shielded in order to avoid EMI in and from them. The picture of the final SSPA is shown in Fig. 24. Sizes are 300 × 245 × 55 mm^3 while weight is <3 kg.

The measured RF performance of the complete SSPA are shown in Fig. 25 for a base plate temperature of $T_{BP} = 35$ and $T_{BP} = 70^{\circ}$C.

As can be noted, at $T_{BP} = 35^{\circ}$C the SSPA provides a minimum output power of 250 W, at 1.6 dB of gain compression, with an efficiency of 53.7% (dissipated power 215 W) and a minimum gain of 53.2 dB (the GCU gain is set to 0 dB), while the saturated power is about 400 W. Similarly, at $T_{BP} = 70^{\circ}$C, 235 W of output power has been achieved at 2 dB of gain compression, with an efficiency of 51.8% (dissipated power 219 W) and a minimum gain of 51.2 dB (the GCU gain is set to 0 dB). Also in this case, the saturated power is close to 400 W. In terms of linearity, the measured AM/AM and AM/PM have been <2 dB and 15°, respectively. Moreover, the latter value could be further optimized by properly tuning the gate biasing voltages of the RFU GaN-based amplifiers (i.e. Driver, 40 and 80 W PAs).

The actual state-of-the-art of HPAs for L-band satellite applications is summarized in Table 2. As can be noted, the improvement reached with this realization is notable, especially in terms of gain and output power for CW operation mode.

V. CONCLUSION

In this contribution, the design of an SSPA for space-borne Galileo system employing GaN European technology has been presented. The amplifier is the first prototype developed in the framework of the European project named SLOGAN. In CW operating mode, the overall SSPA is able to deliver an output power higher than 250 W at <2 dB of gain compression in the whole E1-band. Moreover, the registered gain

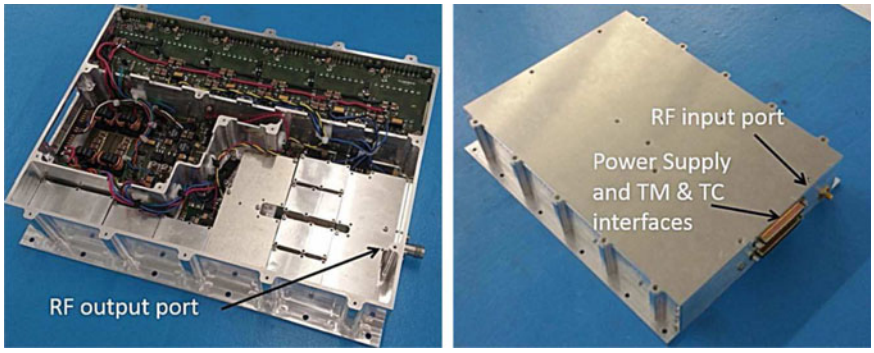

Fig. 24. Final SSPA unit integration.

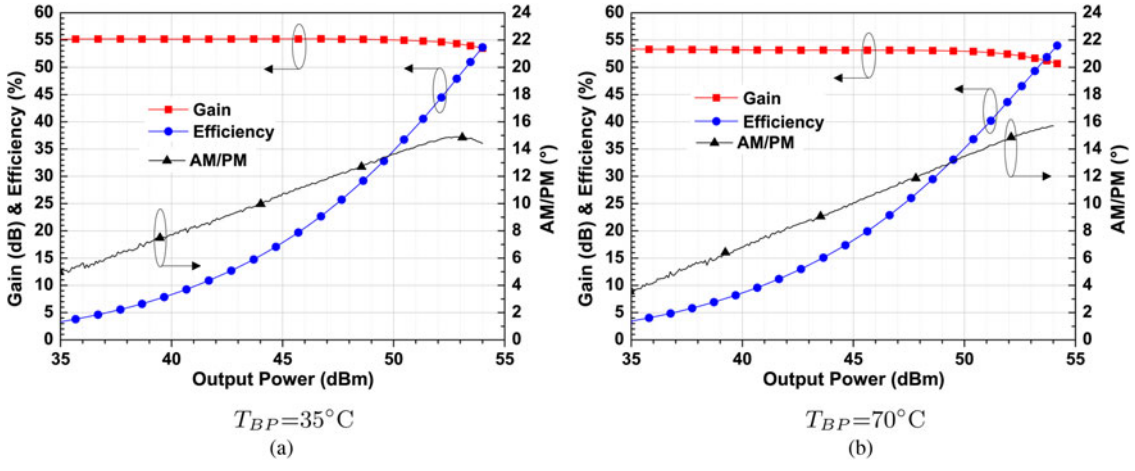

Fig. 25. Measured performances of the SSPA at (a) $T_{BP} = 35^{\circ}$C and (b) $T_{BP} = 70^{\circ}$C.

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Table 2. State-of-the-art power amplifiers for L-band.

References	Tech.	Freq. (GHz)	P_{sat} (W)	Mode	Gain (dB)	η (%)
[11]	TWTA	1.5–1.64	200	–	50	70
[12]	BJT	1.34–1.41	100	CW	12	–
[13]	GaN (EU)	1.2–1.32	140	CW	16	55
[14]	GaN	1.5	500	Pulsed	18	49
[15]	GaN	1.2–1.4	1000	Pulsed	53	50
T.W.	GaN	1.55–1.6	400	CW	67	55

and efficiency are higher than 67 dB and 54%, respectively. The prototype has reached the Technology Readiness Level number six.

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