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RESEARCH PAPER

Compact multi-layer *N*-way power divider with closed-ring-shaped isolation network

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A compact multi-layer N-way power-dividing structure with good isolation and output return loss performance is proposed. The isolation network is circularly distributed that constitutes a closed ring-shaped architecture. The equivalent circuit model is given and the [S] matrix is developed to analyse and design the power-dividing structure. Finally, a six-way power divider centered at 2.1 GHz is designed and fabricated. The measured and simulated results agree well with each other. The total size of the power divider is $0.13\lambda_g \times 0.19\lambda_g$.

Keywords: Multi-layer, Multi-way, Power divider, Isolation

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I. INTRODUCTION

Power divider used to split signals to multi-ways plays a critical role in nowadays microwave communication systems. It could be used in the power-combing amplifier, mixer, and the feeding network of the array antenna [1–16]. Since the Wilkinson power divider has been proposed in the 1960s [3], great interest has been aroused in developing various kinds of power dividers, such as the waveguide-based power divider [1–6], quasi-optical power divider [7, 8], and planar power divider [9–16]. Among these power dividers, the planar power divider, which has advantages of compact size, easy to fabricate, and high level of integration, is widely used in microwave systems. However, it is difficult to imply the isolation network on the planar N-way ($N \geq 3$) power dividers because of the requirement of a three-dimensional common node to connect all the isolation resistances together, and the multi-stage N-way binary power divider suffers the defect of high insertion loss [10, 11]. Thus, the planar multi-way power dividers with the characteristics of high isolation and compact size are still in urgent demand.

This paper presents a novel N-way compact power divider with good isolation and all port impedance matching. The isolation network is circularly distributed, which constitutes a closed ring-shaped architecture. The power-dividing network is analysed in detail. Theoretically, the proposed structure could realize the power divider with arbitrary numbers of output ports. The results show that the proposed power-dividing structure has the advantages of high isolation, compact size, excellent output and input impedance matching, and low insertion loss.

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II. STRUCTURE, ANALYSIS, AND DESIGN

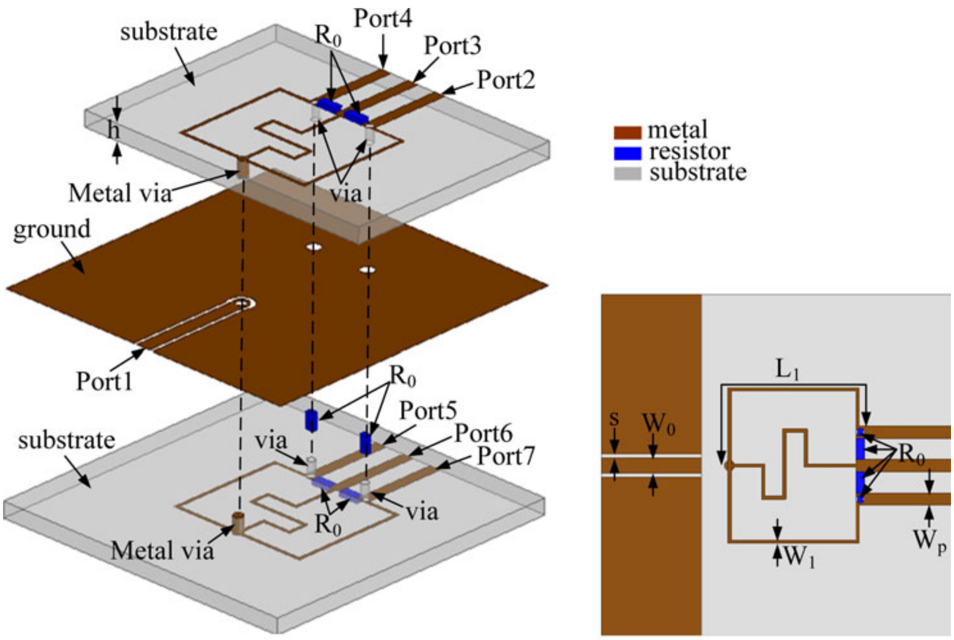
To realize the multi-way high-isolation power divider, a two substrate layers and three metal layers power dividing network is presented, as shown in Fig. 1. The three metal layers lie on the top, middle, and the bottom of the two substrate layers, respectively. The middle metal layer acts as the common ground for the top and bottom microstrip line. Port1 (input port) is CPW lying on the middle metal layer, and port2–port7 (the output ports) are the microstrip lines lying on the bottom and top metal layers, respectively. The radially placed output ports, through six transmission lines (TLs) with each one being characteristic impedance Z_1 and electric length L_1, split directly the input power into six ways with equal amplitudes and phases through the central metal via.

Meanwhile, the isolation network is circularly distributed and the isolation resistors R_0 are connected among neighboring TLs, as illustrated in Fig. 2. The isolation network constitutes a closed ring-shaped architecture; thus, the common node is avoided compared with the Wilkinson multi-way power dividers. Around the sided isolation resistor, the middle metal layer is etched to avoid the signal being shorted to the ground. Theoretically, the proposed structure could realize the power divider with arbitrary numbers of output ports.

Figure 3 gives the equivalent circuits of the direct 1–6-way power division networks. Z_{CPW} and Z_1, Z_0 are the impedance of the input CPW TL and the microstrip TLs, respectively. Fig. 3(b) depicts the even-mode equivalent circuits.

According to the even-mode equivalent circuit, the electric length of L_1 is chosen to be $\lambda_g/4$ to realize the input impedance matching, where λ_g is the guide wavelength at the operating center frequency. Thus, we have

$$Z_1 = \sqrt{6}Z_0. \tag{1}$$



(a) (b)

Fig. 1. The model of the novel four-way power-dividing structure. (a) Three-dimensional structure; (b) top view.

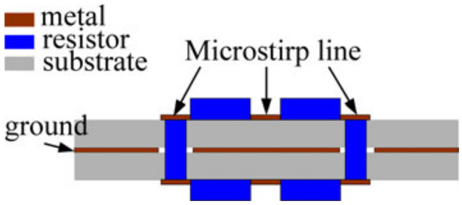


Fig. 2. Assembly layout of the isolation resistor.

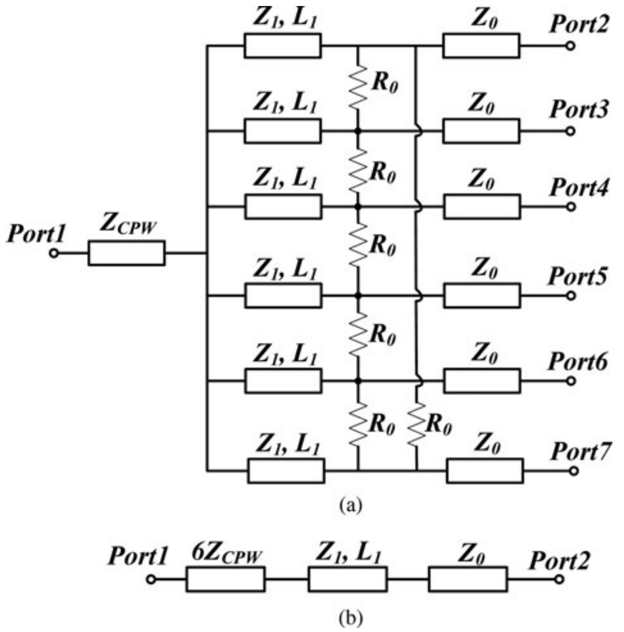


Fig. 3. Equivalent circuits of the direct 1–6-way power divider. (a) Proposed architecture equivalent circuit; (b) even-mode equivalent circuit.

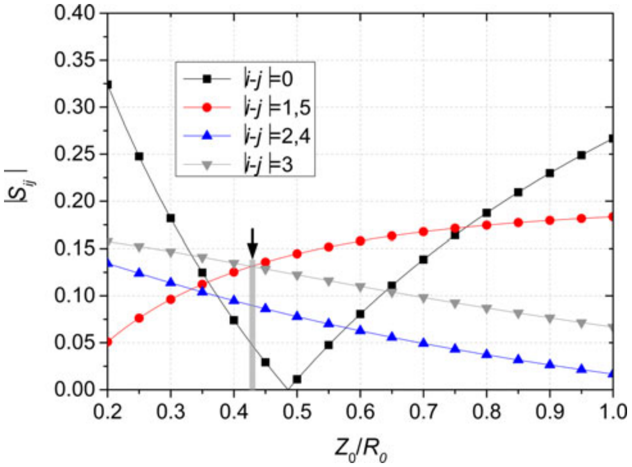


Fig. 4. The calculated results of $|S_{ij}|$ against the value of Z_o/R_o.

By developing the [S] matrix [13] among the output ports, the isolation performance of the proposed power divider could be obtained. The isolation and output return loss could be given by

$$S_{ij} = 2f_{ij}\left(\sqrt{1+4(Z_o/R_o)}\right) - 1/n - \delta_{ij}, \tag{2}$$

where n is the number of the output ports, $i = j = 2,3,\ldots,7$, δ_{ij} is the Kronecker δ, and

$$f_m(x) = x^{-1}\left(y^{n/2-m} + y^{m-n/2}\right)\left(y^{n/2} - y^{-n/2}\right)^{-1}, \tag{3}$$

$$\delta_{ij} = \begin{cases} 0, & i \neq j \\ 1, & i = j \end{cases}, \tag{4}$$

Table 1. Circuit dimensions.

Dimensions	W_o (mm)	W_1 (mm)	W_p (mm)	s (mm)	L_1 (mm)	R_o (Ω)
Calculated	1.46	0.16	1.14	0.13	23.5	116
Optimized	1.46	0.15	1.14	0.13	23.3	116

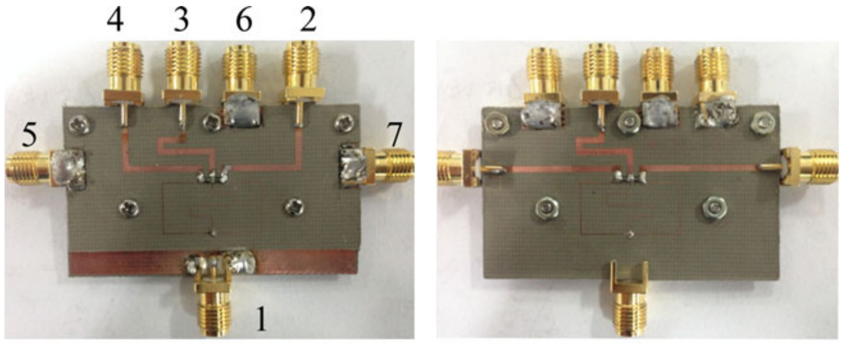
with $y = (x+1)/(x-1)$, $x = \sqrt{1+4(Z_o/R_o)}$, $m = |i-j| = 0, 1, 2, \ldots, 5$.

To obtain the optimal isolation and output impedance matching, the maximum of $|S_{ij}|$ should be minimized.

Therefore, through equations (1)–(4), the multi-way high-isolation power divider could be easily designed at the required frequency. The calculated results of equation (2) are shown in Fig. 4. It can be seen that the value of isolation and output return loss varies with the value of Z_o/R_o, and the minimized value of $|S_{ij}|$ is 0.13 (−17.7 dB) with $Z_o/R_o = 0.43$ as labeled in Fig. 4.

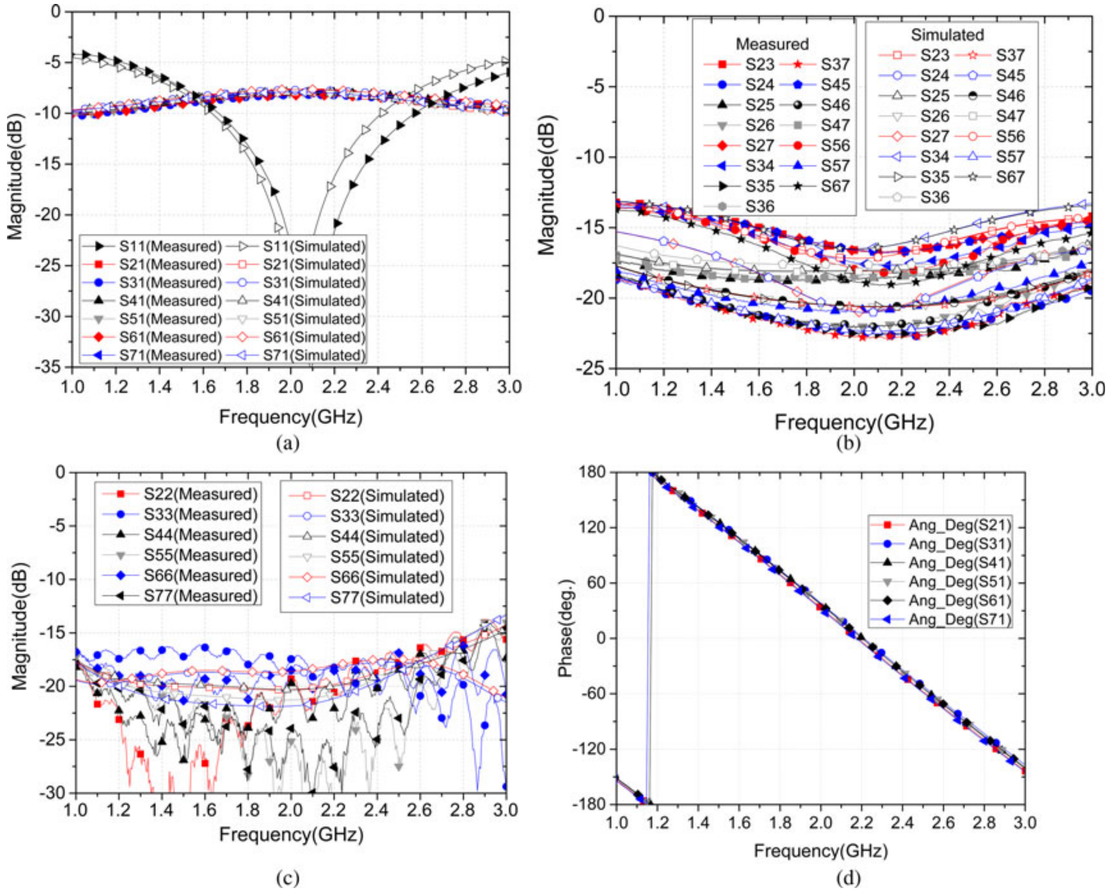
According to the above analyses, the design procedure of the proposed power dividers is as follows:

(1) As the desired frequency f_o is given, the guided wavelength of microstrip line λ_g could be calculated based on the chosen substrate; therefore, L_1 can be derived. According to equation (1), the characteristic impedance Z_1 could be derived.



(a) (b)

Fig. 5. Photograph of the fabricated power divider. (a) Top view; (b) bottom view.



(a) (b) (c) (d)

Fig. 6. The measured and simulated results of the fabricated power divider. (a) Measured and simulated S-parameter; (b) measured and simulated isolation; (c) measured and simulated output return loss; (d) measured phase.

Table 2. Comparison with other multi-way power dividers.

Performance	Center frequency (GHz)	15 dB isolation (GHz)/RBW (%)	15 dB ORL (GHz)/RBW (%)	Size($\lambda_g \times \lambda_g$)	Insertion loss (dB)	NOP
[1]	9.3	9.4–10.1/7.1	9.3–10.3/10.2	0.62 × 2.58	7 ± 0.5	4
[14]	3.2	3.1–3.4/9.2	3.1–3.16/1.9	1.45 × 1.45	8.1 ± 0.3	6
[15]	6.9	None	None	0.52 × 0.54	6.8 ± 0.4	4
[16]	2.1	1.59–2.48/43.7	1.1–3.0/92.6	0.17 × 0.31	6.35 ± 0.2	4
This work	2.1	1.6–2.8/54.8	1.0–2.9/97.4	0.13 × 0.19	8.05 ± 0.15	6

RBW, relative bandwidth; ORL, output return loss; None, isolations <20 dB; NOP, number of output ports.

(2) According to equation (2), the value of the isolation resistor R_o could be derived. Therefore, the multi-way power divider with optimal isolation and output impedance matching can be obtained.

III. EXPERIMENTAL RESULTS

Based on the analyses given above, a six-way high-isolation power divider/combiner was designed and fabricated. The structure was optimized in Ansys-HFSS. The used substrate is Taconic RF-35 with a dielectric constant ε_r of 3.5, a thickness of 0.508 mm, and a loss tangent of 0.0018. The calculated and optimized dimensions are shown in Table 1.

Figure 5 gives the fabricated six-way power divider. All the ports are terminated with the type-SMA connectors.

The simulated and measured results of the six-way power divider are shown in Fig. 6. Figure 6(a) gives the simulated and measured results of the *S*-parameters. It shows that the measured and simulated results agree well with each other over the operating frequency band. The measured input return loss is larger than 15 dB from 1.82 to 2.38 GHz and larger than 20 dB from 1.97 to 2.22 GHz. The measured insertion losses are within 8.05 ± 0.15 dB including the insertion loss of SMA-connector to microstrip transitions over the frequency from 1.9 to 2.25 GHz. Figure 6(b) shows the measured result of isolation between the six output ports, and Fig. 6(c) shows the measured results of output return loss of each output ports. The measured isolations are all >15 dB over the frequency from 1.6 to 2.8 GHz, while the isolations in the operation center frequency are all >16.8 dB at 2.1 GHz. The measured output return losses are >16.2 dB from 1.0 to 2.7 GHz, which illustrates the calculated result in Fig. 4, and the measured result of each output port's phase is shown in Fig. 6(d). The final size of the power divider is 0.13 × 0.19 λ_g.

Table 2 shows the performance of some multi-way power dividers in recent years. It can be seen that this work realized better performances of isolation, output return loss, and insertion loss.

IV. CONCLUSION

This work presents a compact *N*-way power divider with good isolation and all ports impedance matching. It could be easily designed according to the equivalent circuits. The measured and simulated results agree well with each other; it indicates that the proposed power divider has the advantages of good isolation, compact size, excellent input and output impedance matching, and low insertion loss. The proposed structure could realize the power divider with arbitrary numbers of output ports.

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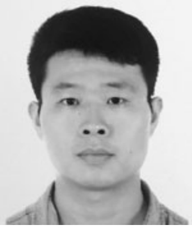

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