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Overcoming the relative bandwidth limitations of single VCO frequency synthesizers by implementing a novel PLL architecture

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Research Paper

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Abstract

Frequency-modulated continuous-wave radar systems profit from increasing the absolute bandwidths of the generated frequency chirps to improve range resolution. As the relative bandwidth of SiGe-voltage-controlled oscillators (VCOs) is limited to about 80%, increasing the center frequency fundamentally or via frequency multiplication is the most direct way to increase that absolute bandwidth. However, as some applications require penetration depth, which dramatically decreases with frequency, other solutions are necessary. Therefore, state-of-the-art concepts rely on the down-conversion of generated frequency chirps via two separately stabilized frequency sources. This article implements a novel architecture, offering relative bandwidths of >100% within a single phase-locked loop (PLL). Therefore, two VCOs at different center frequencies are fed into a down-conversion mixer, whose output is directly stabilized via that PLL with one loop filter generating both tuning voltages. Those circuit blocks can be summarized as one equivalent VCO, offering a higher relative bandwidth and a significantly more linear tuning curve. Thereby, a solution to limited relative bandwidths with high VCO gain variation of single VCO synthesizers is offered while substantially reducing the hardware and implementation effort compared to the state-of-the-art.

Introduction

High-resolution frequency-modulated continuous-wave (FMCW) radar systems are used in several applications, from industrial thickness measurements to landmine detection [1, 2]. This is partly thanks to their robustness to environmental influences like dust, steam, and fog. The range resolution of those systems is defined by the minimum resolvable distance of two adjacent targets, which is given by:

$$d_{\mathrm{res}} = \frac{c}{2B}. \tag{1}$$

As this distance decreases, the range resolution, therefore, improves with the bandwidth B of the continuous frequency chirps. For synthetic aperture radar-based imaging, this corresponds to the depth resolution of the image [3]. Because any oscillator generating those chirps with a maximum and minimum frequency of f_{max} and f_{min}, respectively, offers limited relative bandwidth

$$B_{\mathrm{rel}} = \frac{B}{f_{\mathrm{c}}} = \frac{2(f_{\mathrm{max}} - f_{\mathrm{min}})}{f_{\mathrm{max}} + f_{\mathrm{min}}}, \tag{2}$$

an improved range resolution thanks to a larger absolute bandwidth can be achieved more easily at a higher center frequency f_{c}. In wideband radar systems, this is often utilized by incorporating a frequency multiplier behind the oscillator to increase f_{c} and B simultaneously [4, 5]. Apart from smaller form factors due to the decreased wavelength, the promise of larger absolute bandwidths is one of the main drivers toward THz systems [6]. However, a high f_{c} also comes with several disadvantages. In addition to the increased demands on the transistor speed and packaging solutions, the electromagnetic waves' penetration capabilities decrease rapidly with frequency [7].

Therefore, systems can require a large bandwidth at a specific f_{c} depending on the desired application. In [8], four different systems with center frequencies of 195 MHz, 750 MHz, 5 GHz, and 15 GHz, respectively, were utilized to image polar ice caps. Each system addresses a specific measurement, from surface topography to deep internal imaging, with resolutions ranging from 4 cm to 20 m. Specifically, the "snow radar" offers a B of 6 GHz at an f_{c} of 5 GHz, equaling a B_{rel} of 120%.

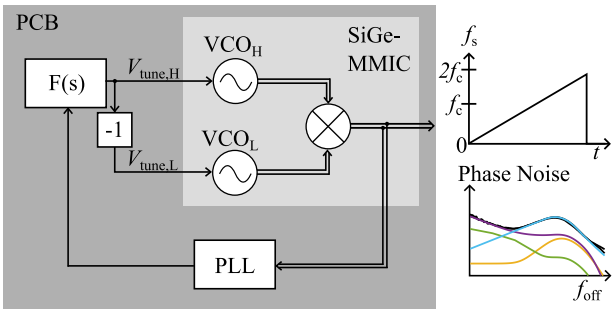

Figure 1. Block diagram of the proposed PLL concept. One PLL generates the tuning voltages for two RF-VCOs to sweep them simultaneously. Their output frequencies are down-converted to generate a signal with a very high relative bandwidth. By stabilizing the mixer's output only one PLL is needed.

State-of-the-art silicon-based voltage-controlled oscillators (VCOs) are not able to achieve those relative bandwidths, topping off at about 80% [9, 10]. Those values are exceeded by other oscillator types, such as YIG-tuned oscillators (YTOs) with 168% in [11] and opto-electronic oscillators (OEOs) with 178% in [12], respectively. However, YTOs and OEOs are comparatively frail and bulky due to the required YIG sphere or laser, respectively, and their use therefore contradicts the benefits of the radar systems outlined at the beginning of this section.

To achieve similar relative bandwidths with VCOs, switchable concepts are proposed in the literature. This includes one core with different dividers in [13] or multiple VCO cores in combination with a divider in [14]. Within a single core, [15] offers limited continuous varactor tuning around broadly switchable center frequencies by utilizing a discretely tuneable artificial transmission line. However, these approaches do not offer the continuous tuning necessary for FMCW chirp generation, as switching between different cores or center frequencies will introduce significant phase errors.

Instead, the state of the art has developed different concepts of combining multiple frequency sources to generate continuous chirps with a high relative bandwidth. Therein, two synthesizers based on direct digital synthesis (DDS) or analog phase-locked loops (PLL) are fed into a down-conversion mixer. While in [16] and [17], only one synthesizer generates the chirp, which is down-converted with a fixed frequency, in [18], the absolute bandwidth of two VCOs is added. Therefore, they each generate a chirp inside their own PLL. However, this requires the design of two individual PLLs and their synchronized control to generate chirps in opposite directions.

In contrast, the PLL architecture utilized in this article directly stabilizes the mixer's output. Therefore, two tuning voltages are generated inside one shared PLL. This architecture is illustrated in Fig. 1. It significantly reduces the hardware and simulation effort, as only one PLL is needed to generate the ultra-wideband (UWB) frequency chirp. This approach has been published as a patent in [19] and was successfully implemented in a previous version of this paper, presented at the European Microwave Conference, and published in its proceedings [20]. It presents the successful implementation of a PLL exceeding the UWB based on this concept. This frequency range was selected due to the UWB's demanding relative bandwidth of over 109% at a maximum frequency stabilizable with commercially available PLLs.

This article extends that work by investigating the theoretical limitations of conventional, single VCO synthesizers and the benefits of this approach toward relative bandwidth and VCO gain linearity. The conducted measurements prove the validity of those considerations and are extended to include the open-loop phase noise of the equivalent VCO, as well as measurements of wideband frequency chirps. However, to first establish the necessity of the PLL architecture, we investigate the limitations of conventional, single VCO synthesizers in the "Bandwidth limitations with a single VCO" section. Subsequently, we explain the proposed novel PLL architecture in detail while providing analytical considerations for improved VCO gain linearity in the "Novel PLL architecture" section. The section on the "Monolithic Microwave Integrated Circuit (MMIC)" presents the realized chip required to prove the validity of those considerations. It is then utilized to achieve what is presented in the "Measurement results" section.

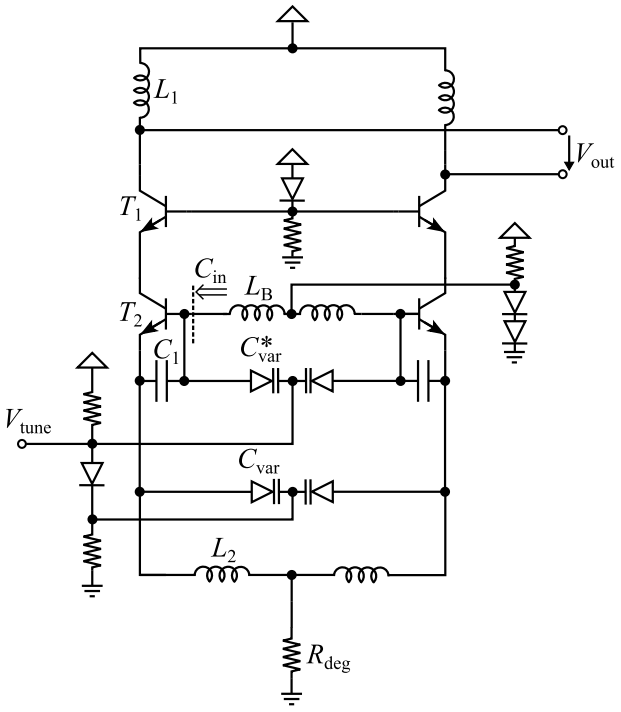

Figure 2. Schematic of the utilized VCO architecture. The two varactors of the Colpitts-Clapp approach increase the relative bandwidth, while still remaining limited when using a single VCO.

Bandwidth limitations with a single VCO

The Colpitts-Clapp architecture utilized for the two required VCOs is presented in Fig. 2. It was introduced in [21] and has since been used for several wideband VCOs in different technologies [22, 23]. Compared to the cross-coupled topology of [9], it was chosen due to its more stable and higher output power, which is required in the proposed concept to drive the down-conversion mixer.

Relative bandwidth limitations

When first neglecting C^*_{var}, the resulting, fundamental Colpitts architecture is based on a series resonant circuit formed by the input capacitance C_{in} and the base inductance L_B at the base of the transistor T_2 [21]. The input capacitance can be modified using a varactor and changing the applied tuning voltage V_{tune} to control

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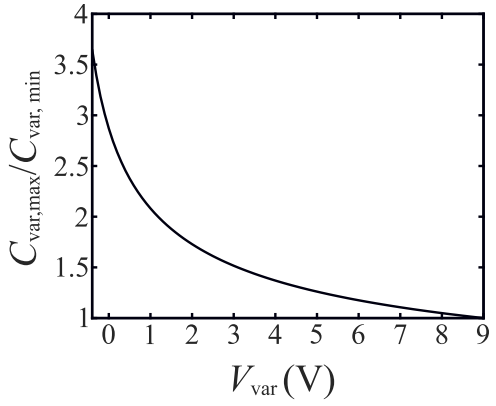

Figure 3. Dependency of the varactor capacitance C_{var} on the varactor voltage V_{var}. In the utilized technology, the capacitance variation reaches a ratio of 3.6:1, including a slight forward biasing.

the output frequency. To maximize the relative bandwidth, C_{in} would ideally equal the varactor's capacitance C_{var}. The oscillation frequency is then given by:

$$f_{osc} = \frac{1}{2\pi \cdot \sqrt{L_B C_{var}}}. \tag{3}$$

By inserting (3) in (2), the relative bandwidth achievable in dependency of the tuneable range of the varactor can be calculated as:

$$B_{rel} = \frac{2 \cdot \left(\sqrt{C_{var,max}/C_{var,min}} - 1\right)}{\sqrt{C_{var,max}/C_{var,min}} + 1}. \tag{4}$$

To be able to estimate the maximum achievable relative bandwidth, the simulation results for the $C_{var,max}/C_{var,min}$ of the used varactor are shown in Fig. 3. It has to be noted that the realizable variation increases significantly if the varactor is biased in forward direction. In the case of Fig. 3, a conservative voltage proven in previous designs was chosen, to reach a varactor capacitor variation of 3.6:1. Therefore, with the help of (4), the maximum relative bandwidth utilizable in this process equals 62.6%. However, as presented in [21], C_{in} does not equal C_{var}, as ideally assumed in (3), but also includes a capacitance in series C_s and, in parallel, C_p, respectively. With their weak dependency on V_{tune}, they additionally reduce the achievable tuning range. Therefore, to decrease this effect, [21] proposes using a second varactor C^*_{var}, increasing the total variable capacitance. This changes (3) to a more sophisticated version:

$$f_{osc} = \frac{1}{2\pi \cdot \sqrt{L_B}} \cdot \left(\frac{C_{var} \cdot C_s}{C_{var} + C_s} + C_p + C^*_{var}\right)^{-\frac{1}{2}}, \tag{5}$$

as is given in [22], where this architecture was used in the same technology to achieve a relative bandwidth of 40.24% and 38.62% in the E- and W-band, respectively. Both designs, therefore, exceed the relative bandwidth of their corresponding waveguide frequency bands. In [9], those relative bandwidths are significantly surpassed with a cross-coupled VCO. This is partly thanks to a $C_{var,max}/C_{var,min}$ of 8.5 in that technology, allowing for a theoretical value of 98%. Combined with smaller parasitic capacitances at the center frequency of 10.8 GHz, this design achieved a relative bandwidth of 80% in measurements.

However, none of these state-of-the-art VCOs can cover the relative bandwidth of the UWB with its 109%, let alone coming close to the maximum of 200% as some YTOs do. To further examine why, we determine the necessary tuneable capacity range of the varactor for a given B_{rel}. Solving (4) for $C_{var,max}/C_{var,min}$ provides

$$\frac{C_{var,max}}{C_{var,min}} = \left(\frac{B_{rel} + 2}{B_{rel} - 2}\right)^2. \tag{6}$$

Achieving a relative bandwidth of 176%, as presented in this article, C_{var} would therefore require a tuneable range of $C_{var,max}/C_{var,min} \approx 245$. This exceeds the value of the technology used in [9] by a factor of 29 while still neglecting the aforementioned parasitics. Therefore, this clearly illustrates the infeasibility of covering such a relative bandwidth with a single VCO.

PLL loop gain variation

If we move from the design of the broadband VCO as a single component to its integration inside of a frequency synthesizer, another challenge arises. Therefore, the PLL's filter bandwidth is chosen to optimize phase noise performance at a specific design frequency. At this design frequency, the PLL exhibits a fixed loop gain K_{PLL} given by:

$$K_{PLL} = \frac{K_{VCO} K_{PFD}}{N}. \tag{7}$$

It depends on the PFD gain K_{PFD}, the divider value N, and critically, the VCO gain K_{VCO}. Even for VCOs with a continuous tuning range, their proportionality between the tuning voltage and output frequency can be nonlinear. Therefore, the K_{VCO} varies significantly over the tuning voltage, especially for ultra-wideband VCOs. To assess this analytically, (3) can be expanded to include the varactor capacitances' dependency on the tuning range. By excluding the parasitics of (5) and modeling the varactor's capacitance as the diode's junction capacity in dependency of the tuning voltage V_{tune} and diffusion voltage V_{diff},

$$f_{osc} = \frac{1}{2\pi \cdot \sqrt{L_B \cdot \frac{C_{var,max}}{\sqrt{1 + \frac{V_{tune}}{V_{diff}}}}}}, \tag{8}$$

is obtained, corresponding to the VCO's tuning curve. As K_{VCO} corresponds to the derivative of this equation, it equals

$$K_{VCO} = \frac{1}{8\pi \cdot V_{diff} \cdot \sqrt{L_B C_{var,max} \left(\sqrt{1 + \frac{V_{tune}}{V_{diff}}}\right)^3}}. \tag{9}$$

The VCO gain, therefore, decreases with a proportionality of $V_{tune}^{-3/4}$. For the previously discussed VCO with the highest relative tuning range, this variation reaches a vast ratio of 30:1 [9]. Furthermore, it is aggravated by the variation of the PLL's divider value N, also included in (7). This effect is further enhanced as its reciprocal decreases simultaneously to K_{VCO} when generating higher frequencies. Therefore, the loop filter's realized bandwidth and phase margin vary greatly with output frequency during frequency synthesis [24, 25]. Thus increasing phase noise and, in the worst case,

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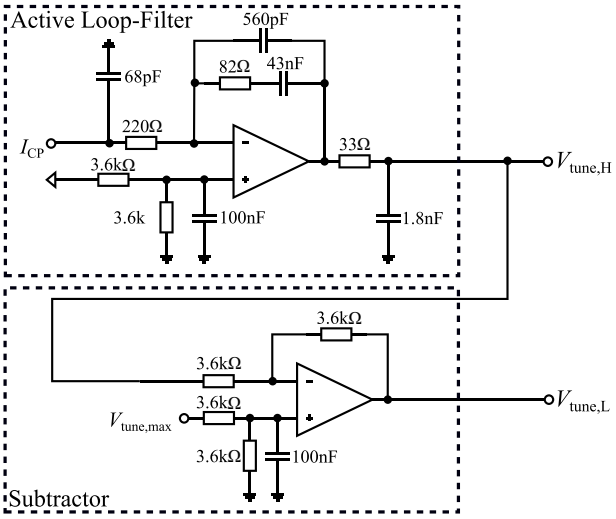

Figure 4. The presented loop filter generating the tuning voltages for both VCOs. The conventional active loop filter generates $V_{tune,H}$, while an additional subtractor generates $V_{tune,L}$ working in opposite direction.

introducing stability problems. For this reason, several loop gain stabilization methods exist that try to compensate for VCO gain variation [26, 27].

Novel PLL architecture

With the limitations and challenges of single VCO frequency synthesizers clearly defined, we can look at the solutions the state of the art offers. They are based on subtracting two different frequency sources to increase the relative tuning range significantly. In [16], the frequency chirp with the desired absolute bandwidth is generated by a DDS. Subsequently, a second oscillator is stabilized separately to generate a fixed frequency. It is used to down-convert the chirp generated by the DDS to achieve the same absolute bandwidth at a lower center frequency for a higher relative bandwidth. The same concept is utilized in [17], replacing the DDS with an additional analog PLL. Again, the bandwidth generated by the one PLL is down-converted by a fixed frequency to increase relative but not absolute bandwidth. However, since these concepts each use two different frequency sources, it is also possible for both to be tuneable to also add their absolute bandwidths. This was demonstrated in [18], where two oscillators with different center frequencies are tuned in opposite directions inside their own PLL, respectively. However, as suggested in [19], directly stabilizing the mixer's output should synthesize the desired frequency immediately, significantly reducing the necessary hardware and implementation effort. This concept is illustrated in Fig. 1. Therein, the lower center frequency VCO_L's signal is subtracted from VCO_H's higher frequency signal. To add their respective bandwidths, the tuning voltage of VCO_L has to be inverted for the two VCOs to chirp in opposite directions. Therefore, the loop filter architecture presented in Fig. 4 is proposed. While a traditional active B filter [28] provides the tuning voltage $V_{tune,H}$ for VCO_H, a subtractor also inverts it to generate $V_{tune,L}$ via the equation:

$$V_{tune,L} = V_{tune,max} - V_{tune,H}. \tag{10}$$

Therefore, when VCO_H is at its highest frequency, VCO_L is at its lowest, and vice versa. Should the VCO require a minimum

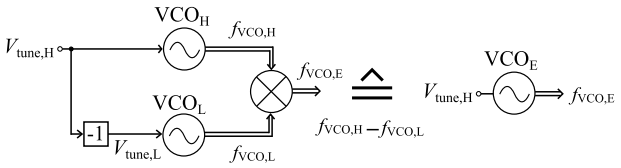

Figure 5. Concept of the two VCOs with the proposed loop filter behaving as one equivalent VCO. The validity of this concept eases the required simulation effort significantly.

tuning voltage for oscillation, this $V_{tune,min}$ also must be included in (10). Additionally, the frequency of both VCOs depends solely on a single tuning voltage that dictates the output frequency of the presented PLL architecture. Therefore, it is possible to summarize the complete architecture as an equivalent VCO outputting a frequency $f_{VCO,E}$ given by:

$$f_{VCO,E} = f_{VCO,H} - f_{VCO,L}, \tag{11}$$

in dependency of a single tuning voltage $V_{tune,H}$, as described in Fig. 5.

Subsequently, to analyze $f_{VCO,E}$ analytically, $f_{VCO,H}$ in dependency of $V_{tune,H}$ is modeled by:

$$f_{VCO,H} = \frac{1}{2\pi \cdot \sqrt{L_{B,H} \cdot \frac{C_{var,max,H}}{\sqrt{1+\frac{V_{tune,H}}{V_{diff}}}}}}, \tag{12}$$

as described in (8). Additionally, $V_{tune,H}$ receives a negative sign for VCO_L by inserting (10) in (8) to get:

$$f_{VCO,L} = \frac{1}{2\pi \cdot \sqrt{L_{B,L} \cdot \frac{C_{var,max,L}}{\sqrt{1+\frac{V_{tune,max}-V_{tune,H}}{V_{diff}}}}}}. \tag{13}$$

A distinction is made between the base inductance $L_{B,H}$ and $L_{B,L}$, as well as the maximum varactor capacitance $C_{var,max,H}$ and $C_{var,max,L}$ of VCO_H and VCO_L, respectively. Additionally, we summarize those constants as the minimum oscillation frequencies $f_{m,H} = \left(2\pi\sqrt{L_{B,H}C_{var,max,H}}\right)^{-1}$ for VCO_H and $f_{m,L} = \left(2\pi\sqrt{L_{B,L}C_{var,max,L}}\right)^{-1}$ for VCO_L, respectively. This results in a concise equation for the frequency of the equivalent VCO when inserting (12) and (13) in (11):

$$\begin{aligned} f_{VCO,E} =& f_{m,H} \cdot \sqrt[4]{1 + \frac{V_{tune,H}}{V_{diff}}} \\ & - f_{m,L} \cdot \sqrt[4]{1 + \frac{V_{tune,max} - V_{tune,H}}{V_{diff}}}. \end{aligned} \tag{14}$$

The derivation of which equates to:

$$\begin{aligned} K_{VCO,E} = \frac{1}{4V_{diff}} \cdot \Bigg(& f_{m,H} \cdot \left(1 + \frac{V_{tune,H}}{V_{diff}}\right)^{-\frac{3}{4}} \\ & + f_{m,L} \cdot \left(1 + \frac{V_{tune,max} - V_{tune,H}}{V_{diff}}\right)^{-\frac{3}{4}} \Bigg). \end{aligned} \tag{15}$$

To visualize these results and proportionalities, Fig. 6 plots (8) and (9), as well as (14) and (15), respectively. Therein shows that the equivalent VCO based on the novel PLL architecture offers a higher relative tuning range based on frequency subtraction combined with a more linear tuning curve. Thereby, based on analytical

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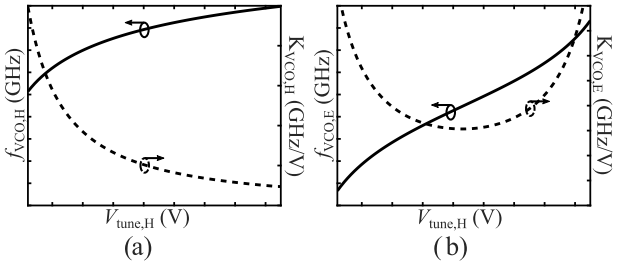

Figure 6. A plot of the proportionalities described by the analytical considerations regarding the frequency and VCO gain of (a) a single VCO and (b) the proposed architecture. The curves plot the corresponding equations (8) and (9), as well as (14) and (15), respectively.

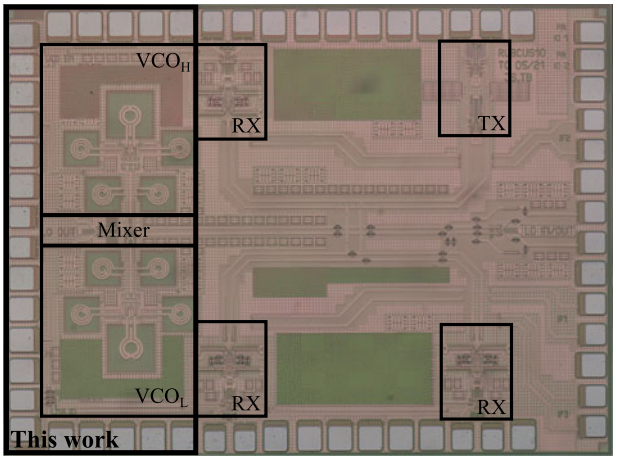

Figure 7. Photograph of the realized MMIC containing the two VCOs and the down-conversion mixer. The TX- and RX-channels are not part of this work, which focuses on the frequency generation.

considerations, the novel PLL architecture can solve both problems outlined in "Bandwidth limitations with a single VCO".

Monolithic Microwave Integrated Circuit (MMIC)

To verify those promising analytical considerations in practice, we designed an MMIC including the necessary components to implement the novel PLL architecture. A photograph of which is presented in Fig. 7. The MMIC also includes one transmit and three receive channels that are not further discussed, as this work focuses on the frequency generation.

Regarding the necessary components, the two RF-VCOs are visible on the left. They are based on the schematic presented in Fig. 2 and therefore utilize the Colpitts-Clapp architecture. As explained in the "Bandwidth limitations with a single VCO" section and described by (5), this increases the variable capacity to maximize the tuning range of the individual VCOs. Specifically, the higher f_c VCO$_H$ covers a frequency range of 32–41 GHz and is based on the design presented in [29]. Its measured tuning curve and calculated K_{VCO} are presented in Fig. 8. In principle, VCO$_L$ utilizes the same architecture while using slightly larger integrated inductances and varactor sizes to decrease its center frequency. Its determined tuning curve covering a range of about 28–36 GHz and K_{VCO} are also presented in Fig. 8. They both strongly present the proportionalities described in Fig. 6(a). During the design process, we aimed to create no overlap between the two VCOs, while minimizing their

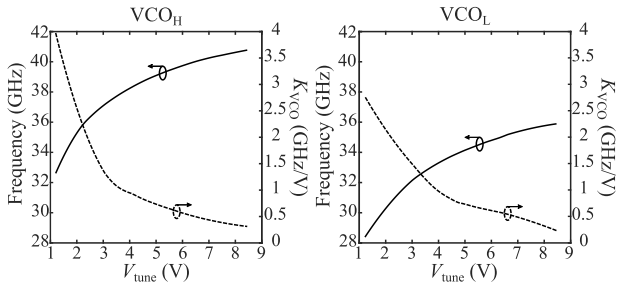

Figure 8. Measured tuning curve and calculated K_{VCO} of VCO$_H$ and the calculated tuning curve and K_{VCO} of VCO$_L$.

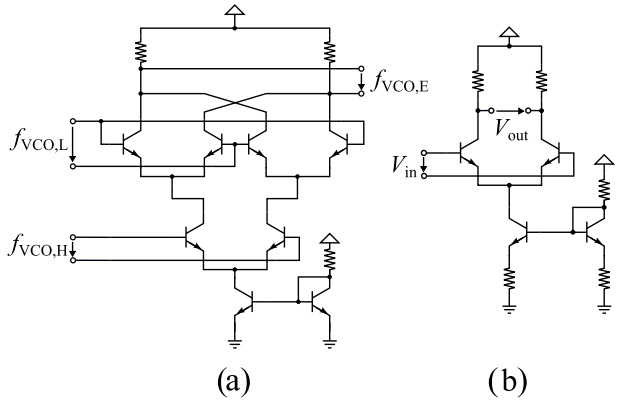

Figure 9. Schematic of the utilized (a) down-conversion mixer and (b) output buffer.

separation to maximize relative bandwidth. The remaining overlap of less than 4 GHz can be reduced in the future to increase the signal generation's absolute tuning range.

As the presented concept generates several different frequencies, intermodulation can be a concern. Advantageously, the second harmonics of $f_{VCO,H}$ and $f_{VCO,L}$ are canceled out, respectively, due to the differential circuit topology. However, as the upper sideband is only attenuated by the first-order low-pass filter of the mixer's load, its intermodulation products should be considered. Therefore, to reduce the main distortion possible, which corresponds to the minimum sum of $f_{VCO,H}+f_{VCO,L}$ mixing with the maximum available frequency of VCO$_H$ $f_{VCO,H,max}$ the condition presented in [18]:

$$f_{L,min} + f_{H,min} - f_{H,max} > f_{H,max} - f_{L,min}, \tag{16}$$

has been fulfilled. Additionally, this is an overfulfilled condition, as $f_{H,min}$ never occurs simultaneously to $f_{L,min}$ and $f_{H,max}$, by definition.

The frequency mixer, necessary for the down-conversion, is realized as a Gilbert cell connected to a resistive load, as can be seen in Fig. 9(a). In conjunction with the parasitic capacitances of the transistors, the resulting RC-load attenuates the unwanted sideband. Additionally, the differential amplifier of Fig. 9(b) is used to increase the output power to approx. 0 dBm while acting as an additional low-pass filter. The resulting output power is therefore high enough to act as the input signal of commercially available PLLs. This should be the case for a large span of temperatures as the VCOs deliver a stable output power, as shown in Fig. 10.

To validate those components working together to form the equivalent VCO, the bare die of the MMIC was mounted on a

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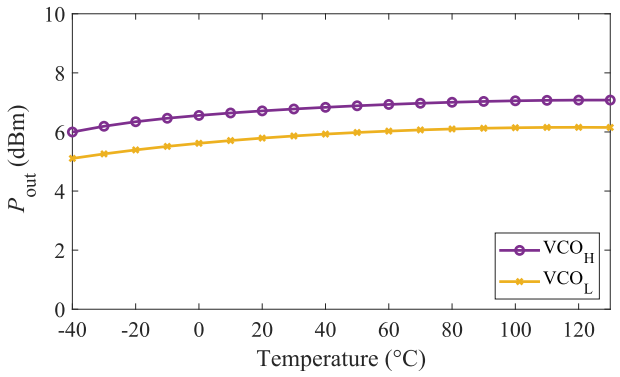

Figure 10. Simulated output power of VCO_H and VCO_L in dependency of temperature.

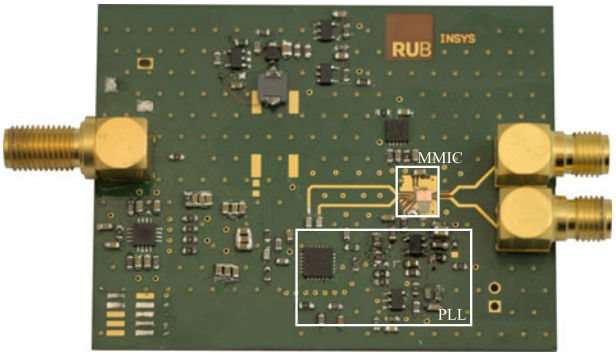

Figure 11. Photograph of the measurement PCB.

printed circuit board (PCB), which is presented in Fig. 11. The PCB provides the supply voltage, the reference frequency and contains the PLL chip and the loop filter. The ADF4169 by Analog Devices was chosen as the PLL chip. With its RF-bandwidth of 13.5 GHz, it can stabilize the equivalent VCO up to its maximum frequency.

To design the loop filter generating $V_{\text{tune,H}}$, available simulation tools for conventional, single-loop PLLs can be used. By doing so, a loop bandwidth of 389 kHz and a phase margin of 67° were chosen. The subtractor's resistor values were matched to the op-amp's noise voltage and current for minimum noise power density.

Measurement results

Firstly, the board was used to measure the tuning curve of the free-running, equivalent VCO. It is illustrated in Fig. 12, next to the frequencies of the individual VCOs, all in dependency of $V_{\text{tune,H}}$. To prevent the aforementioned overlap of the two VCOs, $V_{\text{tune,H}}$ is limited to a minimum of 2 V. Thereby, the tuning curve follows the proportionality described analytically by (14), as illustrated in Fig. 6(b). The same also applies to the presented VCO gain variation of the equivalent VCO described by (15). It is therefore compensated by the novel PLL architecture as anticipated by the analytical considerations. Quantitatively, the $K_{\text{VCO,H}}$ variation of 12.84:1 and the $K_{\text{VCO,L}}$ variation of 12.07:1 are thereby reduced to only 2.33:1. Additionally, in similarity to [26], the maximum of $K_{\text{VCO,E}}$ at the highest frequency, reduces the impact of the $1/N$ also included in the K_{PLL} described by (7).

Secondly, the free-running VCO's phase noise is measured by using a phase noise and signal source analyzer (R&S FSWP).

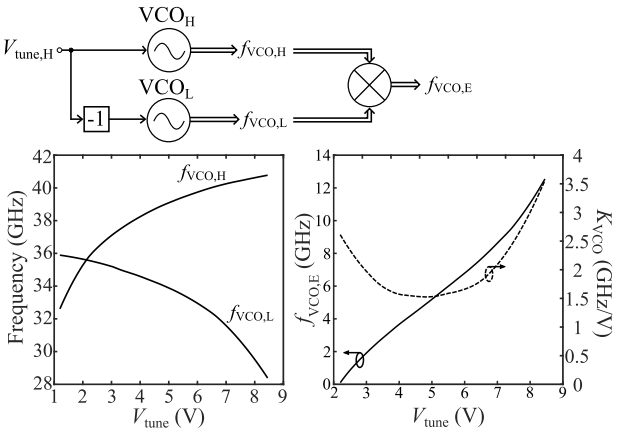

Figure 12. The measured tuning curve and K_{VCO} of the equivalent VCO. The calculated K_{VCO} varies less than for a single VCO. Therefore, the broadband VCO is easier to stabilize inside a PLL.

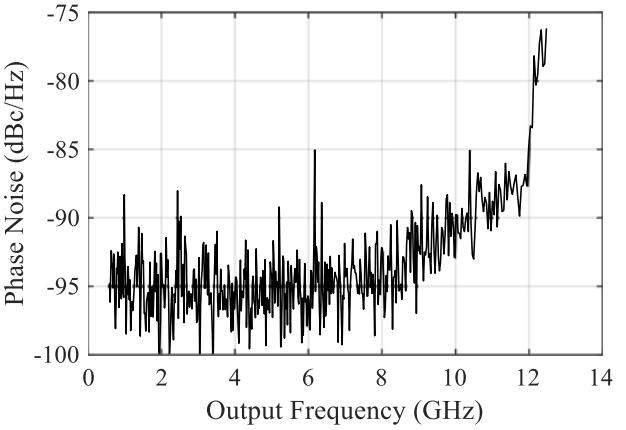

Figure 13. Measured open-loop phase noise of the equivalent VCO at an offset frequency of 1 MHz in dependency of output frequency. This phase noise includes the noise of the two RF-VCOs, the subtractor and the mixer.

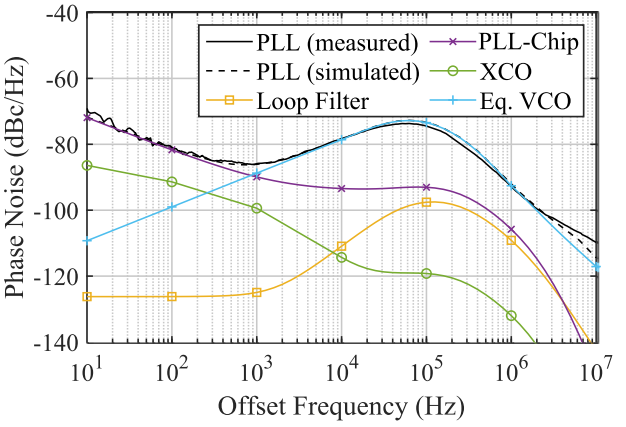

Figure 14. Measured and simulated closed-loop phase noise at $f_s = 8$ GHz. The simulated contributions are calculated based on measurements of the individual components or their corresponding data sheets.

Therefore, it was connected via SMA to a second output of the signal source opposite of the one used as the PLL's input. The result of the phase noise over output frequency at an offset frequency of 1 MHz is illustrated in Fig. 13. It is, as expected, higher than

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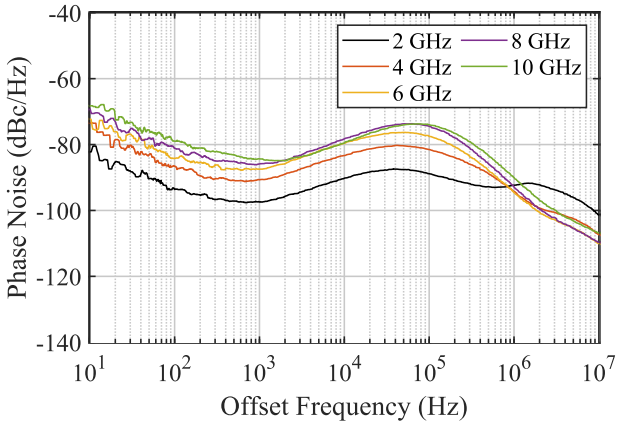

Figure 15. Closed-loop phase noise measurements of multiple output frequencies. The realized loop bandwidth and phase margin are very consistent for the large variance in output frequency thanks to the loop gain compensation of the presented concept.

fundamental VCOs at the generated frequencies, as it corresponds to the sum of the two VCOs at higher frequencies. However, for applications such as the discussed snow radar in [8], the increased relative bandwidth brings resolution and penetration depth advantages that outweigh higher phase noise. Its signal generation, as well as all the approaches presented in [16–18] also exhibit the added phase noise of two oscillators. However, regarding hardware and simulation efforts, this concept offers significant improvements. Additionally, as this synthesizer was implemented to prove the validity of the concept, phase noise can be optimized in the future, by carefully choosing the center frequencies and bandwidths of the respective RF-VCOs.

Additionally, the phase noise of the stabilized VCO is measured, with the FSWP's programmable signal source acting as the PLL's reference. The results are depicted in Fig. 14 at a carrier frequency of 8 GHz. Moreover, the PLL's components' individual noise contributions are also presented. The commercial PLL-chip dominates the phase noise up to an offset frequency of approximately 1 kHz. From there on, the VCO dominates. It is to be noted that based on the frequency down-conversion and the resulting increase of the relative tuning range, the minimum frequency can, in this case, be arbitrarily low. During stabilization, a limit is introduced based on the minimum divider value of the PLL. As described in [30], a higher reference can simultaneously improve a PLL's phase noise and settling time. Reducing the reference frequency to reach the lowest desired output frequency should, therefore, be avoided to not increase phase noise and settling time, as the latter would result in slower sweep times. In this case, the commercially available PLL chip requires a high minimum divider value of 75 offered with the 8/9-prescaler. Other programmable frequency dividers, such as the 12 of [31] utilized in the aforementioned [30], offer lower values, even going down to one as presented in [32].

Overall, the measured and simulated phase noise matches each other almost perfectly. This validates the aforementioned simulation method based on the equivalent VCO with single VCO simulation tools. Therefore, the synthesizer's implementation is successfully simplified from having to design multiple frequency sources individually to one synthesizer with nearly unlimited relative bandwidth.

Furthermore, the stabilized phase noise is measured at different carrier frequencies, with the results illustrated in Fig. 15. The in-band phase noise variation corresponds to the expected $20\log(10\,\text{GHz}/2\,\text{GHz}) = 14\,\text{dB}$. Although the output frequency is varied by this factor of 5, the loop bandwidth stays reasonably constant. In conventional single VCO synthesizers, the deviation from the desired loop bandwidth and phase margin is conventionally significantly higher [25]. This highlights the advantage of the proposed concept, reducing the VCO gain variation to only 2.33:1.

Finally, measurements of frequency chirps generated by the synthesizer were conducted. Therefore, a R&S FSW85 with a maximum analysis bandwidth of 8.3 GHz was connected to the synthesizer's output. However, in the generated frequency band, the analysis bandwidth of the FSW85 is reduced to 4.4 GHz. Therefore, the realizable frequency range is illustrated by three individual chirps with different prescalers and an individual bandwidth of 4.4 GHz, allowing for some overlap. The spectrograms of those are illustrated in Fig. 16. Additionally, the tuning voltages $V_{\text{tune,H}}$ and $V_{\text{tune,L}}$ were probed with an oscilloscope and are depicted in the

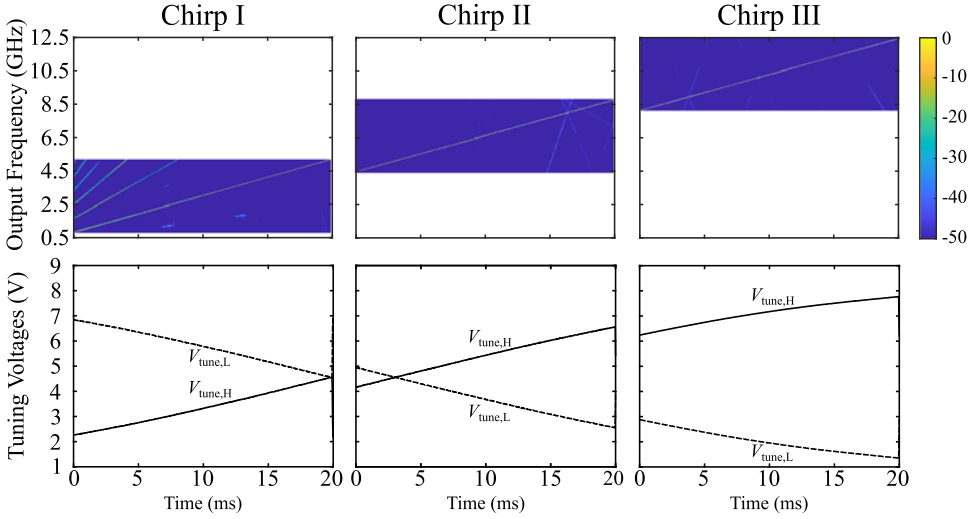

Figure 16. Spectrogram of three frequency chirps, covering a frequency range of 0.8–12.5 GHz. Additionally, the tuning voltages $V_{\text{tune,H}}$ and $V_{\text{tune,L}}$ are also presented, which generate those chirps by working in opposite directions inside of one PLL.

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Table 1. State-of-the-art FMCW-synthesizers with high relevance to this work

Ref.	This work	[24]	[14]	[16]	[17]	[18]
Year	2023	2019	2019	2017	2016	2020
Frequency range (GHz)	0.8[a]–12.5	6–15	3–23	2–18	0.4–6	6–46
Max. continuous tuning range (GHz)	11.7[a]	9	10.5	16	5.6	40
Relative bandwidth	176%[a]	82%	74%	160%	175%	154%
Output frequency (GHz)	8	11.5	7	–	3.2	–
PN @ 10 kHz (dBc/Hz)	−78	−85[b]	–	–	−94[b]	–
PN @ 1 MHz (dBc/Hz)	−94	−109[b]	−111[b,c]	–	−95[b]	–
Active oscillator chip area (mm^2)	0.402	0.252	0.554	–	–	0.399
Oscillator power consumption (mW)	138.6	20	300	–	–	–
PLLs + DDSs	1	1	1	2	2	2

[a]The 200% offered by the equivalent VCO is only limited by the chosen PLL chip's minimum divider value and integer range.
[b]Normalized to an output frequency of 8 GHz.
[c]Open-loop VCO phase noise.

same figure. In Chirp I, the spectrogram includes harmonics of the desired chirp, partly due to an intermediate amplifier and the single-ended input of the FSW85. Chirps II and III only include the desired frequency chirp, apart from some parasitics folding into the limited analysis bandwidth at approximately −40 dB. Finally, the tuning voltages illustrate the presented concept working as intended to generate the respective chirps with $V_{\mathrm{tune,H}}$ and $V_{\mathrm{tune,L}}$ going in opposite directions simultaneously.

Compared to recently published FMCW-synthesizers of Table 1, the works presented in [14, 24] achieve better phase noise using a single VCO or a switchable VCO bank, respectively. Using two VCOs and subtracting their signals is, as explained above, not beneficial regarding phase noise. This is partly because designing the VCOs for higher frequencies increases their individual phase noise by 20 dB per decade [33]. With a singular VCO at the fundamental frequency however, the relative bandwidth is limited. Using the switchable VCO bank of [14], a broader spectrum of frequencies can be covered, e.g., for pulse-based applications in the UWB. However, the full bandwidth cannot be utilized to generate coherent FMCW chirps.

The results presented in [17, 18] both use two VCOs stabilized by an individual analog PLL, respectively. Therefore, increasing the area and power consumption by an additional PLL chip at least. Additionally, the design effort is more than doubled based on the necessity of two loops that work synchronously against each other. Most notably, the presented system is the only one achieving a relative bandwidth of >100% with a single PLL or DDS. With the approach presented in this work, such a system's hardware and design effort could be reduced to one PLL. Finally, to utilize the concept for the frequencies covered in [18], an additional prescaler output can be used, as is common practice with single RF-VCOs.

Conclusion

In this article, we successfully implemented an architecture to generate relative bandwidths of >100% within a single PLL. Therefore, a conventional active loop filter was expanded via an op-amp subtractor to generate two opposing tuning voltages for two VCOs at different center frequencies. The topology forms an equivalent VCO with a relative bandwidth of 200% at the mixer's output, which is stabilized directly while benefiting from the absolute bandwidths of both individual VCOs. Furthermore, analytical considerations and experimental validations have proven this concept's supplementary tuning curve linearization. Thereby, a maximum VCO gain variation of 12.84:1 for one individual VCO was reduced to just 2.33:1 for the equivalent VCO. All in all, the presented concept offers relative bandwidths previously requiring two individual synthesizers in just one, to significantly reduce hardware and implementation effort compared to the state of the art.

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Competing interests. None declared.

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