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X-band T/R-module front-end based on GaN MMICs

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Amplifiers for the next generation of T/R modules in future active array antennas are realized as monolithically integrated circuits (MMIC) on the basis of novel AlGaN/GaN (is a chemical material description) high electron mobility transistor (HEMT) structures. Both low-noise and power amplifiers are designed for X-band frequencies. The MMICs are designed, simulated, and fabricated using a novel via-hole microstrip technology. Output power levels of 6.8 W (38 dBm) for the driver amplifier (DA) and 20 W (43 dBm) for the high-power amplifier (HPA) are measured. The measured noise figure of the low-noise amplifier (LNA) is in the range of 1.5 dB. A T/R-module front-end with mounted GaN MMICs is designed based on a multi-layer low-temperature cofired ceramic technology (LTCC).

Keywords: AlGaN/GaN, MMICs, T/R module, X-band

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I. INTRODUCTION

Active electronically scanned array (AESA) radars are increasingly being favored over conventional mechanically scanned systems. The achievable radar range of such an AESA radar is mainly determined by the output power and the noise figure of the antenna. Both properties can be improved using GaN technology. T/R modules are key elements in active phased-array antennas for radar and electronic warfare applications [1]. Inside these T/R modules two main building blocks are the amplifier chain in the transmit path and the low noise amplifier (LNA) in the receive path.

In most of today's T/R modules GaAs monolithically integrated circuit (MMIC) amplifiers are used with typical output power levels in the range of 5–10 W [2–4]. Higher output power levels, broader bandwidth, increased power-added efficiency (PAE) values, and higher operating voltages are advantages for performance improvement to meet future requirements. For these applications the use of amplifiers based on AlGaN/GaN is a very promising approach [5–8]. With the GaN technology, high-power amplifiers (HPAs) with higher output power compared to GaAs MMICs are already demonstrated [9–11]. With limited prime power and also limited cooling capacity, as often existing in military systems, another important parameter is the PAE of the amplifier. Due to the higher breakdown voltage of the GaN device compared to a GaAs device, the supply voltage can be significantly increased. This leads to an additional increase in efficiency on system level, because of lower losses in the power supply.

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Besides the noise figure performance the robustness against high input power overdrive is also a key issue for the receive path in a T/R module. The AlGaN/GaN technology with its high breakdown voltage is very well suited for robust low noise applications [12,13].

To satisfy these future needs, a T/R-module front-end composed of novel GaN MMICs and multi-layer packaging technology is designed.

In this paper the design and the achieved performance of single GaN MMIC amplifiers and of a whole T/R-module front-end based on these GaN MMICs are presented.

The MMIC and front-end design, simulation, and measurements are performed at European Aeronautic Defence and Space (EADS) Defence Electronics, Ulm. The wafer and MMIC fabrication is done at the Fraunhofer Institute of Applied Solid-State Physics, Freiburg.

II. GaN MMIC TECHNOLOGY AND MODELING

The AlGaN/GaN HEMT MMIC technology is based on multi-wafer growth of single heterojunction devices on 3-in s.i. SiC substrates by metal organic chemical vapor deposition (MOCVD). The 3-in HEMT technology uses electron-beam-defined gates with 0.25-μm gate-length including fieldplates for high-power operation.

The two-terminal breakdown voltages of the power HEMTs are $BV > 100$ V. Typical output power densities are beyond 5 W/mm at 10 GHz with an associated drain efficiency $\eta > 50\%$ at $V_{DS} = 28$ V for high efficiency operation. For low-noise operation, the AlGaN/GaN HEMTs yield a minimum noise figure of $NF < 0.8$ dB at $f = 10$ GHz and $V_{DS} = 10$ V.

After the front side processing, the full 3-in SiC wafer is thinned to 100 μm thickness and a via-hole back side process is applied. In Fig. 1 photo of the cross-section is shown. The via-

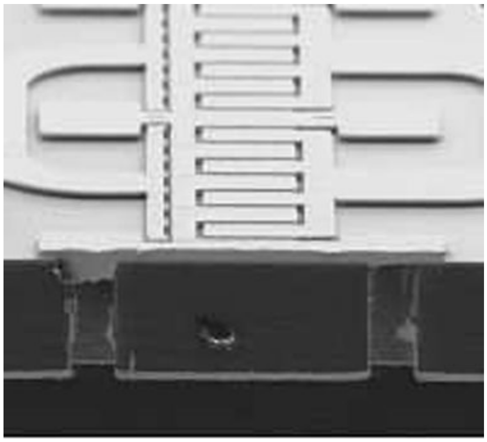

Fig. 1. Photo of the cross-section of a 100-μm-thick SiC wafer substrate, with a HEMT structure on the front side, via-holes, and back side metallization.

holes are well covered by metal from the back side, which ensures good grounding of the front side elements.

For the design a library of passive microstrip components is available, including all technology-specific elements like capacitors, resistors, and inductances. The large-signal GaN HEMT modeling is based on an in-house two-dimensional voltage-lag model to appropriately describe thermal effects and low-frequency dispersion, and their impact on gain and PAE [14].

III. DRIVER AMPLIFIER MMIC

The MMIC driver amplifier (DA) is designed as a two-stage amplifier with one transistor 8 × 60 μm gate-finger width in the first stage and one transistor 8 × 125 μm gate-finger width in the second stage (see Fig. 2). The amplifier is designed for an impedance of 50 ohm at the input and output ports and for operation in linear mode, not using the whole available output power of the transistor. One design objective was to provide enough input power for two HPAs in parallel configuration in the frequency band from 8 to 12 GHz. Although this amplifier will be used for operation in linear mode, the output matching is designed using harmonic balance simulation.

In Fig. 3 a whole wafer mapping of the measured small signal gain is shown. Comparing the simulated small signal gain at $V_{DS} = 15$ V with the on-wafer measurements, a very good compliance is observed. The uniformity is very good over the entire 3-in wafer.

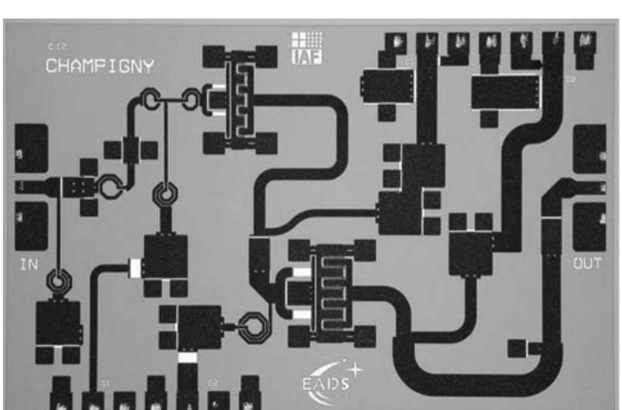

Fig. 2. Photo of a GaN DA MMIC chip. Chip size: 3 mm × 2 mm.

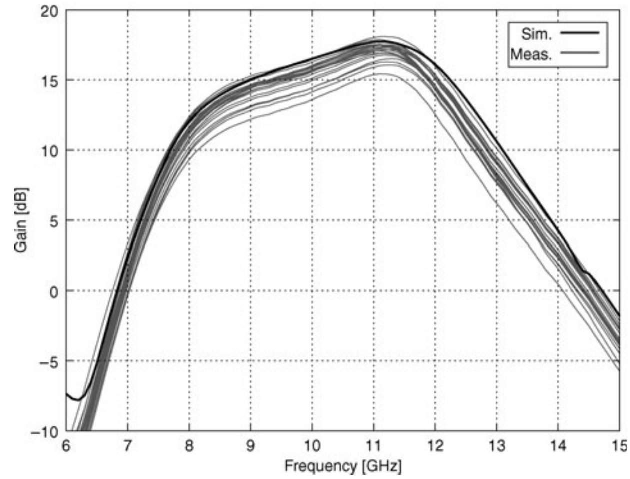

Fig. 3. Measured on-wafer small signal gain versus frequency of the GaN DA MMIC at $V_{DS} = 15$ V compared with the simulated performance.

The maximum measured output power is higher than 38 dBm while operating in saturation mode with up to 5-dB gain compression (Fig. 4). This output power leads to a power density of 7.4 W/mm at the transistor level. The measured saturated output power is even a little bit higher than that predicted by the simulation. The achieved output power is sufficient for driving one or two HPAs in the frequency range between 8.5 and 14 GHz, while operating the DA below the 1-dB compression point.

IV. HIGH-POWER AMPLIFIER MMIC

The MMIC HPA is designed as a two-stage amplifier based on four transistors with 8 × 125 μm gate-finger width in the second stage and two transistors with the same size in the first stage (see Fig. 5). The amplifier is designed for an impedance of 50 ohm at input and output ports. The output combiner is optimized for maximum output power in the frequency range from 8.5 to 11 GHz.

Previous intensive load-pull simulations have been performed to find the optimum load impedance for maximum output power.

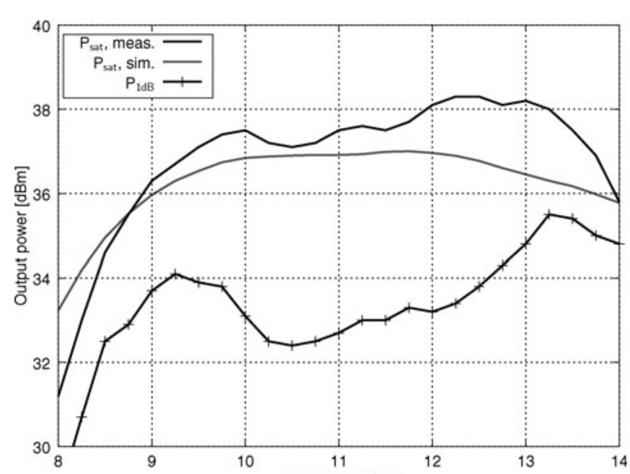

Fig. 4. Comparison of the simulated and measured output power versus frequency of the GaN DA MMIC at 1 dB gain compression and at saturation with $V_{DS} = 30$ V and $V_{GS} = -4.9$ V.

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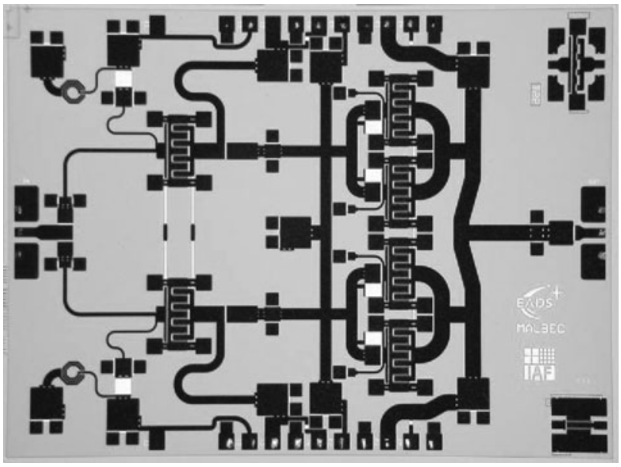

Fig. 5. Photo of a GaN HPA MMIC chip. Chip size: 4 mm × 3 mm.

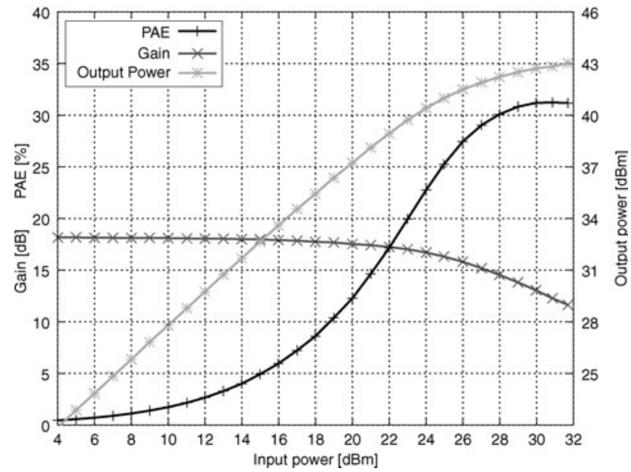

Fig. 7. Measured power performance of the GaN HPA MMIC at 11 GHz with $V_{DS} = 30$ V and $V_{GS} = -5$ V. $P_{max} = 43$ dBm and $PAE_{max} = 31\%$.

For electrical stabilization of the second-stage RC networks close to all transistor inputs are used. Odd-mode stability analysis has been performed for the parallel transistor structure. The first-stage transistors are stabilized by the gate bias circuits. The interstage network and the output combiner are optimized by electromagnetic simulations of distributed elements. An improved PAE performance is obtained by the application of second harmonic short networks at all gates of the second-stage transistors.

The on-wafer measurement of the small signal gain is indicating a slightly higher slope in the frequency range from 8 to 10 GHz compared to the result obtained by simulation (see Fig. 6). The uniformity over the entire wafer is again very good. The output power, gain, and PAE measurement results in pulsed mode are shown in Fig. 7.

Here, pulse conditions with 50 μs pulse length and 10% duty cycle are used for all pulsed measurements. The maximum measured output power is 20 W, when biased for class-AB operation. This output power leads to a power density of 5.7 W/mm at the transistor level. In this case the small signal gain is about 18 dB and the associated PAE value is 31%.

The small signal gain at $V_{DS} = 30$ V is higher than 15 dB over the whole frequency range from 8.5 to 11 GHz (see Fig. 8). The simulated small signal gain is more flat for lower frequencies, as already seen when operating the HPA with $V_{DS} = 15$ V. A part of the measured slope is linked to a weak input matching at frequencies around 8.5 GHz. More than 14 W output power is measured over a frequency range from 8.75 to 11.5 GHz. Again the simulated output power fits very well with the measurement results.

V. LOW-NOISE AMPLIFIER MMIC

For the designed MMIC LNA the same transistor size of 8 × 30 μm is used for the first and second stage (see Fig. 9). For this first iteration design the transistor layout was not optimized for low-noise operation. It is similar to the power transistor layout. The transistor size of the first stage is a trade-off between low-noise performance and large signal robustness.

To allow a simultaneous noise match and input match over a sufficiently broad bandwidth, an additional source inductance is used. The design model is based on small signal and noise parameter measurements of the transistor, without any inductive feedback.

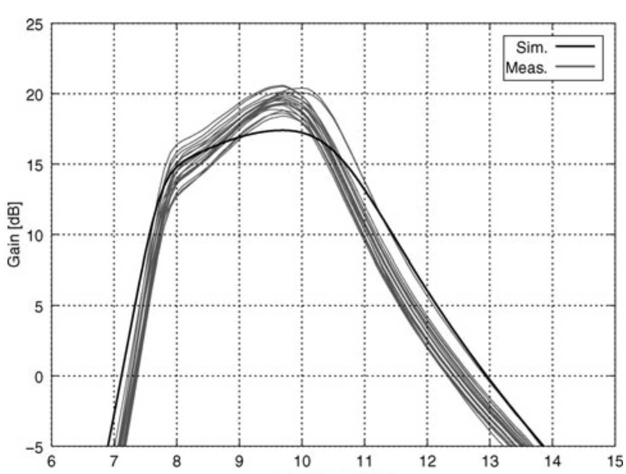

Fig. 6. Measured on-wafer small signal gain versus frequency of the GaN HPA MMIC at $V_{DS} = 15$ V compared with the simulated performance.

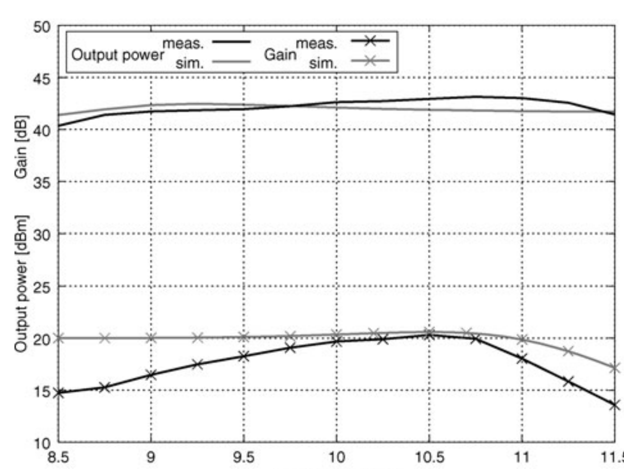

Fig. 8. Comparison of the simulated and measured saturated output power and small signal gain versus frequency of the GaN HPA MMIC. Bias point: $V_{DS} = 30$ V and $V_{GS} = -5.0$ V.

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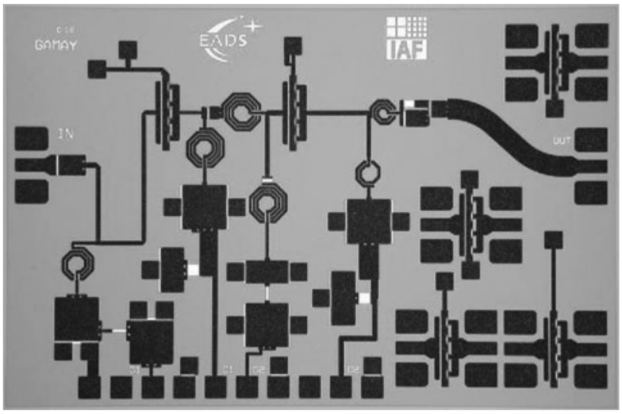

Fig. 9. Photo of a GaN LNA MMIC chip. Chip size: 3 mm × 2 mm.

For decoupling purpose, but also to increase the robustness [15], a resistor is used in the gate bias network. This LNA MMIC was originally designed for transistors with shorter gate length for the frequency range from 8 to 12 GHz [16]. Using a new transistor geometry a shift to lower frequencies occurred.

Taking into account the new transistor model a gain between 15 and 17 dB is simulated in the frequency range from 6.5 to 10 GHz. The expected noise figure is about 1.5 dB.

Again a very good agreement between simulation and measurement of the small signal gain exists (see Fig. 10). The shape of the frequency response is well predicted through the simulation. The average measured gain is about 1 dB higher than the simulated gain.

In Fig. 11 the simulated and measured noise figure of the GaN LNA MMIC is shown. The obtained noise figure is very close to the expected one over the whole frequency band. The minimum noise figure is only about 1.45 dB. For frequencies up to 10.5 GHz the noise figure of this GaN LNA is only 0.5 dB worse than the normally used GaAs LNA [17].

Besides the good noise performance the behavior of LNA with large input power signals is very important for this type of LNA. The saturated output power of the LNA is about 26.5 dBm (see Fig. 12). First robustness tests have been performed up to 6 W input power. At this input power level the LNA is about 27 dB in compression.

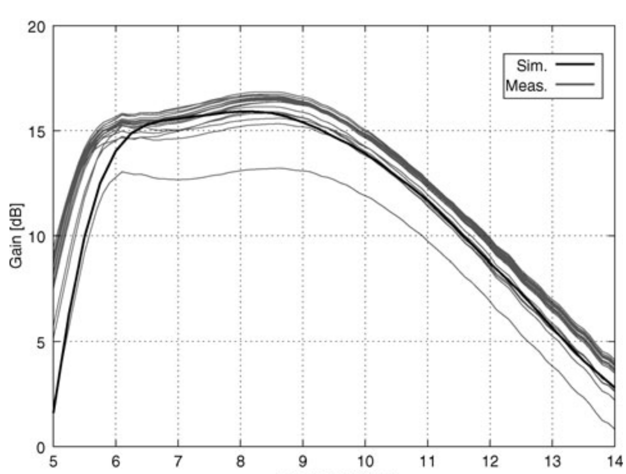

Fig. 10. Measured on-wafer small signal gain versus frequency of the GaN LNA MMIC at $V_{DS} = 15$ V compared with the simulated performance.

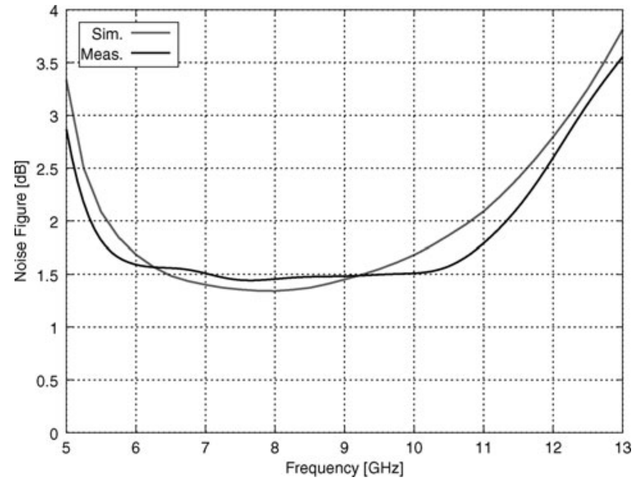

Fig. 11. Comparison of the simulated and measured gain and noise figure versus frequency of the GaN LNA MMIC with $V_{DS} = 15$ V and $V_{GS} = -2.2$ V. $NF_{min} = 1.45$ dBm.

VI. T/R-MODULE FRONT-END

For the front-end a multi-layer low-temperature cofired ceramic (LTCC) substrate is used. After obtaining first experience with an amplifier chain on LTCC with GaN MMICs [17] some modifications are realized. In Fig. 13 the completely assembled new front-end is shown.

One big challenge is the thermal situation with these GaN MMICs having a very high-power density compared to today's state-of-the-art GaAs MMICs.

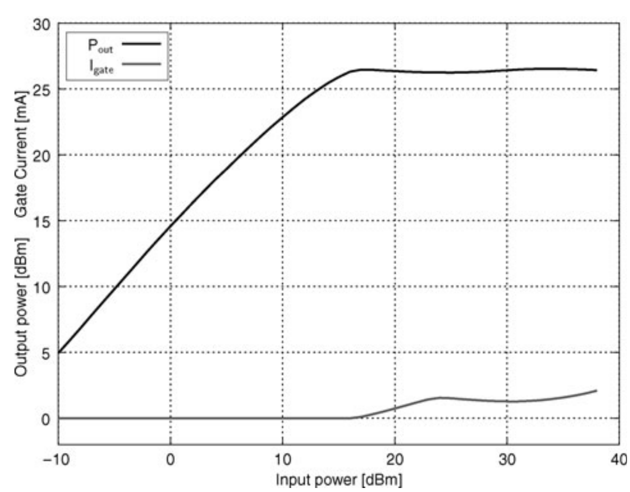

Fig. 12. Measured output power and gate current versus input power of the GaN LNA MMIC. Bias Point: $V_{DS} = 15$ V and $V_{GS} = -2.2$ V.

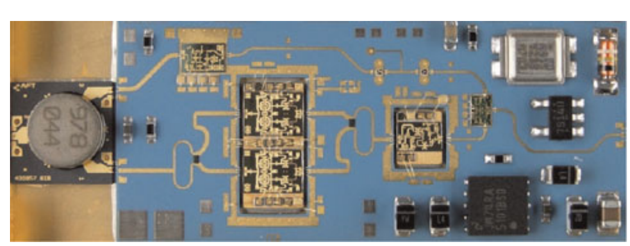

Fig. 13. Photo of a T/R-module front-end with GaN MMIC chips.

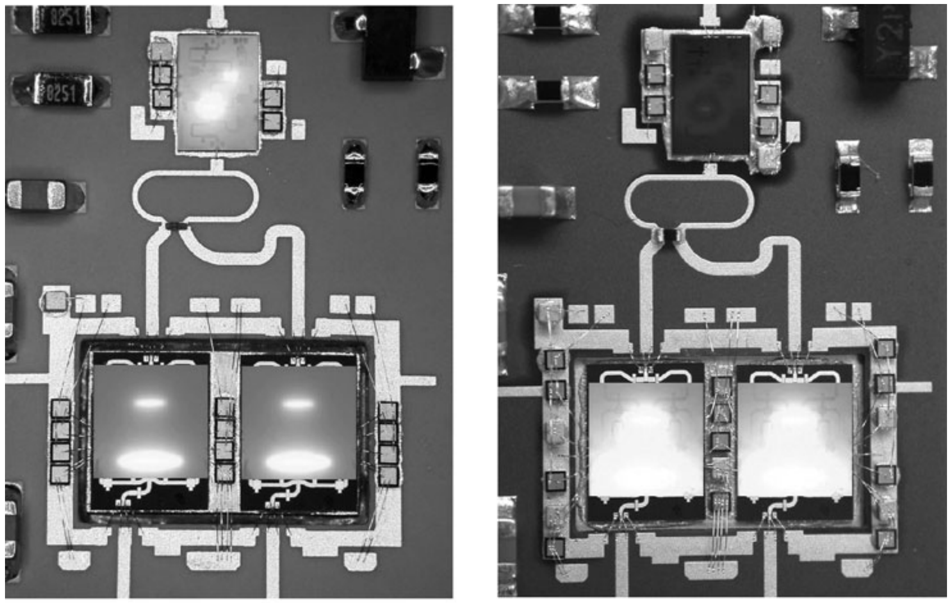

Fig. 14. Thermal photos of the GaN MMIC mounted on different substrates. Brighter colors represent higher temperature: (a) LTCC and (b) HTCC.

A first approach was to use AlN high-temperature cofired ceramic (HTCC) instead of LTCC because of its significantly higher thermal conductivity. In this case the DA and the two HPAs were mounted directly on the HTCC substrate in cavities. In Fig. 14 thermal photos of the GaN MMICs are shown. During the measurement the same dissipation power was used for both assemblies, the LTCC version (Fig. 14(a)) and the HTCC version (Fig. 14(b)). When mounting the DA on top of the HTCC substrate, the thermal situation is improved. The thermal conductivity of HTCC is much higher than the thermal conductivity of LTCC with thermal via-holes. But the situation is changing in the case of HPAs. The thermal situation is dramatically declined compared to the LTCC version where the HPAs are mounted on a metallic heatsink.

The favored solution today is using the proven LTCC technology for T/R modules used in series production and soldering the DA similar to the HPAs on a CuMo heatsink.

The T/R module front-end consists of a whole transmit path with one DA and two HPAs in parallel, a circulator, a receive path with LNA and limiter and a GaAs switch combining both paths. It can be used as a front-end for a software-defined radar or can be combined with any core chip using CMOS, SiGe, or GaAs technology.

Besides the RF relevant components, like power splitter and combiner, also the whole DC control electronics is integrated on the substrate. The control electronics provides the pulsed 30v drain voltage for the GaN high-power MMICs, the LNA bias voltages, and the T/R switch control.

For the transmit operation mode the output power, gain, and PAE measurement results in pulsed mode are shown in Fig. 15. The maximum measured output power is 32 W. In this case the small signal gain is about 31 dB and the associated front-end PAE value is 24%, also taking into account the dissipation power of the control electronics.

More than 20 W output power is measured over a bandwidth of 2.5 GHz (see Fig. 16). The small signal gain of the front-end has a positive slope versus frequency up to 11 GHz.

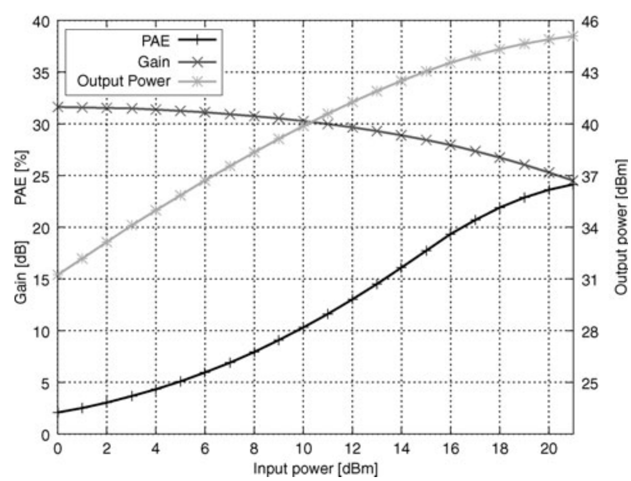

Fig. 15. Measured power performance of the GaN T/R-module front-end at 11 GHz with $V_{DS} = 30$ V and $V_{GS} = -5$ V. $P_{max} = 45$ dBm, $PAE_{max} = 24\%$.

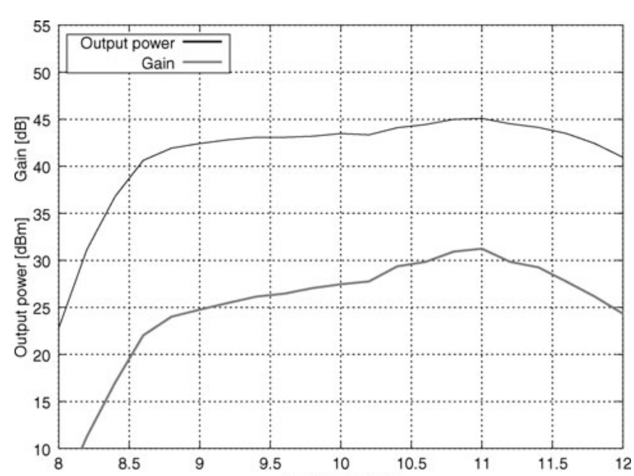

Fig. 16. Measured saturated output power and small signal gain versus frequency of the GaN T/R-module front-end. Bias point: $V_{DS} = 30$ V and $V_{GS} = -5.0$ V.

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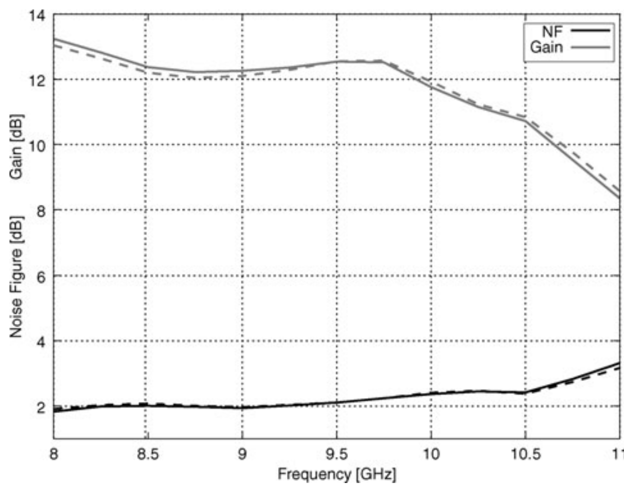

Fig. 17. Measured gain and noise figure versus frequency of the GaN T/R module front-end. Initial measurements (solid lines) and after applying 7 W input power (dashed lines). $NF_{min} = 2$ dBm.

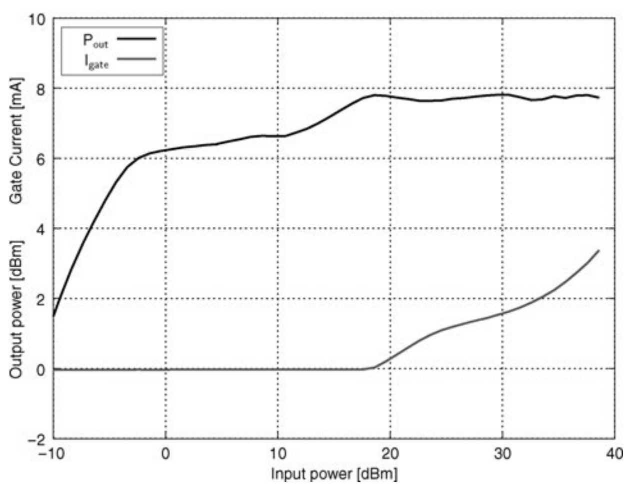

Fig. 18. Measured output power and gate current versus input power of the GaN T/R-module front-end in the receive mode.

In the receive operation mode a small signal gain in the range of 12.5 dB is measured. The associated noise figure is about 2 dB at room temperature (see Fig. 17). After the initial noise figure measurement the input power at the front-end was stepwise increased up to 7 W. After each step the noise figure measurement was repeated. In Fig. 17 the noise figure measurement result after applying 7 W input power is the same just like the initial measurement result. Also there is no variation of the receive gain visible.

In Fig. 18 the compressed output power of the front-end in receive mode is shown. Up to 7 W input power the output power stays below 8 dBm. This allows a safe operation of the following small signal MMICs like GaAs core chips.

VII. CONCLUSION

A whole GaN MMIC amplifier chip set for an X-band T/R module front-end was designed, simulated, fabricated, and measured. Output power levels up to 20 W for the transmit path HPA and a noise figure of 1.45 dB for the receive path LNA are achieved. A T/R module front-end with three types of amplifiers (DA, HPA, and LNA) integrated on multi-layer LTCC substrates is successfully demonstrated. To our knowledge, this is the first published GaN-based T/R module front-end, outperforming the state-of-the-art GaAs-based T/R module front-end in terms of transmit output power and receive noise figure. With such a front-end, T/R modules with more than 20 W transmit output power and a receive noise figure below 3 dB can be realized.

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