International Journal of Microwave and Wireless Technologies

cambridge.org/mrf

Optimization of InP DHBT stacked-transistors for millimeter-wave power amplifiers

Michele Squartecchia[1], Tom K. Johansen[1], Jean-Yves Dupuy[2], Virginio Midili[1], Virginie Nodjiadjim[2], Muriel Riet[2] and Agnieszka Konczykowska[2]

[1]Department of Electrical Engineering, Technical University of Denmark, 2800 Kongens Lyngby, Denmark and [2]III-V Lab (joint lab of Nokia Bell Labs, Thales, and CEA-Leti), 91767 Palaiseau, France

Research Paper

Cite this article: Squartecchia M, Johansen TK, Dupuy J-Y, Midili V, Nodjiadjim V, Riet M, Konczykowska A (2018). Optimization of InP DHBT stacked-transistors for millimeter-wave power amplifiers. *International Journal of Microwave and Wireless Technologies* **10**, 999–1010. https://doi.org/10.1017/S1759078718001137

Received: 3 March 2018
Revised: 9 July 2018
Accepted: 11 July 2018
First published online: 7 August 2018

Keywords:
Power amplifiers; semiconductor devices and IC-technologies; stacked-transistor

Author for correspondence:
Tom K. Johansen E-mail: tkj@elektro.dtu.dk

Abstract

In this paper, we report the analysis, design, and implementation of stacked transistors for power amplifiers realized on InP Double Heterojunction Bipolar Transistors (DHBTs) technology. A theoretical analysis based on the interstage matching between all the single transistors has been developed starting from the small-signal equivalent circuit. The analysis has been extended by including large-signal effects and layout-related limitations. An evaluation of the maximum number of transistors for positive incremental power and gain is also carried out. To validate the analysis, E-band three- and four-stacked InP DHBT matched power cells have been realized for the first time as monolithic microwave integrated circuits (MMICs). For the three-stacked transistor, a small-signal gain of 8.3 dB, a saturated output power of 15 dBm, and a peak power added efficiency (PAE) of 5.2% have been obtained at 81 GHz. At the same frequency, the four-stacked transistor achieves a small-signal gain of 11.5 dB, a saturated output power of 14.9 dBm and a peak PAE of 3.8%. A four-way combined three-stacked MMIC power amplifier has been implemented as well. It exhibits a linear gain of 8.1 dB, a saturated output power higher than 18 dBm, and a PAE higher than 3% at 84 GHz.

Introduction

Wireless communications in backhaul networks are envisioned to take place at E-band (71–76 GHz and 81–86 GHz) and higher millimeter-wave frequencies due to the increasing demand for large bandwidths. In this context, power amplifiers are probably the most critical part. The continuous size downscaling of devices allows to operate at such high frequencies [1], but this entails also a reduction of the sustainable operating voltage and output power, as predicted by the Johnson limit [2]. Power combining techniques are often needed to reach acceptable levels of transmitted power. Parallel current combining architectures represent the mainstream in this regard, but their moderate losses can impair the power amplifier performance. Moreover, their relatively large chip-area occupancy might be an issue. A viable alternative is the series voltage combining technique, known as stacked-transistor, where individual voltage swings of the single devices are summed up in phase keeping the current swing approximately unchanged in comparison with a single-device power cell. If n is the number of transistors connected in series, this results in an overall output power n times higher. Another potential benefit is that the optimum output load, defined as the ratio between the maximum voltage and current swings, also increases by the same factor, allowing a wider bandwidth and lower losses in the matching network. The stacked-transistor topology consists of a common-emitter (or common-source) stage followed by a series of $n-1$ common-base (or common-gate) stages. It differs from the cascode because finite impedances are connected to the base of the common-base stages, making the base terminals experience a voltage swing to prevent base-collector breakdown. Collector-emitter breakdown is avoided by making the overall output voltage be equally divided among all the devices. This architecture has been successfully deployed at RF and microwave frequencies since its conception a couple of decades ago [3–9], showing promising performances in terms of output power, gain, and efficiency. More recently, many research efforts have been exerted to extend the stacked-transistor concept at higher frequencies and into the millimeter-wave range [10–15]. An important condition to be satisfied for optimal performance is the interstage impedance matching between all the devices so as to limit internal reflections and power degradation. This aspect has been particularly emphasized in previous works and detailed analysis for calculating the common-base input impedance have been carried out. For operating frequencies much lower than the cut-off frequency f_T, the transistors' reactive components have been neglected without significant loss of accuracy [5]. At high millimeter-wave frequencies, however, this simplification does not hold and layout-related parasitics must be characterized through electromagnetic (EM) simulations and taken into account [13, 15]. Several strategies have been proposed to accomplish

CAMBRIDGE UNIVERSITY PRESS

the interstage matching condition, comprising series or parallel shunt inductive tuning and capacitive shunt-feedback tuning [10].

The stacked-transistor technique has been used mostly to overcome the limited breakdown voltage of silicon-based devices and GaAs HEMTs. Only a few works have been focused on applying this approach to InP Double Heterojunction Bipolar Transistors (DHBTs) [16–18], and they were just limited to two-stacked topologies. InP DHBTs are proved to be well-suited for power amplifiers at high millimeter-wave frequencies thanks to high values of f_T and f_{max}, as well as moderately high breakdown voltage [19–21]. To the best of the authors' knowledge, this work represents an unprecedented attempt to extend the stacking technique to three and four InP DHBT transistors. The investigation follows a structured design flow starting from a small-signal analysis; it then includes large-signal models and finally accounts for the parasitic effects impairing the performance of the power cells. The latter step is particularly crucial and is carried out by means of extensive EM simulations [22, 23]. Three- and four-stacked monolithic microwave integrated circuit (MMIC) matched power cells have been realized and measured for operation in the upper range of the E-band.

This paper is structured as follows: In the section 'Circuit analysis and design', the analysis and procedure for the design of DHBT stacked-transistors is described in detail, including layout optimization based on EM-circuit co-simulations. In the section 'Implementations and experimental results', the MMIC implementations of the matched power cells and their measured response are outlined. A four-way combined MMIC power amplifier based on three-stacked transistors is also reported together with measured results. Finally, in the section 'Conclusion', the results are summarized and discussed.

Circuit analysis and design

Figure 1 shows a conceptual schematic of a four-stacked transistor power cell ($n = 4$). It is composed of a common-emitter stage Q_1 followed by a series of three common-base stages Q_2–Q_4. For optimum output power and avoiding collector-emitter breakdown, all the devices must operate in phase under maximum voltage and current swing conditions. Base-collector breakdown is avoided by making all the base terminals swing with proper amplitude and phase, which is accomplished with the base capacitances C_2–C_4 providing finite impedances, in contrast with classical cascode implementation, where the base terminals are dynamically grounded. The base capacitances C_k, together with the susceptances $B_{k-1,k}$ (k = 2,3,4), play also an important role for interstage impedance matching between the transistors. The parallel R_1–C_1 is essential to stabilize the circuit at low frequencies. In order to easily separate real and imaginary parts in the interstage matching design, admittances are considered instead of impedances as the elements to be tuned out are usually shunt parasitic capacitances. The bias network is omitted in the figure, but it should be noted that all transistors must operate with the same quiescent point, and since they are dc-coupled, a relatively high bias voltage could be required. In this section, we outline the theoretical relationships and the design procedure for properly dimensioning the circuit parameters for optimum operation. First, a calculation based on an approximated small-signal equivalent circuit is given. A more practical approach based on the large signal-model is described afterward and the real design with layout considerations will be finally presented.

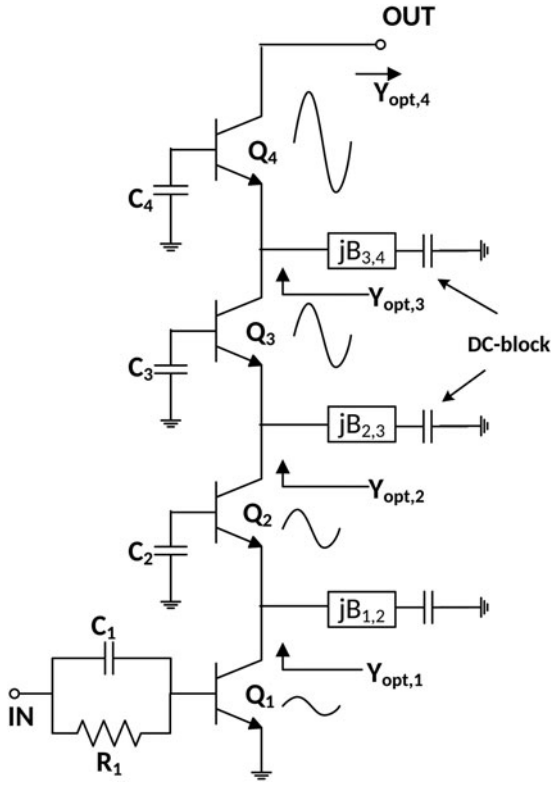

Fig. 1. Conceptual circuit schematic of a four-stacked transistor power cell.

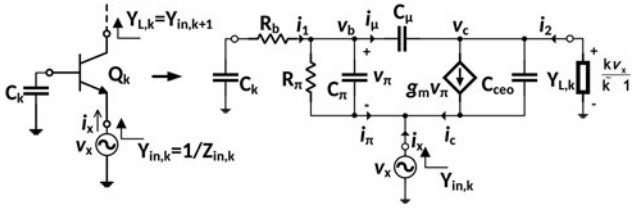

Fig. 2. InP DHBT small-signal equivalent circuit of the *k*th common-base stage for calculation of the input admittance $Y_{in,k}$. Extracted parameters for a single-finger device with emitter area of $10 \times 0.7\ \mu m^2$ are: $R_b = 21.1\ \Omega$, $R_\pi = 110\ \Omega$, $C_\pi = 129.1$ fF, $C_\mu = 10.7$ fF, $C_{ceo} = 4.9$ fF, and $g_m = 403$ mS.

Small-signal analysis

The small-signal analysis of the stacked architecture is essential to understand the design principles. Like previous works on this subject, it can be conducted by considering the *k*th common-base stage for assessing its emitter input admittance $Y_{in,k}$, which must be equal to the optimum load $Y_{opt,k-1}$ of the preceding partial stack [9, 13, 17]. In doing so, we refer to Fig. 2, where a test voltage source v_x is applied to the emitter terminal and the resulting current i_x is evaluated. The interstage susceptance $B_{k-1,k}$ has been omitted in the figure as it can be considered separately as a mean to resonate the imaginary part of $Y_{opt,k-1}$, so at the beginning, only the real part $\Re[Y_{in,k}]$ is of concern. The illustrated small-signal equivalent circuit corresponds to a single-finger InP DHBT biased at $V_{ce} = 2$ V and $I_c = 15$ mA, whose parameters have been extracted from measured *S*-parameters following the procedure described in [24]. Some simplifying assumptions are

https://doi.org/10.1017/S1759078718001137 Published online by Cambridge University Press

made: we neglected in this representation the distributed nature of the base resistance and of the base-collector capacitance, so we assumed $R_b = R_{bx} + R_{bi}$ and $C_\mu = C_{bcx} + C_{bci}$, where R_{bx} and R_{bi} are the extrinsic and intrinsic base resistances, respectively, and C_{bcx} and C_{bci} are the extrinsic and intrinsic base-collector parasitic capacitances, respectively. We assumed also that the emitter resistance R_E and the collector resistance R_C are small enough to be neglected. It should be noted that in this analysis, differently from some previous works, the feedback effects introduced by C_μ and C_{ceo} are carefully taken into account. At millimeter-wave frequencies, in fact, these represent an important contribution to the calculation of $Y_{in,k}$, which strongly depends on the load admittance $Y_{L,k}$. The relationship between the collector voltage v_c and the emitter voltage v_x, corresponding to the required voltage gain for in-phase voltage addition of the kth common-base stage is explicitly shown in the figure. In mathematical form, the following three conditions must be met simultaneously:

$$\begin{cases} \Re[Y_{in,k}] = \Re[Y_{opt,k-1}] & \text{(1a)} \\ \Re\left[\dfrac{v_c}{v_x}\right] = \dfrac{k}{k-1}, \quad (k = 2, \ldots, n), & \text{(1b)} \\ \Im\left[\dfrac{v_c}{v_x}\right] = 0, & \text{(1c)} \end{cases}$$

where the gain v_c/v_x has been found to have the following expression (see Appendix):

$$\frac{v_c}{v_x} = \frac{\left[(sC_\mu + sC_{ceo})Z_b + (g_m + sC_{ceo})(1 + sC_\mu Z_b)Z_\pi\right]}{\begin{array}{l}(Y_{L,k} + sC_{ceo})(Z_b + Z_\pi + sC_\mu Z_b Z_\pi) \\ +sC_\mu(Z_b + Z_\pi + g_m Z_b Z_\pi)\end{array}}, \quad (2)$$

with $Z_b = R_b + 1/(sC_k)$, $Z_\pi = R_\pi/(1 + sC_\pi R_\pi)$, and $s = j\omega$. Imposing the conditions (1b) and (1c) to (2), the admittance seen into the emitter can be calculated as:

$$Y_{in,k} = \frac{sC_\mu Z_\pi(k/(k-1)) + 1}{Z_b + Z_\pi + sC_\mu Z_b Z_\pi} + \frac{k}{k-1} Y_{L,k}. \quad (3)$$

At a given frequency and for a given transistor model, it can be seen that (1) is a system of three equations in the three unknowns C_k, $G_{L,k} = \Re[Y_{L,k}]$, and $B_{L,k} = \Im[Y_{L,k}]$, which can be solved numerically and verified with a circuit simulator. The calculated values of the unknown parameters are reported in Figs 3 and 4 as functions of the stack number k at different frequencies for a single-finger InP DHBT with an emitter area of $10 \times 0.7\ \mu m^2$. It can be observed that both the base capacitance C_k and the load admittance $Y_{L,k}$ decrease as the stack number k and frequency increase.

The value of the interstage shunt susceptance $B_{k-1,k}$ is calculated for conjugate matching:

$$B_{k-1,k} = -\Im[Y_{opt,k-1}], \quad (4)$$

which is often implemented by means of an inductor $L_{k-1,k}$ tuning out the output parasitic capacitance of the $(k-1)$th transistor. The latter condition ensures that the same current flows through all the devices.

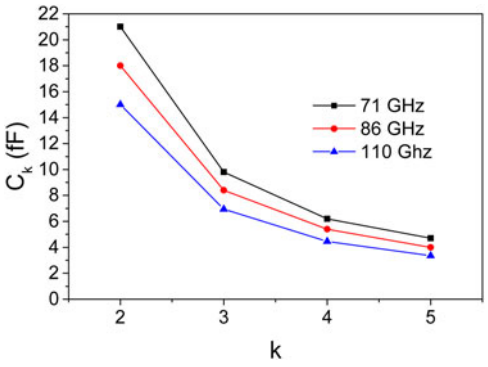

Fig. 3. Theoretical values of the base capacitance C_k as a function of the stack number k for the kth common-base stage operating at different frequencies.

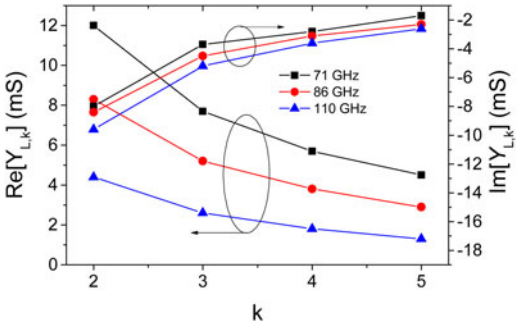

Fig. 4. Theoretical values of the load admittance $Y_{L,k}$ as a function of the stack number k for the kth common-base stage operating at different frequencies.

Large-signal analysis

The above small-signal analysis is essential to get a useful understanding of the stacked-transistor concept and it is used to make a first estimation of the circuit parameters. However, it represents an idealization as real power amplifiers work in the large signal regime, near or well into saturation. Moreover, additional parasitics might be present, especially in multifinger devices, which are usually preferred to get higher power performances. A follow-up simulation using harmonic balance and large-signal transistor models is necessary in order to capture nonlinearities and additional parasitic effects. Besides interstage matching and in-phase voltage addition, power performances must be evaluated to determine the effectiveness of an additional stage along the stacked architecture. A structured design-flow for dimensioning all the parameters can be synthesized in a few essential points as illustrated in the flow-chart of Fig. 5. The initial step is the evaluation of the common-emitter power gain performances and optimum load $Y_{opt,1}$ by means of a load-pull simulation performed on the large-signal model of the selected transistor. At millimeter-waves, in order to achieve acceptable gain and good linearity, Class A bias condition is selected. In this work, four-finger InP DHBT transistors featuring a breakdown voltage $BV_{CEO} \approx 5$ V and a maximum oscillation frequency $f_{max} > 350$ GHz have been considered. A modified UCSD HBT model extracted from previous measurements is used in simulations with a bias point $V_{ce} = 2.4$ V and $I_c = 60$ mA [25]. The 86-GHz optimum load $Z_{opt,1} = 1/Y_{opt,1}$ and the resulting load

https://doi.org/10.1017/S1759078718001137 Published online by Cambridge University Press

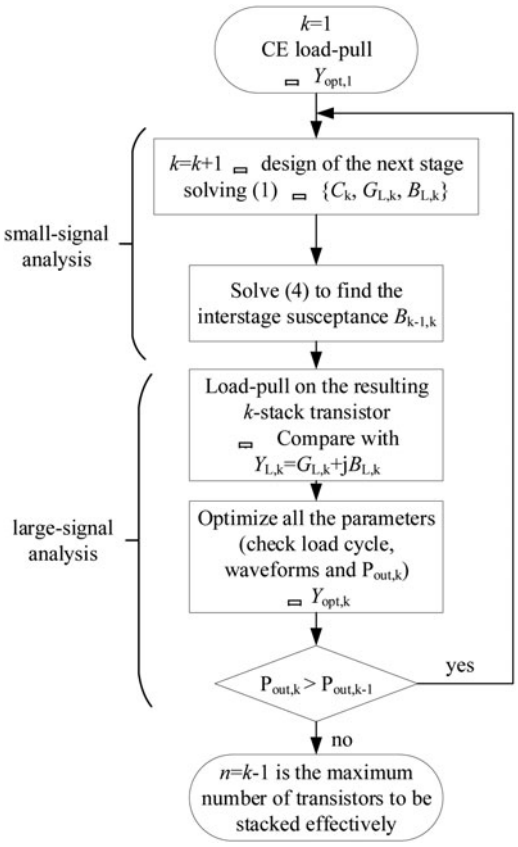

Fig. 5. Structured design flow for the design of an *n*-stacked transistor power cell.

cycle for such a transistor in common-emitter configuration is shown in Fig. 6(a). A first estimation of the circuit parameters of the following common-base stage is then carried out by solving (1) and (4) in the small-signal analysis with $k = 2$. The found value $Y_{L,2}$ can then be checked in large-signal regime by means of a load-pull simulation performed on the resulting two-stacked structure. All the parameters are then optimized so as to obtain maximum voltage and current swings for both devices, as shown in Fig. 6(b). In this way $Y_{opt,2}$ is obtained and eventually used as the starting point in the design of the following third stage. This procedure can be iterated for the subsequent stages as long as positive incremental power gain is achieved. There will be a value of k for which $P_{out,k} \leq P_{out,k-1}$. In this case $n = k - 1$ is the maximum number of transistors that can be stacked effectively. In Fig. 6, the optimized load cycles of the common-emitter, two-stacked, three-stacked, and four-stacked transistors operating at the 1-dB compression point at 86 GHz are shown. The power performance improvement of each stage is reported together with the corresponding increase of the load impedance level (or reduction of the load admittance) as predicted in the small-signal analysis. The values of the circuit elements of the optimized four-stacked transistor are reported in Table 1. In Fig. 7, the corresponding in-phase voltage waveforms taken at each collector node are reported. The improvements in terms of maximum available gain (MAG) are shown in Fig. 8, where a slight bandwidth reduction can be observed along the stacked architecture as a consequence of the inherently narrow-band reactive tuning of the design approach.

Layout

The InP technology used in this work comprises three TiPdAu metal layers (*met1–met3*) separated by polyimide for the realization of interconnections and transmission lines. A NiCr layer featuring 40 Ω/square is used for the realization of resistors and a thin Si_3N_4 layer serves for the realization of high-*Q* metal-insulator-metal capacitors with 0.49 fF/μm^2. In Fig. 9, the schematic and layout views of the common-emitter, two-, three-, and four-stacked transistors are shown together with the respective optimized load cycles taken across each device after EM-circuit co-simulations and optimization carried out on ADS Momentum. The EM-circuit co-simulation approach ensures that all parasitics related to the particular layout and technology are accurately taken into account [22, 23]. Resistive feedback networks are used as self-bias and for stabilization [26]. The EM-simulation approach ensures that all the parasitic effects are inherently taken into account during the optimization process.

As can be seen in Fig. 9(a), the optimum load of the common-emitter power cell has a small reactive component so a shunt interstage inductor was not necessary in the design of the two-stacked transistor. For the three- and four-stacked transistors, the shunt inductors $L_{2,3}$ and $L_{3,4}$ for interstage matching are realized by means of dynamically shorted coplanar waveguide (CPW) lines. Given the size constraints, the dc-blocking capacitors are of limited value and the equivalent *LC* series cause a resonance effect around 50 GHz. Another extremely important circuit component in the circuit layout is the finite-length emitter-collector interconnection between adjacent devices. This circuit element, in fact, represents the major limitation for efficient operation as it introduces significant phase misalignment between the collector voltages, as shown in the resulting waveforms of Fig. 10. However, technology-related design rules impose a lower limit on its length and some performance degradation seems unavoidable. In Fig. 9, the key performance metrics for the four designed power cells are reported. It can be seen that the gain improves considerably with the number of stacked transistors, while power performances are characterized by an earlier compression. For instance, the gain improvement of the three-stacked transistor over the two-stacked one is approximately 3 dB, while the output power at the 1-dB compression point is only one dB higher. The three- and four-stacked transistors exhibit comparable output power levels, but compression occurs at lower input power for the latter and, because of the higher bias voltage, it results also in a power added efficiency (PAE) degradation. Thus, it seems that the three-stacked transistor represents the best compromise in terms of gain and power performances.

Another layout-related effect can be noticed on the values of the optimum load impedances, whose values, differently from the schematic implementation, do not increase substantially with the number of stacked transistors. Some attention has to be drawn also to the effects of layout parasitics on the MAG. Fig. 11 shows the MAG comparison between pure schematic and layout designs. While the degradation for the common-emitter and the two-stacked transistors is due to extra parasitics of the layout implementations, the resonating effect of the shunt interstage CPW lines in the layout of the three- and four-stacked transistors makes their MAG decay considerably about 50 GHz. On the other hand, the series interconnects between the devices could be responsible for a small increase of the MAG at higher frequencies, an effect that can be somehow ascribed to an inductive peaking effect.

https://doi.org/10.1017/S1759078718001137 Published online by Cambridge University Press

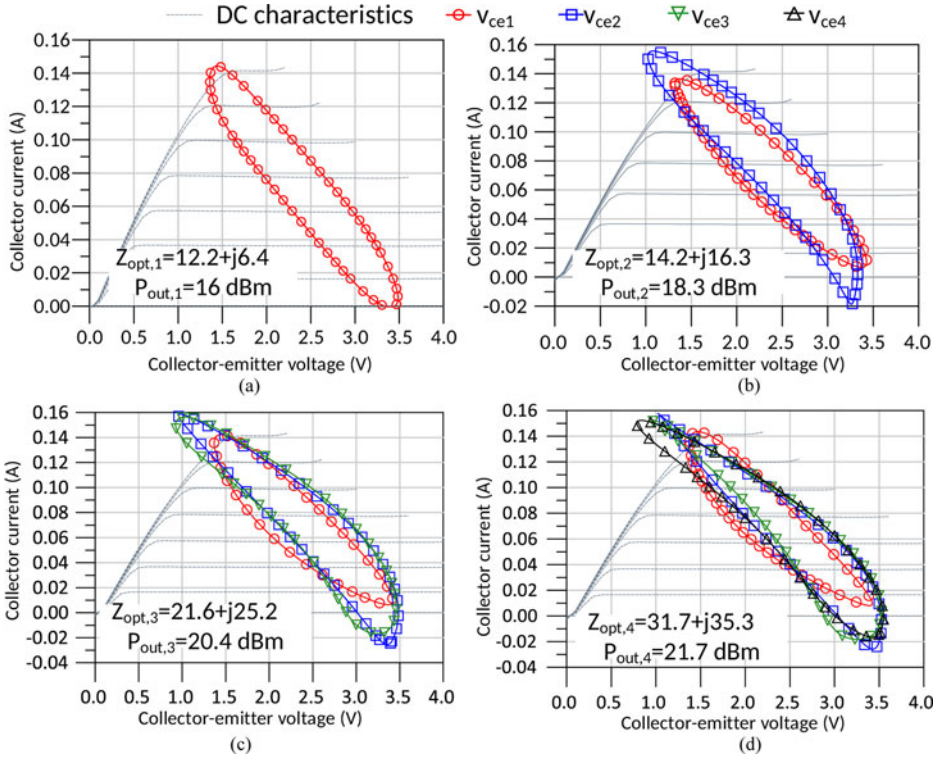

Fig. 6. Optimized load cycles for common-emitter (a), two-stacked (b), three-stacked, (c) and four-stacked (d) $4 \times 10 \times 0.7\,\mu m^2$ InP DHBTs transistors at 86 GHz. The input power is kept at $P_{in} = 10$ dBm in all cases.

Table 1. Circuit parameters for an optimized four-stacked transistor.

R_1 (Ω)	C_1 (fF)	C_2 (fF)	C_3 (fF)
250	300	160	65
C_4 (fF)	$L_{1,2}$ (pH)	$L_{2,3}$ (pH)	$L_{3,4}$ (pH)
40	150	88	75

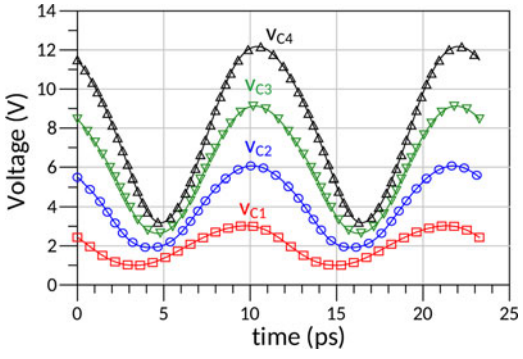

Fig. 7. Collector voltage waveforms of the four-stacked transistor at 86 GHz after load cycle optimization.

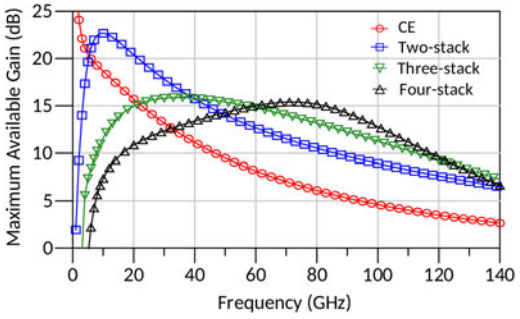

Fig. 8. Maximum available gain of the optimized common-emitter, two-, three-, and four-stacked transistors.

Implementations and experimental results

The design principles described above have been verified experimentally for the three- and four-stacked transistors. The relative matched power cells have been implemented and tested in small- and large-signal operations. The matching networks have been designed using the in-house developed design-kit comprising all passive structures, including 50-Ω CPW transmission lines. Once again, all these structures have been previously characterized through extensive EM simulations. A four-way combined power amplifier employing three-stacked transistors has been realized as well, where a corporate power combiner is used. S-parameters measurements have been carried out on the wafer using RF GSG probe tips and the VNA MS4647 by Anritsu. For large-signal measurements, a custom-made test setup has been implemented, whose conceptual representation is shown in Fig. 12(a): a low-frequency sinusoidal signal is generated by the frequency synthesizer 68169B by Anritsu; the required E-band signal is then obtained by means of the frequency multiplier (×6) RPG AFM6 capable of a maximum output power of 7 dBm. A 0–50 dB variable attenuator and the 70–90 GHz medium power amplifier RPG 7090 are used together to vary the input power fed into the device under test. The output power level is measured with the power sensor W8486A and

https://doi.org/10.1017/S1759078718001137 Published online by Cambridge University Press

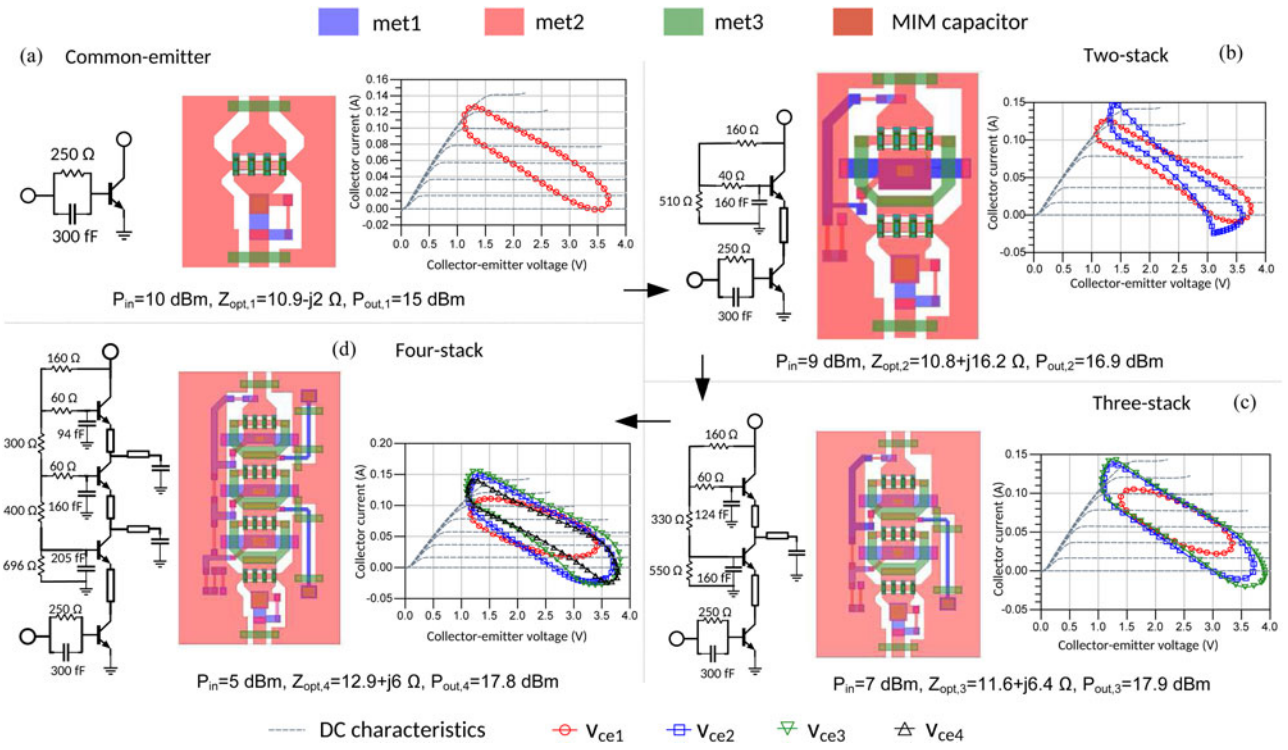

Fig. 9. Power cells layout of the common-emitter (a), two-stacked (b), three-stacked, (c) and four-stacked transistors (d) and corresponding simulated load cycles after EM-circuit co-simulation and optimization at 86 GHz.

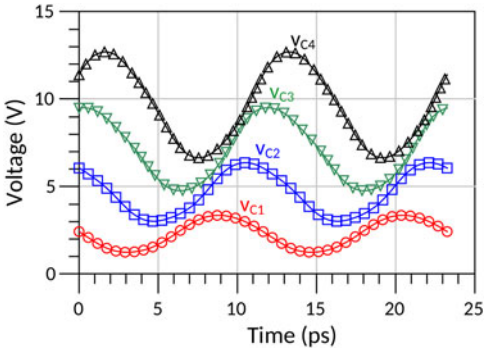

Fig. 10. Collector voltage waveforms at 86 GHz of the four-stacked transistor taking into account layout parasitics.

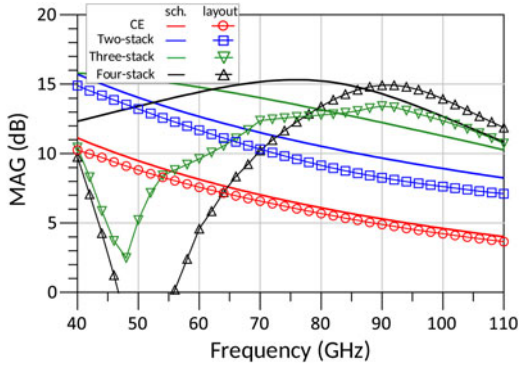

Fig. 11. MAG comparison between pure schematic design and taking into account layout parasitics for the four power cells.

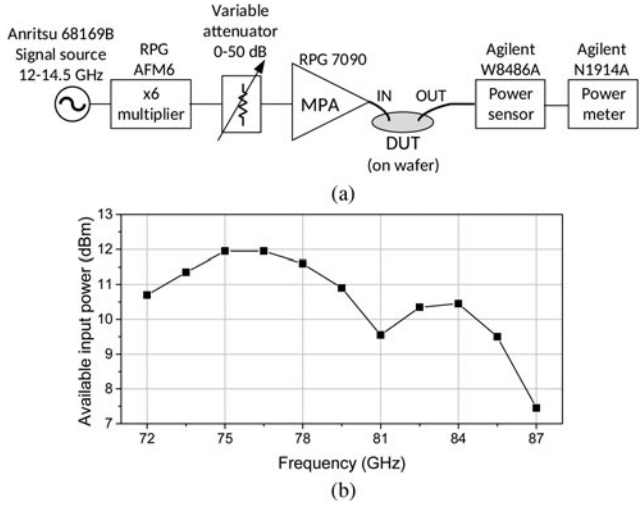

Fig. 12. Conceptual representation of the large-signal measurement setup (a) and calibrated maximum available input power at different frequencies (b).

the power meter N1914A by Agilent. A shortcoming with this setup is that the maximum available power at the input probe tip is limited and its frequency dependence over the E-band range is reported in Fig. 12(b). This did not represent an issue in measuring simple power cells, but revealed as a significant restriction for multiple power-combined circuits, which could not be operated in saturation.

https://doi.org/10.1017/S1759078718001137 Published online by Cambridge University Press

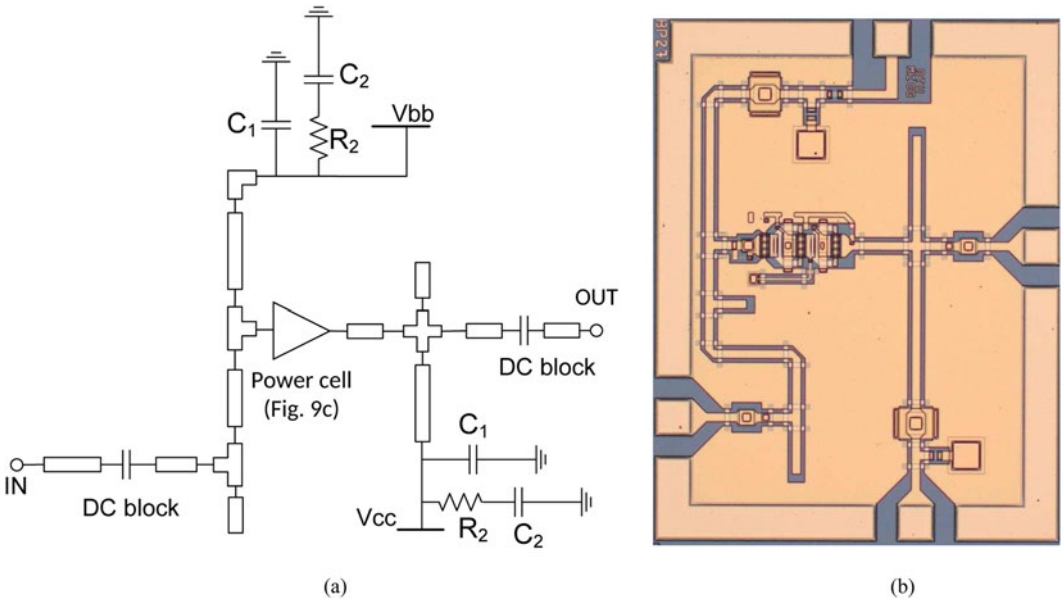

Fig. 13. Schematic (a) and chip microphotograph, (b) of the matched three-stacked transistor power cell. The chip size is 1.2 × 1.5 mm^2.

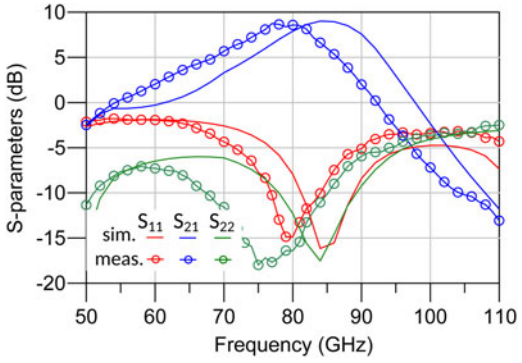

Fig. 14. Simulated and measured *S*-parameters of the matched three-stacked transistor power cell.

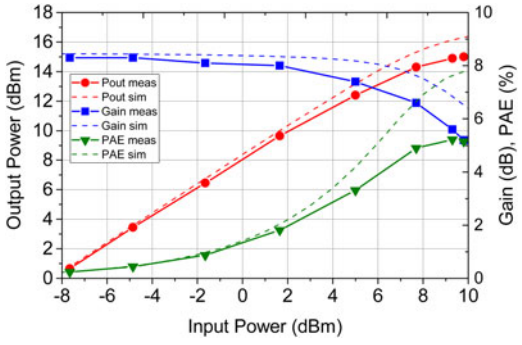

Fig. 15. Simulated and measured power sweep of the matched three-stacked transistor power cell at 81 GHz.

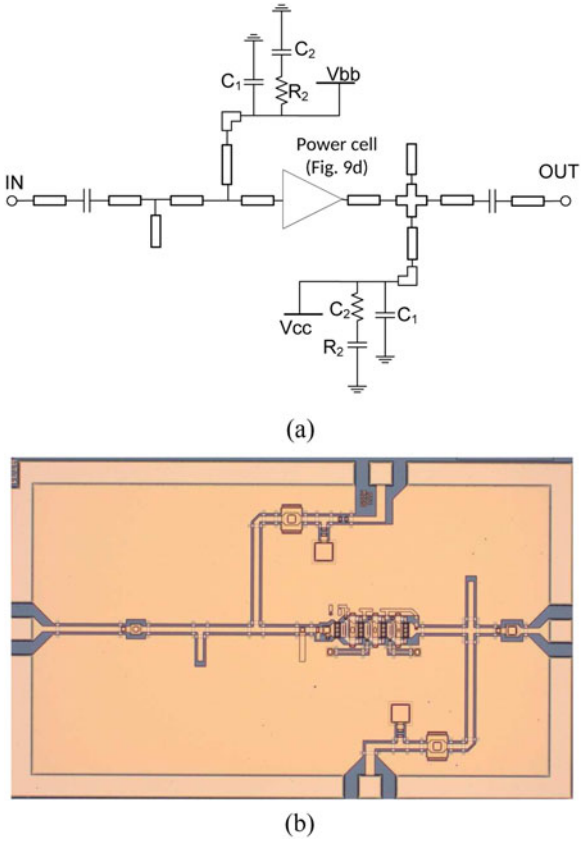

Fig. 16. Schematic (a) and chip microphotograph (b) of the matched four-stacked transistor power cell. The chip size is 2.4 × 1.5 mm^2.

Three-stacked transistor power cell

Figures 13(a) and 13(b) show the schematic and chip microphotograph, respectively, of the matched three-stacked transistor power cell. The bias voltages V_{cc} and V_{bb} are 6 and 1.7 V, respectively, resulting in a total current of 65 mA, including the current flowing in the resistive feedback network. The bypass capacitors C_1 provide dynamic shorts at the operating frequencies, while the series R_2–C_2 helps to attenuate eventual low-frequency

https://doi.org/10.1017/S1759078718001137 Published online by Cambridge University Press

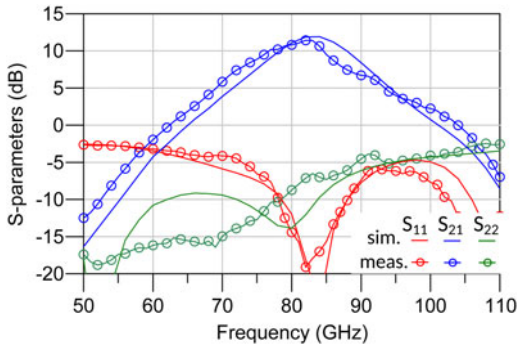

Fig. 17. Simulated and measured *S*-parameters of the matched four-stacked transistor power cell.

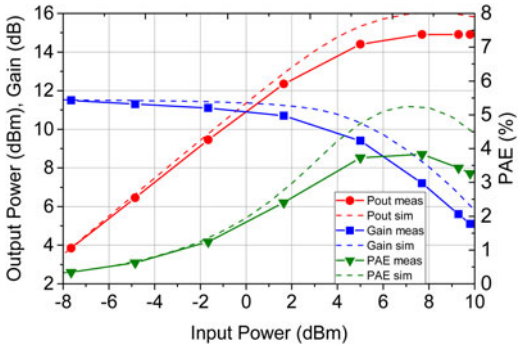

Fig. 18. Simulated and measured power sweep of the matched four-stacked transistor power cell at 81 GHz.

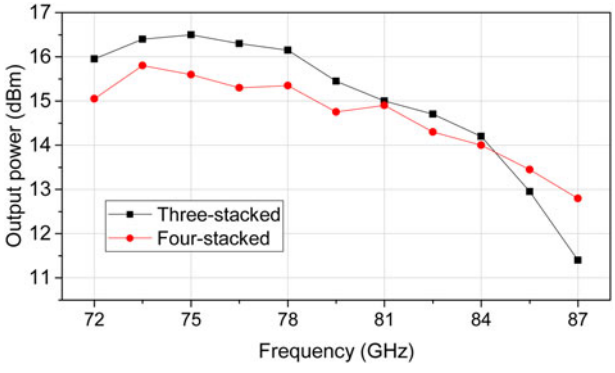

Fig. 19. Output power versus the frequency of the three-stacked and four-stacked MMIC power cells.

oscillations. The MMIC size is $1.2 \times 1.5\ \text{mm}^2$. Measured and simulated *S*-parameters are reported in Fig. 14, where a good agreement can be observed, except for a frequency downshift of approximately 5 GHz most likely due to the input matching network, where bended CPW structures are used in order to comply with the chip-size requirements. The peak $|S_{21}|$ is 8.6 dB and occurs at 80 GHz. A 15-GHz 3-dB bandwidth is obtained in the range 70–85 GHz and the input return loss is better than 10 dB from 77 to 84 GHz. Simulated and measured large-signal performances at 81 GHz are reported in Fig. 15. It can be seen that the output power at the 1-dB compression point is approximately $P_{out,1dB} \approx 12.5$ dBm, with the corresponding input power $P_{in,1dB} \approx 5$ dBm. The saturated output power is $P_{sat} \approx 15$ dBm and the peak power-added efficiency resulted in $PAE \approx 5.2\%$. An excellent agreement between measurements and simulations is obtained at low power levels, somehow confirming *S*-parameter measurements. However, as the input power increases, the measured response seems to exhibit a slightly earlier compression. This can be due to a small difference in the output matching condition caused by the frequency downshift and to the accuracy of the large-signal modeling of the devices.

Four-stacked transistor power cell

For the realization of the four-stacked transistor matched power cell (Fig 16), the requirements on the chip-size were less stringent and a straight matching network could be realized. The MMIC size, in this case, is $2.4 \times 1.5\ \text{mm}^2$. The only difference in the bias setting with respect to the three-stacked power cell is a higher V_{cc}, which in this case is 8 V. The measured and simulated *S*-parameters are reported in Fig. 17, where a peak $|S_{21}|$ of 11.4 dB at 83 GHz is observed. A 12-GHz 3-dB bandwidth is obtained from 74 to 86 GHz and the input return loss is better than 10 dB from 78 to 88 GHz. The power sweep response at 81 GHz is shown in Fig. 18, where the output power at the 1-dB compression point is observed around $P_{out,1dB} \approx 12.5$ dBm with an input power $P_{in,1dB} \approx 2$ dBm, approximately 3 dB lower than the three-stacked power cell, as already predicted during the design process. The saturated output power is $P_{sat} \approx 14.9$ dBm, which is comparable with that of the three-stacked power cell, but because of the higher bias voltage, the peak power-added efficiency is degraded to $PAE \approx 3.8\%$. The different power performance characteristics of the two matched power cells can be better evaluated by comparing their broadband frequency response under large signal excitation. In Fig. 19, the measured output power of the two circuits are compared as functions of frequency, with the input power being the maximum available one as previously shown in Fig. 12(b), for which both circuits are in saturated operation. Better performances of the three-stacked power cell are evident, at least up to 84 GHz. At 85.5 GHz, the output power of the four-stacked power cell is slightly higher, but it is the result of the more pronounced frequency downshift of the three-stacked one. The three-stacked transistor has been selected for the design of a four-way combined power stage as described in the following.

Four-way combined three-stacked power amplifier stage

A schematic representation of the designed four-way combined power stage is illustrated in Fig. 20(a). Corporate topologies have been used at the input and output for combining and impedance matching. To prevent odd-mode instabilities, the R_{odd} resistors with a value of 10 Ω are placed midway between adjacent power cells. The collector bias lines have been placed at both sides of the chip to ensure symmetry. The bias voltage V_{cc} has been slightly increased to 6.5 V due to the small voltage drop along the longer bias lines, and a total collector current of 260 mA resulted. The chip microphotograph of the MMIC, whose size is $2.4 \times 1.5\ \text{mm}^2$, is shown in Fig. 20(b) and the measured and simulated S-parameters are reported in Fig. 21. The

https://doi.org/10.1017/S1759078718001137 Published online by Cambridge University Press

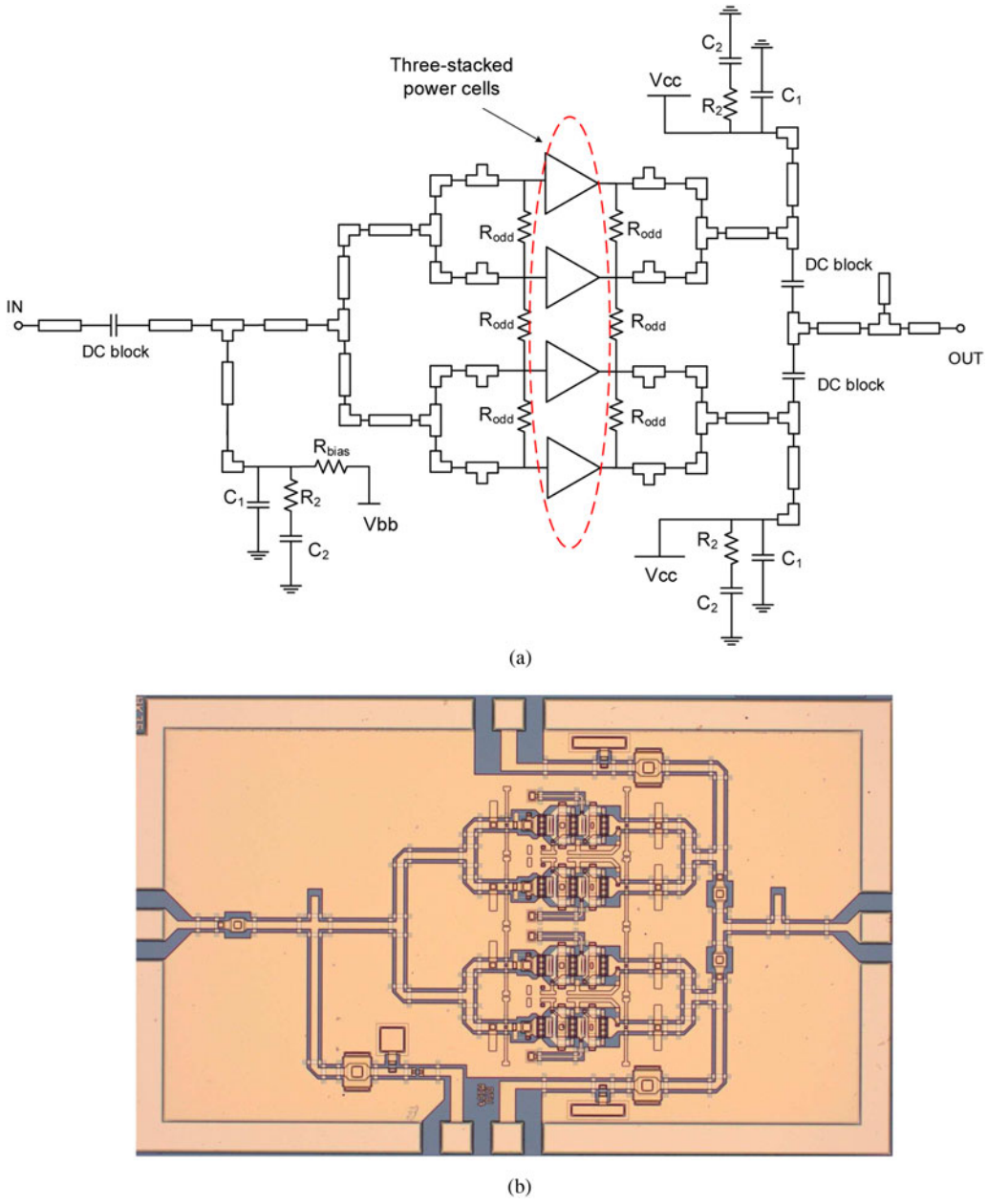

Fig. 20. Schematic (a) and chip microphotograph (b) of the four-way combined three-stacked power stage amplifier. The chip size is 2.4 × 1.5 mm2.

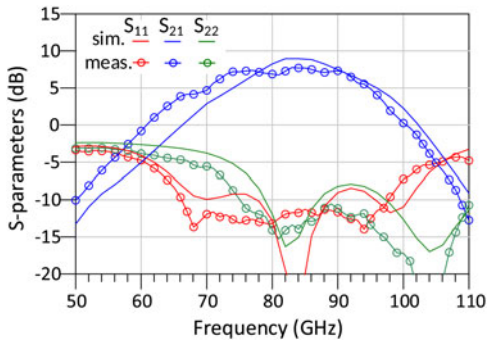

Fig. 21. Simulated and measured S-parameters of the four-way combined three-stacked power stage amplifier.

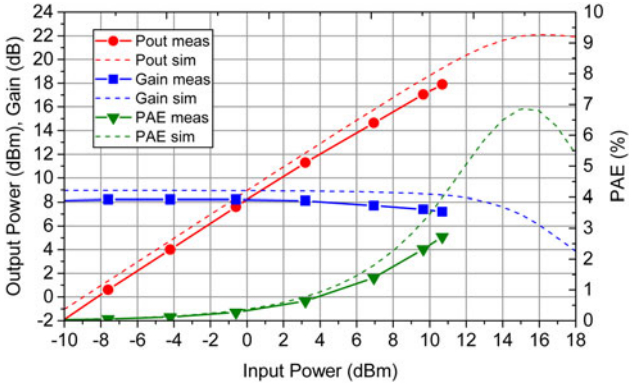

Fig. 22. Simulated and measured power sweep of the four-way combined three-stacked power stage amplifier at 84 GHz.

https://doi.org/10.1017/S1759078718001137 Published online by Cambridge University Press

3-dB bandwidth of this power amplifier is from 70 to 95 GHz, 10 GHz larger with respect to the single cell implementation. The peak $|S_{21}|$ is 7.8 dB at 83 GHz, 1 dB lower than the simulated one. The insertion loss is better than 10 dB from 67 to 97 GHz. Large-signal measurements have been carried out up to 11 dBm of input power at 84 GHz and are shown in Fig. 22. The highest linear gain is 8.1 dB and is obtained with the input power ranging between −8 and 0 dBm. The limited capabilities of the available measurement setup did not allow to evaluate the performance of the power amplifier in gain compression. At 11 dBm of input power, the output power is 18 dBm and shows little indication of gain compression. Thus the saturated output power is expected to be higher. Simulation results show an output power at the 1-dB compression point of $P_{out,1dB} \approx 21$ dBm and a saturated output power of $P_{sat} \approx 22$ dBm.

Conclusion

In this work, the well-known stacked-transistor topology for power amplifiers design has been extended to InP DHBT technology in an attempt to increase its power performance capabilities at millimeter-wave frequencies, and in particular the E-band. Structured and detailed analysis have been conducted in small- and large-signal regimes, providing guidelines for the design procedure. Limiting factors related to the particular technology have been especially identified in unavoidable layout parasitic effects. In particular, the finite length of the interconnects introduces an undesirable phase misalignment between the collector voltages, resulting in early compression. Three- and four-stacked transistors power cells have been implemented and measured in small- and large-signal operation. At 81 GHz, the saturated output power of the two circuits is comparable, being 15 and 14.9 dBm, respectively. The peak *PAE*, however, is higher for the three-stacked transistor, 5.2% against 3.8%, because of the lower bias voltage. On the other hand, small-signal gain performances are better for the four-stacked power cell, exhibiting a peak $|S_{21}|$ of 11.4 dB at 83 GHz against 8.6 dB of the three-stacked one. The three-stacked transistor has been selected as the basic power cell for the implementation of a four-way combined power stage. The measured small-signal gain of this amplifier is 7.8 dB at 83 GHz and the saturated output power is higher than 18 dBm.

Acknowledgments. This work is supported by the European Commission (FP7-People-2013-ITN project IN-POWER, grant #607647).

APPENDIX A. Gain and input admittance of the *k*th common-base stage

Applying KCL to the equivalent circuit of Fig. 2 gives:

$$\begin{cases} i_x + i + ic = 0, & \text{(A.1a)} \\ i_c = i_\mu + i_2, & \text{(A.1b)} \\ i_1 = i_\mu + i_\pi, & \text{(A.1c)} \\ i_x = i_1 + i_2 = 0. & \text{(A.1d)} \end{cases}$$

The single currents can be expressed as functions of the node voltages:

$$i_c = g_m(v_b - v_x) + sC_{ceo}(v_c - v_x), \tag{A.2}$$

$$i_\pi = (v_b - v_x)/Z_\pi, \tag{A.3}$$

$$i_\mu = sC_\mu(v_b - v_c), \tag{A.4}$$

$$i_1 = -v_b/Z_b, \tag{A.5}$$

$$i_2 = -v_c Y_{L,k}, \tag{A.6}$$

where $Z_b = R_b + 1/(sC_k)$, $Z_\pi = R_\pi/(1 + sC_\pi R_\pi)$, and $s = j\omega$. Here we try to express the collector voltage v_c as a function of the circuit parameters and the voltage source v_x. Using (A.2), (A.4), and (A.6) into (A.1b), the collector voltage can be written as

$$v_c = \frac{sC_\mu(v_b - v_c) - g_m(v_b - v_x) - sC_{ceo}(v_c - v_x)}{Y_{L,k}}. \tag{A.7}$$

In order to eliminate v_b from this expression, we can use the following equivalent relationships:

$$(v_b - v_x) = -\left[\frac{v_b}{Z_b} + sC_\mu(v_b - v_c)\right]Z_\pi, \tag{A.8}$$

$$(v_b - v_c) = \frac{v_x Z_b - v_c(Z_b + Z_\pi)}{Z_b + Z_\pi + sC_\mu Z_b Z_\pi}, \tag{A.9}$$

$$v_b = \frac{v_x Z_b + v_c sC_\mu Z_b Z_\pi}{Z_b + Z_\pi + sC_\mu Z_b Z_\pi,} \tag{A.10}$$

so that, after some algebraic manipulation, (A.7) can be rewritten as

$$v_c = \frac{\left[(sC_\mu + sC_{ceo})Z_b + (g_m + sC_{ceo})(1 + sC_\mu Z_b)Z_\pi\right]}{\begin{array}{l}(Y_{L,k} + sC_{ceo})(Z_b + Z_\pi + sC_\mu Z_b Z_\pi) \\ +sC_\mu(Z_b + Z_\pi + g_m Z_b Z_\pi)\end{array}} v_x. \tag{A.11}$$

In order to find the expression for the input emitter admittance $Y_{in,k}$, we can consider the equation (A.1d). Using (A.5), (A.6), and (A.10), it can be rewritten as

$$i_x = \frac{sC_\mu Z_\pi v_c + v_x}{Z_b + Z_\pi + sC_\mu Z_b Z_\pi} + v_c Y_{L,k}. \tag{A.12}$$

To find an expression dependent only on v_x, we could use (A.11), but for the present case we must have $v_c = kv_x/(k-1)$, so we can write (A.12) as:

$$i_x = \left[\frac{sC_\mu Z_\pi(k/(k-1)) + 1}{Z_b + Z_\pi + sC_\mu Z_b Z_\pi} + \frac{k}{k-1} Y_{L,k}\right]v_x. \tag{A.13}$$

which finally yields the expression (3) to calculate the input admittance $Y_{in,k}$.

References

1 **Scavennec A, Sokolich M and Baeyens Y** (2009) Semiconductor technologies for higher frequencies. *IEEE Microwave Magazine* **2**, 77–87.
2 **Johnson EO** (1965) Physical limitations on frequency and power parameters of transistors. *IRE International Convention Record* **13**, 27–34.
3 **Shifrin M, Ayasli Y and Katzin P** (1992) A new power amplifier topology with series biasing and power combining of transistors. *IEEE Microwave and Millimeter-wave Monolithic Circuits Symposium Digest*, pp. 39–41.

https://doi.org/10.1017/S1759078718001137 Published online by Cambridge University Press

4 **Jeong J, Pornpromlikit S, Asbeck PM and Kelly D** (2006) A 20 dBm linear RF power amplifier using stacked silicon-on-sapphire MOSFETs. *IEEE Microwave and Wireless Components Letters* **16**, 684–686.

5 **Pornpromlikit S, Jeong J, Presti CD, Scuderi A and Asbeck PM** (2010) A Watt-level stacked-FET linear power amplifier in silicon-on-insulator CMOS. *IEEE Transactions on Microwave Theory and Techniques* **58**, 57–64.

6 **Lee C, Kim Y, Koh Y, Kim J, Seo K, Jeong J and Kwon Y** (2009) A 18 GHz broadband stacked FET power amplifier using 130 nm metamorphic HEMTs. *IEEE Microwave and Wireless Components Letters* **19**, 828–830.

7 **Fritsche D, Wolf R and Ellinger F** (2012) Analysis and design of a stacked power amplifier with very high bandwidth. *IEEE Transactions on Microwave Theory and Techniques* **60**, 3223–3231.

8 **Ezzeddine AK, Huang HC and Singer JL** (2011) UHiFET – a new high-frequency high-voltage device. *IEEE MTT-S International Microwave Symposium*.

9 **Wu HF, Cheng QF, Li XG and Fu HP** (2016) Analysis and design of an ultrabroadband stacked power amplifier in CMOS technology. *IEEE Trans. Circuits and systems II: Express Briefs* **63**, 49–53.

10 **Dabag HT, Hanafi B, Golcuk F, Agah A, Buckwalter JF and Asbeck PM** (2013) Analysis and design of stacked-FET millimeter-wave power amplifiers. *IEEE Transactions on Microwave Theory and Techniques* **61**, 1543–1556.

11 **Agah A, Jayamon JA, Asbeck PM, Larson LE and Buckwalter JF** (2014) Multi-drive stacked-FET power amplifiers at 90 GHz in 45 nm SOI CMOS. *IEEE Journal of Solid-State Circuits* **49**, 1148–1157.

12 **Chakrabarti A and Krishnaswamy H** (2014) High-power high-efficiency class-E-like stacked mmWave PAs in SOI and Bulk CMOS: theory and implementation. *IEEE Transactions on Microwave Theory and Techniques* **62**, 1686–1704.

13 **Kim Y and Kwon Y** (2015) Analysis and design of millimeter-wave power amplifier using stacked-FET structure. *IEEE Transactions on Microwave Theory and Techniques* **63**, 691–702.

14 **Gavell M, Angelov I, Ferndahl M and Zirath H** (2015) A high voltage mm-wave stacked HEMT power amplifier in 0.1 µm InGaAs technology. *IEEE MTT-S International Microwave Symposium*.

15 **Datta K and Hashemi H** (2017) High-breakdown, high-f_{max} multiport stacked-transistor topologies for the W-Band power amplifiers. *IEEE Journal of Solid-State Circuits* **52**, 1305–1319.

16 **Johansen TK, Yan L, Dupuy JY, Nodjiadjim V, Konczykowska A and Riet M** (2013) Millimeter-wave InP DHBT power amplifier based on power-optimized cascode configuration. *Microwave and Optical Technology Letters* **55**, 1178–1182.

17 **Yan L and Johansen TK** (2013) Design of InP DHBT power amplifiers at millimeter-wave frequencies using interstage matched cascode technique. *Microelectronics Journal* **44**, 1231–1237.

18 **Squartecchia M, Midili V, Johansen TK, Dupuy JY, Nodjiadjim V, Riet M and Konczykowska A** (2017) 75 GHz InP DHBT power amplifier based on two-stacked transistors. *Asia Pacific Microwave Conference (APMC), Kuala Lumpur*.

19 **Hadziabdic D, Krozer V and Johansen TK** (2008) Power amplifier design for E-band wireless system communications. *38th European Microwave Conference (EuMC), Amsterdam*.

20 **Griffith Z, Urteaga M, Rowell P and Pierson R** (2015) 340–440 mW broadband, high-efficiency E-band PA's in InP HBT. *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*.

21 **Urteaga M, Griffith Z, Seo M, Hacker J and Rodwell MJW** (2017) InP HBT technologies for THz integrated circuits. *Proceedings of the IEEE* **105**, 1051–1067.

22 **Kassim S and Malek F** (2010) EM/circuit co-simulation: a highly accurate method for microwave amplifier design. *Universal Journal of Computer Science and Engineering Technology* **2**, 127–132.

23 **Thompson M and Moore J** (2015) Challenges and methodologies in EM simulation with circuit models. *IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*.

24 **Johansen TK, Leblanc R, Poulain J and Delmouly V** (2016) Direct extraction of InP/GaAsSb/InP DHBT equivalent-circuit elements from *S*-parameters measured at cut-off and normal bias conditions. *IEEE Transactions on Microwave Theory and Techniques* **64**, 115–124.

25 **Johansen TK, Midili V, Squartecchia M, Zhurbenko V, Nodjiadjim V, Dupuy JY, Riet M and Konczykowska A** (2017) Large-signal modeling of multi-finger InP DHBT devices at millimeter-wave frequencies. *International Workshop on Integrated Nonlinear Microwave and Millimeter-Wave Circuits (INMMiC), Graz*.

26 **Green JE, Tozer RC and David JPR** (2013) Stability in small signal common base amplifiers. *IEEE Transactions on Circuits and Systems-I: Regular Papers* **60**, 846–855.

Michele Squartecchia received his B.Sc. and M.Sc. (*cum laude*) in electronics engineering from the University of L'Aquila, L'Aquila, Italy, in 2010 and 2014, respectively. He is now working towards his Ph.D. at Technical University of Denmark (DTU), Denmark, in collaboration with III-V Lab (Palaiseau, France), a joint lab between Nokia Bell Labs, Thales, and CEA-Leti. In 2018, he joined Bifrost Communications ApS as a circuit designer. His research interests include microwave and mm-wave IC modeling and design for wireless and optical communications.

Tom K. Johansen received his M.S and Ph.D. degrees in electrical engineering from the Technical University of Denmark, Denmark, in 1999 and 2003, respectively. In 1999 he joined the Electromagnetic Systems group, DTU Elektro, Technical University of Denmark, Denmark, where he is currently an Associate Professor. From September 2001 to March 2002 he was a Visiting scholar at the center for wireless communication, University of San Diego, California, Ca. He has spent several external research stays at the Ferdinand Braun Institute (FBH), in Berlin, Germany. His research areas include the modeling of high-frequency solid-state devices, millimeter-wave, and sub-millimeter-wave integrated circuit design.

Jean-Yves Dupuy received the Engineer Degree from the Ecole Nationale Supérieure de l'Electronique et de ses Applications (ENSEA, Cergy, France) in 2005, and the Ph.D. Degree summa cum laude from University of Cergy-Pontoise (France) in 2015, both in Electrical Engineering. He joined III-V Lab (Palaiseau, France) in 2005, now a joint lab between Nokia Bell Labs, Thales and CEA-Leti. He is currently leading the High-Speed Electronics Research Department, covering modeling, design, fabrication, packaging, and characterization of high-performance semiconductor devices, integrated circuits and modules, especially in InP DHBT technology, at microwave and millimeter wave frequencies, aiming at pioneering high-speed analog and digital interfaces in performance-critical optoelectronic and RF systems. Dr. Dupuy has been a participant to the 2013 EU-US Frontiers-Of-Engineering Symposium and a co-recipient of the IET 2017 Electronics Letters Premium Award. He has co-authored more than 100 scientific publications and holds two patents.

Virginio Midili received his B.Sc. in Electrical Engineering from Politecnico di Milano, Milan, Italy, in 2010 and his M.Sc. in Micro and Nanotechnology from Aalto University, Helsinki, Finland, in 2012. He received an industrial Ph.D. Degree from the Technical University of Denmark working in collaboration with Nokia Bell-Labs, III-V Lab in France. His research focused on the optimization of InP DHBT transistors for power amplifiers at mm-wave frequencies.

https://doi.org/10.1017/S1759078718001137 Published online by Cambridge University Press

Virginie Nodjiadjim received the Ph.D. degree in electronic engineering from the University of Lille I, Lille, France, in 2009. In 2009, she joined Alcatel-Thales III-V Labs (currently III-V Lab), Bell Labs, Marcoussis, France, as a Research Engineer, where she has studied compound semiconductor heterojunction bipolar transistors. She is currently in charge of the InP DHBT development: structure and design optimization, characterization, and modeling.

Muriel Riet received the Ph.D. degree in electronic engineering from the University of Paris XI, Paris, France, in 1985. In 1985, she joined CNET, a research center of France Telecom, where she has studied compound semiconductor heterojunction bipolar transistors. Since 1998, she has been in charge of InP HBT technology for high-bit-rate optical communications up to 40 Gb/s in the III-V Lab, Marcoussis, France.

Agnieszka Konczykowska is in charge of microelectronic design activity at III-V Lab, Bell Labs, Thales Research and Technology and CEA/Leti joint laboratory, Marcoussis in France. She is presently an active researcher in the domain of components and circuits for telecommunication systems, in particular for optical and wireless communications. She is author and co-author of over 200 publications and six patents. From 1995 to 1999, she was the president of European Circuit Society. She is an IEEE Fellow.

https://doi.org/10.1017/S1759078718001137 Published online by Cambridge University Press