Low power front-end architecture dedicated to the multistandard simultaneous reception

IOAN BURCIU[1,2], GUILLAUME VILLEMAUD[1], JACQUES VERDIER[1] AND MATTHIEU GAUTIER[1,2]

In this paper, we address the architecture of multistandard simultaneous reception receivers and we aim to reduce the complexity and the power consumption of the analog front-end. To this end, we propose an architecture using the double orthogonal translation technique in order to multiplex two signals received on different frequency bands. A study case concerning the simultaneous reception of 802.11 g and Universal Mobile Telecommunications System (UMTS) signals is developed in this article. Theoretical and simulation results show that this type of multiplexing does not significantly influence the evolution of the signal-to-noise ratio of the signals. In the same time a 30% reduction of the power consumption is expected as well as a significant reduction of the complexity.

I. INTRODUCTION

Nowadays the market presents a real interest in the development of interconnected telecommunication networks based on radiofrequency (RF) systems. In particular, we can note a multiplication of new RF standards such as WiFi, WiMax or the 3G and beyond. Along with the already existing ones, these new standards allow the operators to offer new and better services in terms of speed, quality, and availability. Consequently, in order to handle this important diversity of telecommunication techniques, there is a growing interest in developing new front-end architectures capable of processing several standards.

For the multistandard research domain we can distinguish two different categories of receivers: non-simultaneous receivers using switching techniques [1–5] and simultaneous processing receivers [6]. The state of the art of the multistandard simultaneous reception architectures uses the front-end stack-up technique – each chain being dedicated to the reception of only one standard. Nonetheless, this architecture is characterized by some inconveniences such as the bad complexity-performance trade-off, but also the price and the physical size.

The goal of the architecture proposed in this paper, subject of a patent pending [7], is to answer a need generated by the ambient or sensor network domain, while also not being restricted to that alone. One of its choke points is the creation of a powerful gateway node to the exterior world. A solution to this problem would be the development of a gateway node that integrates a multistandards simultaneous reception front-end in order to relay the information carried by a short-range standard (sensor network using a WiFi standard in our study case) using a second, long-range standard (UMTS standard).

Several ideas concerning multistandard single front-end receiver, capable of simultaneously processing two standards, have been recently patented [6]. Using only one front-end reduces the complexity; nevertheless, additional problems linked to the analog to digital conversion appeared. The main idea already patented is to decrease the spectrum occupied by the two standards, in the RF domain. This technique relies on two dedicated parallel frequency translations of the standards bands in order to bring them closer – without overlapping their spectrums – at intermediate frequency. Compared to the front-end stack-up, the baseband bandwidth that has to be digitized is clearly increased, imposing thus supplementary constraints to the analog to digital converters (ADC).

The structure assessed in this article implements a novel and innovating multistandard simultaneous receiving architecture using a single front-end. This architecture uses the double orthogonal translation technique [8, 9] in order to multiplex the two standards signals by completely overlapping their spectrums at an intermediate frequency. After the second orthogonal frequency translation (IQ translation) the baseband signals are digitized, and then are processed by a signal processing block that separately demultiplexes the baseband component of the two standards. A key point of this structure is the orthogonal mismatches of the translation blocks, which can be digitally mitigated by a proper signal processing [10–12]. In addition, the image frequency impairment is no longer a problem as each of the standards occupies the image band of the other.

This paper consists of three parts. Following this introduction, Section II describes the double IQ principle used by the image frequency rejection technique. In Section III, a multistandard front-end architecture, based on orthogonal multiplexing of the two branches, is presented. The last section details the performance evaluation of such a receiver by showing some significant simulation results as well as by presenting the implementation of a MMSE method [13, 14] dedicated to the mitigation of the IQ mismatches. Finally, conclusions of this study are drawn and the follow-up to this work is provided.

[1]University of Lyon, INRIA-CNRS, INSA-Lyon, CITI-INL, F-69621, France.
[2]Orange Labs, 28 Chemin du Vieux Chêne, 38243 Meylan Cedex, France.
Corresponding author:
I. Burciu
Email: ioanburciu@yahoo.fr

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II. DOUBLE IQ STRUCTURE

In wireless telecommunications, the integration of IQ base-band translation structures in the receiver chain has become a common procedure. The simple IQ architecture is usually used in the receiver front-end design in order to reduce the bandwidth of baseband signals treated by the ADC.

Meanwhile, this orthogonal frequency translation technique is also used to eliminate the image frequency default during the translation steps of heterodyne front-end architectures [9, 10]. The image frequency rejection technique, shown in Fig. 1, consists in using two orthogonal frequency translations of the signal. In order to realize this double translation, three IQ translation blocks are needed. After the double orthogonal translation, a signal processing block uses the four baseband signals to eliminate the image frequency signal.

The structure assessed here relies on the advantage of orthogonalizing the useful signal $s_u(t)$ and the signal occupying its image frequency band $s_{Im}(t)$. Even though the spectrums of the two signals are completely overlapped after the first frequency translation, this orthogonalization allows the baseband processing to theoretically eliminate the image frequency component while reconstructing the useful one.

In order to realize a theoretical study of the double IQ structure presented in Fig. 1, the components $s_u(t)$, $s_{Im}(t)$ of the input $s(t)$ are considered as RF domain signals. Therefore, these signals can be modeled by the following:

$$s_u(t) = I_u(t)\cos(2\pi f_u t) + Q_u(t)\sin(2\pi f_u t), \quad (1)$$

$$s_{Im}(t) = I_{Im}(t)\cos(2\pi f_{Im} t) + Q_{Im}(t)\sin(2\pi f_{Im} t), \quad (2)$$

where $\{I_k(t) + jQ_k(t), j^2 = -1, k = (u;Im)\}$ are the baseband complex envelopes.

Each IQ translation structure multiplies the input by two $90°$ shifted sinusoids provided by the frequency synthesizers. The first IQ block uses a local oscillator having a frequency $f_{LO_1} = (f_u + f_{Im})/2$. The two output signals of the first IQ translation structure $s_I(t)$ and $s_Q(t)$ can be defined by

$$s_I(t) = LP[\cos(2\pi f_{LO_1} t)s(t)]$$

$$= [I_u(t) + I_{Im}(t)]\frac{\cos(2\pi f_{IF} t)}{2}$$

$$+ [Q_{Im}(t) - Q_u(t)]\frac{\sin(2\pi f_{IF} t)}{2}, \quad (3)$$

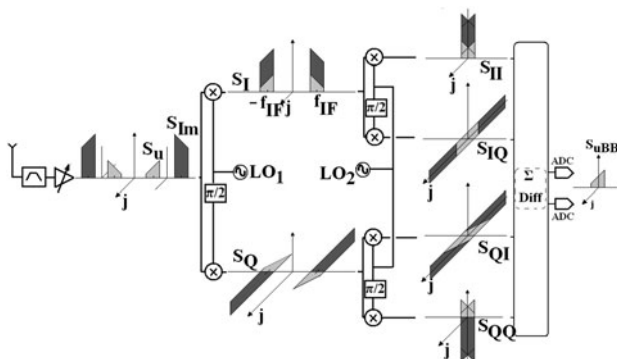$$s_Q(t) = LP[\sin(2\pi f_{LO_1} t)s(t)]$$

$$= [I_u(t) - I_{Im}(t)]\frac{\sin(2\pi f_{IF} t)}{2}$$

$$+ [Q_u(t) + Q_{Im}(t)]\frac{\cos(2\pi f_{IF} t)}{2}, \quad (4)$$

where $LP[.]$ stands for low-pass filter and where the intermediate frequency $f_{IF} = f_u - f_{LO_1} = f_{LO_1} - f_{Im}$. These equations highlight the overlapping of the useful spectrum and the image band spectrum after the intermediate frequency translation, as shown in Fig. 1.

In the second IQ frequency translation step, each of the two signals $s_I(t)$ and $s_Q(t)$ are separately multiplied by two $90°$ shifted sinusoids. As the frequency of the local oscillators is chosen to be $f_{LO_2} = f_{IF}$, the four output signals of this second IQ translation block are translated in the baseband domain and are characterized by the equations

$$s_{II}(t) = LP[\cos(2\pi f_{IF} t)s_I(t)] = \frac{I_u(t)}{4} + \frac{I_{Im}(t)}{4}, \quad (5)$$

$$s_{IQ}(t) = LP[\sin(2\pi f_{IF} t)s_I(t)] = \frac{Q_u(t)}{4} - \frac{Q_{Im}(t)}{4}, \quad (6)$$

$$s_{QI}(t) = LP[\cos(2\pi f_{IF} t)s_Q(t)] = \frac{Q_u(t)}{4} + \frac{Q_{Im}(t)}{4}, \quad (7)$$

$$s_{QQ}(t) = LP[\sin(2\pi f_{IF} t)s_Q(t)] = \frac{I_u(t)}{4} - \frac{I_{Im}(t)}{4}. \quad (8)$$

The four output signals contain the multiplexed baseband translated information of the two RF components $s_u(t)$ and $s_{Im}(t)$. For a mono-standard image rejection front-end architecture, only the useful component $s_u(t)$ is interesting, but both of the baseband translated information can be separately demultiplexed by two different signal processings, detailed by

$$s_{uBB}(t) = s_{II}(t) + s_{QQ}(t) + j[s_{QI}(t) - s_{IQ}(t)], \quad (9)$$

$$s_{ImBB}(t) = s_{II}(t) - s_{QQ}(t) + j[s_{IQ}(t) + s_{QI}(t)]. \quad (10)$$

Each of these series of operations reconstructs one of the two components while eliminating the other. In fact, by developing (9) and (10) using (5)–(8), we obtain $\{s_{kBB}(t) = I_k(t) + jQ_k(t), j^2 = -1, k = (u;Im)\}$, the same baseband characterization as that of the RF input signals $s_u(t)$ and $s_{Im}(t)$.

The image rejection technique presented here allows a theoretically perfect rejection of the image band signal. In fact, the image rejection ratio (IRR) depends on the gain and phase mismatches between the two branches of the IQ translation structures, and especially on the mismatches relied to the first one as this frequency translation is generally the largest. For the receivers using heterodyne process, the image rejection ratio is the ratio of the intermediate frequency signal level produced by the desired input signal to that produced by the image band signal. Depending on the choice of the intermediate frequency, each standard needs a certain amount of IRR.

The orthogonal mismatches are caused by design and layout defaults such as different line lengths between the two branches and non-identical mixers, which generate phase and respectively gain mismatches [12]. Supposing that the first IQ stage

Fig. 1. Spectral evolution of the signals in a double IQ image frequency rejection architecture ($j^2 = -1$).

has a gain mismatch ΔA and a phase mismatch $\Delta \theta$, the final IRR can be modeled by the equation below [11]:

$$IRR \text{ (dB)} = 10 \log \left[\frac{1 + (1 + \Delta A)^2 + 2(1 + \Delta A) \cos (\Delta \theta)}{1 + (1 + \Delta A)^2 - 2(1 + \Delta A) \cos (\Delta \theta)} \right] \quad (11)$$

In order to provide sufficiently high image rejection to meet the requirements of the WLAN 802.11 g standard, an IRR of at least 80 dB is needed. Other wireless communication standards have similar or more severe requirements [10]. For a receiver implementing this kind of architecture, the image rejection is accomplished through a combination between the front-end's input elements: antenna, external RF filter, LNA (low noise amplifier) on one hand, and the image rejection technique achieved by the double IQ configuration on the other hand. The state of the art front-end's input elements can realize an image frequency rejection of up to 40 dB. Therefore, in order to achieve a total 80 dB level of IRR it is shown in [11] that only 0.01 dB gain mismatch and 0.1° of phase mismatch are allowed for each of the IQ blocks. In fact, for these mismatch conditions, the remaining 40 dB of IRR are realized using the image rejection technique.

This high degree of matching is not achievable using only good design and layout techniques. In order to obtain the required 40 dB of rejection level, additional minimum mean square error (MMSE) method have to be used. Such a method has been developed in the digital domain using a least mean square (LMS) algorithm [11]. The results show an IRR level due to the front-end architecture reaching up to 70 dB. Therefore, we can assume that the total IRR of the receiver reaches 110 dB. This level of image rejection allows the elimination of the external band-pass filter, common in a classical receiver design.

In conclusion, the state of the art of the double IQ monostandard architectures offers a good trade-off between the use of digital signal processing and the complexity of the analog part of the receiver.

III. HIGH IMAGE REJECTION MULTIBAND RECEIVER USING A DOUBLE IQ FRONT-END ARCHITECTURE

A) Innovation on the use of double IQ architecture in the simultaneous reception of two frequency bands

All the studies presenting the integration of the double IQ technique use this method in order to cancel the image frequency default in a mono-standard reception front-end. All of them are using a series of basic operations (additions and subtractions) between the four baseband signals obtained after two orthogonal translation steps. This signal processing allows the elimination of the image frequency component and the reconstruction of the useful frequency component.

This section assesses the use of the double orthogonal translation technique to develop a multistandard simultaneous reception front-end. In fact, the main idea is to consider that the signal from the image band becomes another
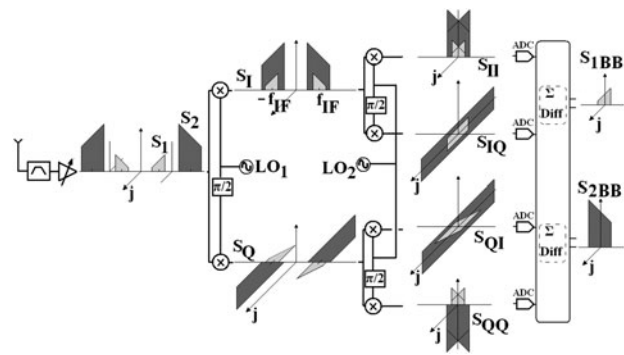

Fig. 2. Double IQ structure able of receiving two different signals ($j^2 = -1$).

useful signal. The architecture and the spectrum evolution of such a receiver, capable of treating simultaneously two standards, are developed in Fig. 2. The input, composed of two different frequency bands signals, is processed by a first orthogonal translation block. The frequency of the oscillator used by this stage is cleverly chosen in such a manner that each of the two useful signals occupies a spectrum in the image band of the other. Therefore they are translated around the same intermediate frequency by the first IQ block. After this first translation, the bandwidth of the useful signal is equal to the larger of the two initial bandwidths. After the second translation stage, the four baseband signals thus obtained are used by a signal processing block to demultiplex the two initial useful signals.

Two parallel processing are made, each of them composed of a series of basic operations, as described in the previous section by (9) and (10). Each of the two parallel processing reconstructs one of the two useful signals, while rejecting the other. As a result, the output signals of this final block are the baseband translated components of the two useful signals. The theoretical development of this process is the same as the one of the image rejection structure presented in the previous section. Instead of considering that the RF input signal is composed of a useful signal $s_u(t)$ and its image band signal $s_{Im}(t)$, for this multistandard architecture the two signals $s_1(t)$ and $s_2(t)$ are considered to be useful, each of them being the image signal for the other. The difference consists in the fact that, if the monostandard image rejection architecture implements only one of the signals' processing in order to recover the useful signal, the proposed architecture implements two dedicated signal processing in order to recover both useful signals. As this dual signal processing is easier to implement in the digital domain, the analog-to-digital conversion step is realized after the second translation.

Similarly to the case of the image band rejection, the rejection of the complementary signal, which is theoretically perfect, depends on the degree of the matching between the orthogonal branches of the IQ translation blocks. If the image frequency rejection was accomplished through a combination between the analog parts (RF filter, LNA) and the image rejection configuration, the rejection of the complementary signal relies here only on the structure rejection. Therefore, the maximum rejection level that can be reached using only the state of the art IQ mixers is only 40 dB [9]. By using an additional MMSE method to reduce the mismatch between the orthogonal branches of the IQ blocks, the rejection factor can reach up to 70 dB. Depending on the choice

of the telecommunication standards, this rejection level may not be sufficient. Therefore, the choice of the standards supported by a receiver implementing this type of architecture could be limited by this rejection factor.

Another sensible point of this structure is the gain control stage. For a classical monostandard front-end, the automatic gain control (AGC) is an adaptive system. The average output signal level is fed back to adjust the gain to an appropriate level for a range of input signal levels. The automatic gain control adjusts the power lever measured in the useful signal frequency band. For this type of multistandard architecture, the gain control cannot separately adjust the power of the two signals. In consequence, severe dynamic constraints will be imposed to the sampling stage as the ADC dynamics are strictly linked to the signal power variation.

In conclusion, this type of multistandard simultaneous reception architecture confers a low complexity to the analog part of the receiver, but requires a special signal processing in order to have a relatively good performance. On the other hand, this structure requires severe implementation conditions such as those imposed to ADC by the position of the automatic gain control.

B) High image rejection multistandard receiver using a double IQ front-end architecture

One of the weak points of the previously presented structure is the gain control stage that cannot separately control the power of the two different frequency bands. This inappropriate power control can lead to poor performance during the final digital processing stage. In order to improve this aspect, we propose to parallelize the input stages of the front-end, each branch being dedicated to the processing of only one standard. This way, the automatic gain control can separately handle the two signals, before realizing the first orthogonal frequency translation, as shown in Fig. 3.

The parallelization of the input stages of the front-end imposes the use of two dedicated antennas, two dedicated RF band filters, and two dedicated LNAs. The gain control stage is realized by the input stages, each LNA being dedicated to the gain control of one of the signal. Once the two signals are well filtered and amplified, an addition of the two outputs is made. The resulting signal is then processed by a double orthogonal translation structure similar to that presented before.

In order to estimate the performance of such architecture, especially in terms of complementary signal rejection, a study concerning the reception of one of the signals $s_1(t)$ will be done, the other signal $s_2(t)$ reception being treated by analogy.

In comparison to the previous architecture, the addition of the parallel branches' outputs generates supplementary parasitic signals that can degrade the final signal-to-noise ratio (SNR) of the two useful signals. Each of the two antennas receives a signal composed of two components $-s_1(t) + s'_2(t)$ for the A_1 antenna and $s'_1(t) + s_2(t)$ for the A_2 antenna, where $s_1(t)$ and $s'_1(t)$ are the same transmitted signals after two different propagation channels, as well as $s_2(t)$ and $s'_2(t)$. The parasitic components $s'_2(t)$ and $s'_1(t)$ are filtered by the input stage of each dedicated branch – antenna, RF band filter, LNA – but even when attenuated like this, these components have to be taken into account while studying the useful signals' SNR evolution.

In fact, the output signal of the adder is mainly composed of four components:

$$Adder_{out}(t) = G_1 s_1(t) + G_2 s_2(t) + G'_1 s'_1(t) + G'_2 s'_2(t), \quad (12)$$

where the coefficients G_1, G_2, G'_1, and G'_2 are the gains that the two input parallel branches of the receiver induce to each of the four components.

In order to evaluate the SNR evolution of the useful signal $s1BB(t)$ after the demultiplexing stage, the evolution of the parasitic signals $s'1(t)$, $s2(t)$, and $s'2(t)$ compared to that of the useful signal $s1(t)$ have to be taken into account:

– The $s'_2(t)$ signal is attenuated by the input blocks of the branch dedicated to the treatment of $s_1(t)$. The state of the art of the antennas, of the RF band filters and of the LNA can generate 40 dB of rejection of $s'_2(t)$ for an architecture such as that of Fig. 3. In addition to these 40 dB of initial rejection, the double IQ structure, associated with a MMSE digital method, can realize up to 70 dB of rejection of the signal from the image band. This means a rejection of up to 110 dB of the parasitic signal $s'_2(t)$.

– The $s_2(t)$ signal undergoes up to 70 dB of rejection compared to the useful signal $s_1(t)$. This rejection is generated by the double IQ structure, similar to that of $s'_2(t)$, as the two signals occupy the same frequency band after the addition of the two branches. In addition to this rejection, another element to be taken into account, when studying the influence of $s_2(t)$ on the SNR of $s_1(t)$, is the dedicated power control stage. In fact, the worst case scenario is characterized by the fact that $s_1(t)$ is at its lowest power level and the parasitic signal $s_2(t)$ is at its highest. This means that $s_2(t)$ has its highest effect on the degradation of the useful signal. On the other hand, the power control will amplify $s_1(t)$ compared to $s_2(t)$ before the addition step. The influence of the parasitic signal on the useful signal is therefore decreased. The state of the art of the power control [15] can provide up to 35 dB between the minimum and the maximum amplification. Therefore, for the worst case scenario the $s_2(t)$ signal undergoes a 105 dB rejection compared to the useful signal $s_1(t)$.

– The $s'_1(t)$ signal, along with $s_2(t)$, is one of the two components of the RF signal received by the A_2 antenna. This signal does not undergo a rejection due to the double IQ structure as it occupies the same frequency band as the useful signal after the addition step. Compared to the useful signal $s_1(t)$, the only rejection that $s'_1(t)$ will undergo is realized by the input elements of the front-end. In fact, as this signal is received by the $s_2(t)$ dedicated branch, the input elements will realize an attenuation of up to 40 dB. As $s'_1(t)$ and the useful signal $s_1(t)$ are not received by the same antenna, even if they are generated by the same transmitter, a phase shift and a gain shift between the two signals appears during the hertzian transmission. For an additive white Gaussian noise (AWGN) transmission channel, the phase shift between the two signals can go from 0 to 360°, but the gain shift can be ignored. For this case, where the two signals $s'_1(t)$ and $s_1(t)$ have the same power level at the input of the front-end, the 40 dB attenuation of the parasitic signal $s'_1(t)$ achieved before the addition step ensures a 40 dB SNR of the useful signal $s_1(t)$ in the baseband domain. This SNR level induces a very good reception quality. In the case of a
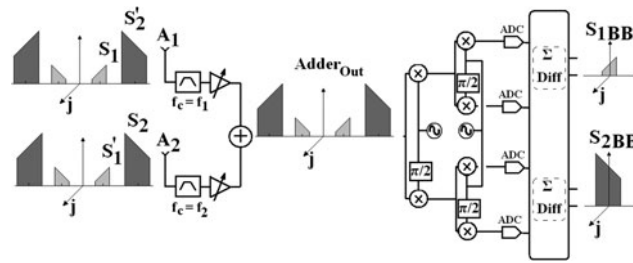
Fig. 3. High complementary standard rejection architecture ($j^2 = -1$).

multipath channel, the gain shift cannot be ignored when treating a multi-antenna reception. This is due to the spatial diversity of a multi-antenna system. Meanwhile, if the spacing between the two antennas is little enough, the gain shift between the components of the same signal can be neglected. Therefore, the conclusions are similar to those of the AWGN channel scenario.

Considering all these arguments concerning the additional parasitic components, it can be considered that the SNR evolution of the useful signals is the same as that of a signal received by a front-end stack-up receiver. Therefore, the single front-end multistandard simultaneous reception structure presents similar performance as a front-end stack-up structure. Moreover, a power-complexity comparison study reveals that the single front-end structure is less complex and it realizes a 30% power consumption gain – more details could be found in [16]. Furthermore, another of the advantages of the single front-end receiver is the elimination of the image rejection RF filters. This represents a real complexity gain as these external components, used to mitigate the impact of the image band signal, can not be integrated on-chip. In the proposed architecture, these components are replaced by a cheaper, on-chip and especially more flexible signal processing.

IV. EVALUATION AND PERFORMANCE

The high image rejection multistandard receiver using a double IQ front-end architecture allows the simultaneous reception of two different frequency bands. In order to validate the theoretical study, a first implementation was simulated using the ADS software (advanced design system) provided by Agilent Technologies [17]. This simulation platform allows a very realistic and trustworthy evaluation of expected performance prior to any prototyping. The selection of the standards used for this implementation was influenced by their complexity and their deployment as well as by their

complementarities in terms of transmission range. These parameters, along with a direct utility of such a structure in the sensor network domain, directed our choice towards the IEEE 802.11 g [18] and the WCDMA-FDD [19]. Regarding this choice, an important point that should be underlined is the implementation constraints imposed by the standards dynamics, but especially by those of the WCDMA-FDD. These dynamics constraints make this standards' choice implementation the most delicate.

In order to realize a good performance comparison between the multistandard single frond-end receiver and the front-end stack-up, the models of the blocks used during the simulation have the same typical metrics (gain, noise figure, 1 dB compression point, third-order interception point) for both cases. The global characterization of the multistandard single front-end receiver is presented in Table 1.

During this study, it will be considered that the metrics of the blocks used by the two parallel input branches are similar and therefore the performance offered by the front-end for the two standards is identical in terms of noise figure, gain, and third-order intercept point.

Table 1. Metrics used for the simulation of the multistandard single front-end receiver.

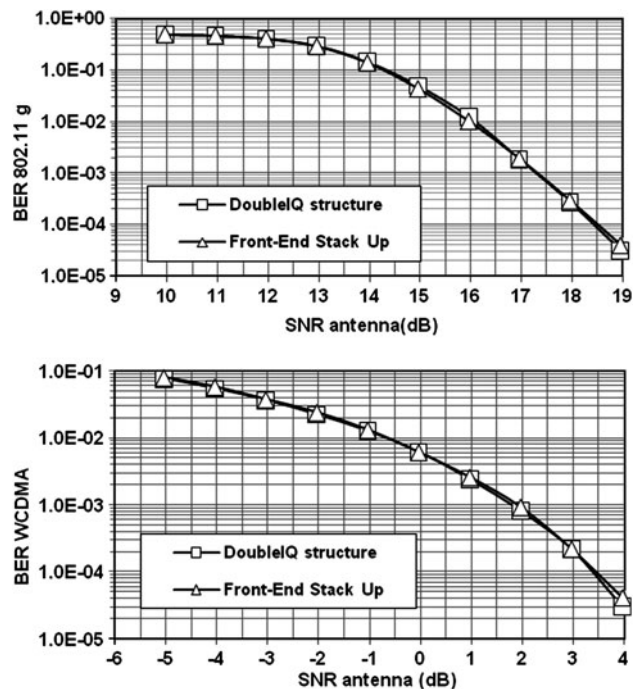| Symbol	SI unit	Value
NF	dB	6
IIP3	dBm	−12
Maximal gain AGC	dB	25
Minimal gain AGC	dB	−10

Fig. 4. 802.11g and WCDMA BER evolutions during multistandards simultaneous reception using the front-end stack-up and the single front-end receiver.
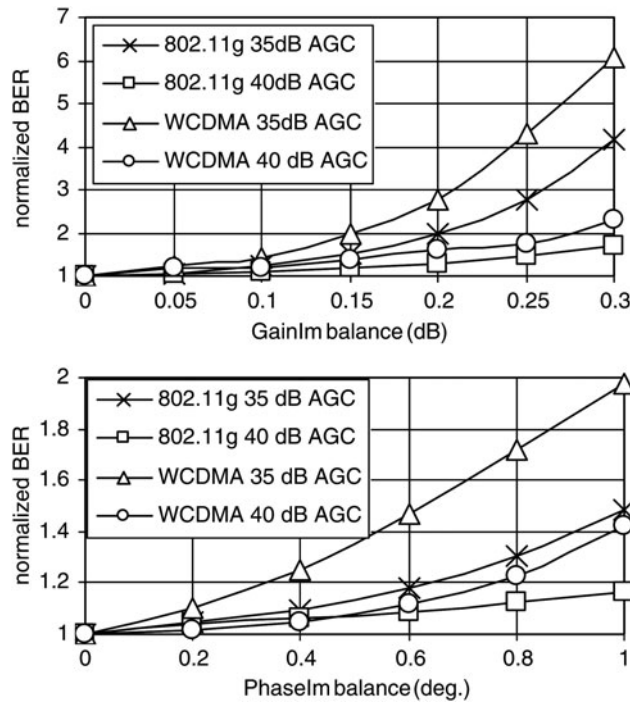
Fig. 5. 802.11g and WCDMA BER evolutions versus gain and phase imbalance of the IQ translation blocks. Two series are dedicated to each BER evolution for an AGC gain dynamics of 35 and 40 dB, respectively.

A) Evaluation of the impact of the IQ mismatches

The first results – Fig. 4 – represent the evolution of the two standards bit error rate (BER) depending on their SNR level at the antenna. This BER evolution was observed using both the multistandard single front-end and the front-end stack-up structures as receivers. Here, the wireless transmission channel was chosen to be AWGN whereas the translation blocks are considered to be ideal in terms of IQ mismatches. During the simulation of the reception of one of the standards, the antenna power level of the complementary standard is set to the maximum level so that its parasitic influence is the highest. Under these conditions the two standards BER evolutions are almost identical for both types of receivers.

In the third section, we have developed a theoretical study that underlines the importance of the IQ mismatches for the performance of a receiver using a double orthogonal translation. For this type of receiver, it is necessary to realize a good rejection of the image frequency band. In fact, this rejection relies on two different sources: the gain control realized in the RF domain and the image band rejection realized by the double IQ structure, depending on the IQ mismatches. In order to estimate the impact of the orthogonal mismatches on the evolution of the two standards BER a second set of simulations is realized. The receiver's metrics used during these simulations are the same as those presented in Table 1, except for the gain dynamics of the AGC which take two different values of 35 and 40 dB.

Concerning the power level of the signals at the antenna, while testing the influence of the IQ mismatches on the BER of one of the standards, the power level of the complementary standard is maximal, whereas the power level of the concerned standard is at its reference level (the minimum power level that ensures a certain quality of service). For our study case, the concerned power levels lead to a 10^{-3} level of BER, when considering no IQ mismatch conditions.

For each standard, two normalized BER evolutions are presented in Fig. 5. Depending on the AGC dynamics, the complementary signal will be attenuated by a certain amount compared to the useful signal. Another rejection step is then realized by the IQ structure, this one being dependent of the orthogonal mismatches.

Simulations show that the BER performance of the receiver depends, on one hand, on the AGC gain dynamics and, on the other hand, on the orthogonal IQ mismatches. For an AGC gain dynamics varying from the state of the art 35–40 dB, the BER can triple for the same power levels and mismatch configuration. It can also be observed that, under significant orthogonal mismatches conditions, the influence of the complementary standard (at its maximum power level) on the useful one's SNR leads to a BER six times higher.
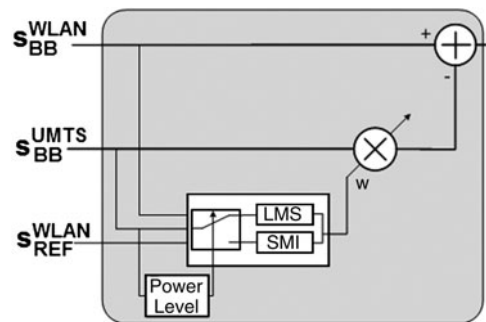

Fig. 6. Digital context-aware method used to mitigate the influence of IQ mismatches in a double orthogonal translation receiver.

B) Digital algorithm dedicated to the mitigation of the IQ defaults influence

In order to mitigate the influence of the IQ mismatches on the quality of the signals processed by the proposed receiver structure, a digital adaptive method has been implemented. It is composed of a mix between a light power consumption iterative LMS algorithm and a power greedier single matrix inversion (SMI) algorithm.

The scenario considered here involves a continuous reception of a 802.11 g signal while the WCDMA (UMTS) signal at the antenna has a random power level. It is also supposed that the IQ mismatches have a slow variation (with respect to the frame duration).

Based on (11) and on the system model presented in the third section, the two signals s_{BB}^{WLAN} and s_{BB}^{UMTS}, obtained after the digital demodulation can be modeled by the following equation:

$$s_{BB}^{WLAN} = \alpha s_{RF}^{WLAN} + \beta s_{RF}^{WLAN*}, \tag{13}$$

$$s_{BB}^{UMTS} = \alpha s_{RF}^{UMTS} - \beta s_{RF}^{WLAN*}, \tag{14}$$

where s_{RF}^{WLAN} and s_{RF}^{UMTS} are the baseband translation of the RF signals at the output of the AGC stages.

The α and β coefficients depend directly on the gain mismatch ΔA and on the phase mismatch $\Delta\theta$:

$$\alpha = (1 + (1 + \Delta A)e^{-j\Delta\theta})/2, \tag{15}$$

$$\beta = (1 - (1 + \Delta A)e^{j\Delta\theta})/2. \tag{16}$$

The α/β ratio is directly proportional to the IRR, as it represents the attenuation of the image band signal compared to the useful baseband signal. In the followings, we choose to focus on the reception of the WLAN signal and to consider the UMTS signal as interference, the UMTS dedicated method being analog to that used for the WLAN. For this study case, the adaptive correction method is estimating β by a weight w.

This estimation uses the two signals from the output of the digital demultiplexing stage and a known training sequence – two long preamble symbols of the 802.11 g signal. Once the estimation step is finished, the weight is multiplied with the s_{BB}^{UMTS} signal and the result is subtracted from s_{BB}^{WLAN}, as shown in Fig. 6. Consequently, the interfering s_{RF}^{UMTS} component of the s_{BB}^{WLAN} signal becomes insignificant.

The estimation is done by a context-aware method using either a LMS or a SMI algorithm [13, 14]. The LMS algorithm is an iterative method using the MMSE technique in order to minimize the difference between the received signal and a training sequence. For our study case, each of the iterations implies the following operations:

$$s_{OUT}(n) = s_{BB}^{WLAN}(n) - w(n)s_{BB}^{UMTS*}(n), \tag{17}$$

$$error(n) = s_{OUT}(n) - s_{REF}^{WLAN}(n),$$

$$w(n+1) = w(n) + \mu\, error\, s_{BB}^{UMTS*}(n),$$

where s_{REF}^{WLAN} is the training sequence of the 802.11 g signal and μ is the algorithm step size.

Simulation results show that the algorithm manages to mitigate the influence of IQ impairments. In addition, for a continuous 802.11 g and UMTS simultaneous reception, LMS manages to adapt to the slow IQ impairments variation. A major drawback of the LMS algorithm is the small precision for the case of a weak power level of the complementary UMTS signal. But this is not a major problem for this input power level case. The real inconvenient is related to the convergence of the LMS algorithm. In fact, if the power level of the UMTS dedicated branch changes from -107dBm to a significant level (about -80 dBm), the LMS algorithm has to converge once again in order to offer a good precision. Simulation results show that, in order to converge to an estimation precision allowing a supplementary 20 dB of IRR, the algorithm needs up to 10 000 samples. Knowing that the two 802.11 g preamble symbols provide 128 samples of training sequence per frame, it takes up to 80 frames for the algorithm in order to grant a sufficient precision. We conclude that this algorithm can provide an adaptive mitigation of the influence of the IQ impairments, but it cannot manage an arbitrary power variation of the complementary signal.

In order to overcome this sensitivity of the LMS algorithm, a solution is the use of this adaptive algorithm only when the complementary signal s_{BB}^{UMTS} has a given power level. But this means that during the absence of the UMTS signal, the algorithm cannot adapt the estimation to the variation of the IQ mismatches. Therefore, each time the UMTS signal power changes from an insignificant to a consistent level, the LMS has to converge in order to evaluate once again the IQ mismatches that could have changed during the absence of the UMTS signal. The chosen solution in order to tackle the UMTS signal fluctuating power level is the use of a SMI algorithm [14]. The advantage of this algorithm is its estimating performance when using a relatively small training sequence – 128 samples of the two 802.11 g preamble
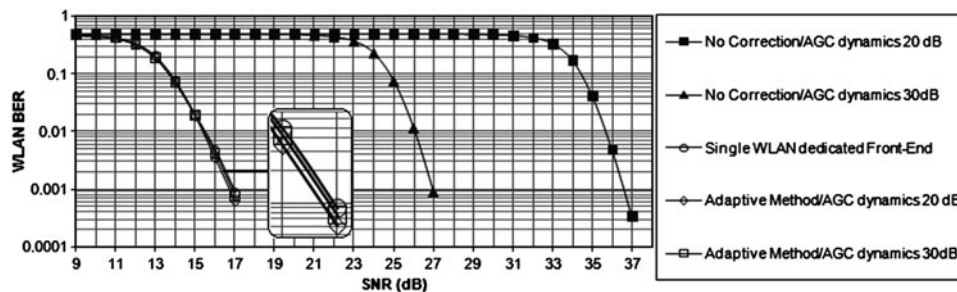

Fig. 7. WLAN BER versus SNR for different configurations and for different study conditions: different AGC dynamics, implantation of the MMSE method dedicated to the mitigation of the IQ mismatch influence.
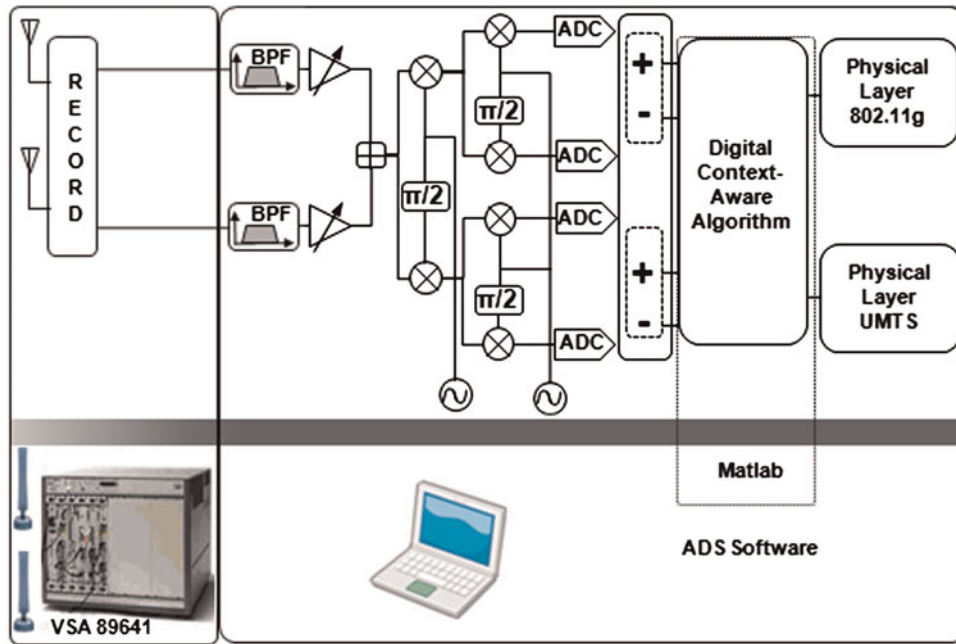
Fig. 8. RF test platform used to realize a simultaneous 802.11 g and UMTS reception.

symbols for our study case. Compared to the continuous estimation approach of the LMS algorithm, the SMI has a block adaptive approach. Instead of using an iterative approach in order to estimate w, it uses the entire training sequence for a matrix inversion operation. Simulations results show that a training sequence of 128 samples is sufficient for the SMI algorithm in order to ensure a supplementary 20 dB rejection of the UMTS complementary signal. However, the main drawback of this type of algorithm is its complexity and power consumption compared to the LMS. Consequently, the optimum solution for an adaptive IQ mismatch correction algorithm is a context-aware method depending on the power level P_{UMTS} of s_{BB}^{UMTS}:

– If the current P_{UMTS} is bigger than a chosen detection level, the decision on which algorithm to be activated depends on the P_{UMTS} level of the previous frame:
  ○ If it was smaller than the detection level, the SMI is activated in order to find the optimum w weight by using only one 128 samples training sequence.
  ○ If it was bigger than the detection level, the LMS algorithm is activated in order to be able to adapt to the IQ mismatches slow variation.
– If P_{UMTS} is smaller than a trigger level, none of the two algorithms is activated in order to estimate the w weight.

C) Results

This context adaptive method was implemented using Matlab software. In the beginning, in order to have more eloquent results, this implementation was incorporated in an ADS/ Matlab co-simulation platform that includes an accurate ADS model of the analog double orthogonal front-end. Figure 7 presents several BER evolutions as function of the 802.11 g signal's SNR. These results reveal that, for different levels of the gain control and therefore of the interfering signal, the influence of the IQ mismatches – the ADS model integers constant 0.3 dB and 1° of gain and phase missmatch, respectevly – is mitigated by the digital adaptive method.

Furthermore, the performance of the proposed architecture is compared to those of a dedicated front-end stack-up. When the MMSE method is used along with the proposed structure, the simulation shows that the performance is identical with those of the front-end stack-up.

In order to further validate these simulation results we used a RF platform that integrates a real transmision channel. On the emmiter side, this platform is composed of two E4438C signal generators, capable of realizing a simultaneous transmission of an UMTS and a 802.11 g signals. The measurements were made by using a real line of sight channel close to the AWGN conditions. In order to realize the simulataneous reception of the 802.11 g and UMTS signals, the two RF signals are first recorded using a 89600 vector signal analyzer. The two recorded RF signals are processed using the ADS software provided by Agilent technologies [10] (Fig. 8). During this measurements campaign, we focused on the 802.11 g reception while the UMTS signal is considered as interfering. In order to validate the context awareness of the adaptive method, the source generating the interfering signal is arbitrarily turned on. The power level for this source is chosen in such a manner that the UMTS interfering signal has a power level of −30 dBm at the input of the receiver. The results presented in Fig. 7 are validated for a BER going from 10^{-2} to 10^{-3}, the MMSE algorithm allows to the double IQ structure to overcome to the IQ mismatch sensibility and to reach the performance of the dedicated front-end stack-up.

We therefore conclude that the performance of a single 802.11 g dedicated front-end and that of the proposed multiband simultaneous reception structure is practically identical when the adaptive method is used.

V. CONCLUSION

In this article, a novel multistandard simultaneous reception architecture was presented. Expected performance of its

implementation has been presented for a particular study case – simultaneous reception of two signals using the 802.11 g and UMTS standards. Compared to the stack-up dedicated front-ends structure, the architecture assessed here uses an innovating double IQ multiplexing technique in order to use a unique front-end for the simultaneous reception of two arbitrarily chosen frequency bands.

The theoretical study shows that the performance of a receiver using this single front-end architecture along with a MMSE digital method is similar to that of a front-end stack-up receiver. These results are validated by simulation: an accurate Agilent ADS model of the proposed front-end architecture was integrated in a co-simulation platform along with a Matlab developed digital method and with a real radio-channel transmission.

The complexity decrease offered by the use of a single front-end engenders a power consumption gain of 30%. If we also take into account the fact that the performance offered by the proposed structure is similar to those of the front-end stack-up architecture, we can conclude that the proposed architecture offers a much better performance-complexity-power trade-off.

The need of low power front-end capable of receiving a discontinuous spectrum signal has become real interest since the 3GPPP announced that the LTE-Advanced standard will use this type of signals for the downlink transmission [20]. Therefore, one of the issues that still has to be addressed turn around the implementation of this type of front-end in a LTE-Advance receiver. Another interesting idea concerns a possible multi-antenna multi-band simultaneous reception technique using the principles of the architecture assessed in this article.

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REFERENCES

[1] Evans, D.; Raynes, D.; Payne, A.: Development and Simulation of a Multi-standard MIMO Transceiver, FLOWS WP4 program, Deliverable Number: D20, IST-2001-32125, November 2004.

[2] Lee, S.-G.; Kim, N.-S.; Oh, S.-M.; Choi, J.-K.; Kim, S.-C.: A dual-band receiver architecture for PCS and IMT-2000, in IEEE Asia-Pacific Conf. on ASICs, August 2000, 235–238. doi: 10.1109/APASIC.2000.896952.

[3] McFarland, B.; Shor, A.; Tabatabaei, A.: A 2.4 & 5 GHz dual band 802.11 WLAN supporting data rates to 108 MB/s, in IEEE Gallium Arsenide Integrate Circuit Symp., October 2002, 1–14. doi: 10.1109/GAAS.2002.1049018.

[4] Belot, D.; Bonhoure, B.; Saias, D.; Bertholet, N.: A DCS1800/GSM900 RF to digital fully integrated receiver in SiGe 0.35 um BiCMOS, in BIPOLAR/BiCMOS Circuits and Technology Meeting, October 2001, 86–89. doi: 10.1109/BIPOL.2001.957863.

[5] Rampmeier, K.; Agarwal, B.; Mudge, P.; Yates, D.; Robinson, T.: A versatile receiver IC supporting WCDMA, CDMA and AMPS cellular handset applications, in IEEE Radio Frequency Integrated Circuits Symp., May 2001, 21–24. doi: 10.1109/RFIC.2001.935633.

[6] Van Der Burgt, C.: Multi-band Receiver and Method Associated Therewith (Patent style), U.S. Patent 7120406, June 11, 2004.

[7] Burciu, I.; Gautier, M.; Villemaud, G.; Verdier, J.: Method for Processing Two Signals Received by a Single Terminal, WO/2010/031944, March 2010.

[8] Mak, I.; Seng.-Pan, U.; Martins, R.P.: Analog-Baseband Architecture and Circuits for Multistandard and Low Voltage Wireless Transceivers, Springer, 2007 (ISBN: 978-1-4020-6432-6).

[9] Rudell, J.C. et al.: A 1.9 GHz wide-band if double conversion CMOS integrated receiver for cordless telephone applications. IEEE J. Solid-State Circuits, **32** (12) (1997), 2071–2088.

[10] Rudell, J.C.: Frequency translation techniques for high-integration high-selectivity multi-standard wireless communication systems, Ph.D. dissertation, Dept. Electrical Engineering and Computer Sciences, Berkeley Univ., 2000.

[11] Çetin, E.; Kale, İ.; Morling, R.C.S.: Adaptive self-calibrating image rejection receiver, in IEEE Communications Society, vol. 5, June 2004, 2731–2735. doi: 10.1109/ICC.2004.1313027.

[12] Traverso, S.; Ariaudo, M.; Fijalkow, I.; Gautier, J.-L., Lereau, C.: Decision directed channel estimation and high I/Q imbalance compensation in OFDM receivers. IEEE Transactions on Communications, **57** (5) (2009), 1246–1249. doi: 10.1109/TCOMM.2009.05. 070161.

[13] Widrow, B.; McCool, J.; Ball, M.: The complex LMS algorithm. Proc. IEEE, **64** (1975), 719–720.

[14] Gantz, M.W.; Moses, R.L.; Wilson, S.L.: Convergence of the SMI and the diagonally loaded SMI algorithms with weak interference. IEEE Trans. Antennas Propag., **38** (3) (1990), pp. 394–399. doi: 10.1109/8.52247.

[15] Xiao, J.; Mehr, I.; Silva-Martinez, J.: A high dynamic range cmos variable gain amplifier for mobile DTV tuner. IEEE J. Solid-State Circuits, **42** (2) (2007), pp. 298–301. doi: 10.1109/JSSC.2006.889386.

[16] Burciu, I.; Verdier, J.; Villemaud, G.: Low power multistandard simultaneous reception architecture, in European Wireless Technology Conf., September 2009.

[17] www.agilent.com

[18] IEEE Computer Society: 802.11 g Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications, http://standards.ieee.org/getieee802/download/802.11g-2003.pdf, June 2003.

[19] 3rd Generation Partnership Project: UMTS Physical layer procedures (TDD) (Release 8), http://www.3gp.org/ftp/Specs/htmlinfo/25224.htm, March 2008.

[20] Parkvall, S. et al.: LTE-advanced – evolving LTE towards IMT-advanced, in Vehicular Technology Conf., IEEE 68th, September 2008. doi: 10.1109/VETECF.2008.313.

Ioan Burciu was born in Craiova, Romania, in 1982. He received the diploma degree in electrical engineering and the M.Sc. degree in microelectronics engineering from INSA, Lyon, France, both in 2006. From 2006 to 2009 he joined Orange Labs where he worked on agile multi-standard receivers. He received his Ph.D. degree in telecommunications engineering in 2010 from INSA of Lyon. His research interests are radiofrequency design and implantation, system level simulation and measurements, and multiple antennas processing (SIMO, MIMO).

Guillaume Villemaud was born in Limoges, France, in 1973. He received M.S. degree in electrical engineering from the University of Limoges, France, in 1999. From 1999 to 2002 he worked at IRCOM, Limoges, France, on compact integrated antennas and received his Ph.D. degree in electronics in 2002. He developed multi-band hybrid arrays for CREAPE from 2002 to 2003 and then joined the CITI Laboratory, Lyon, France, in 2003. He is currently an associate professor at INSA Lyon, France. His research interests are antenna design and integration, antenna diversity and multiple antenna processing (SIMO, MIMO), and system level simulation and measurements.

Jacques Verdier was born in Toulouse, France, in 1969. He received the M.S. degree in electrical engineering from the University of Toulouse, France, in 1997. From 1998, he is an associate professor at INSA Lyon, France. At the same time he joined the research laboratory today called INL (Institut des Nanotechnologies de Lyon, UMR-CNRS 5270). His area of interest includes the modeling and characterization of noise in nonlinear microwave circuits, but also the analog and RF IC design for wireless communications in BiCMOS and CMOS technologies.

Matthieu Gautier Matthieu Gautier was born in Poissy, France, on June 3, 1978. He has received M.Sc. degree in signal and image processing from the University of Cergy-Pontoise, France, and an electrical engineering degree from the ENSEA both in 2001. In march 2006 he received a Ph.D. degree from the INPG Grenoble, France. From September 2006 to September 2009, he was a post-doctoral researcher at Orange labs and at CITI laboratory. He is currently a research engineer at the CEA-LETI laboratory. His research interest is signal processing for wireless communication: wavelet packet modulation, multi-antenna multi-standard system, radio architecture, RF impairments.