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RESEARCH PAPER

Ultra compact multi-standard low-noise amplifiers in 28 nm CMOS with inductive peaking

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This work presents the design of two compact multi-standard low-noise amplifier (LNA) in a 28 nm low-power bulk CMOS process. The transistor parameters were optimized by the g_m/I_D method taking into account the parasitics and the behavior of highly scaled transistors. To cover the industrial science medical (ISM)-bands around 2.4 and 5.8 GHz, the WLAN band as well as the K_u band a bandwidth enhancement is required. Two versions of LNAs, one with vertical inductors and one with active inductors, are implemented and verified by measurements. The noise figure (NF) exhibits 4.2 dB for the LNA with active inductors and 3.5 dB for the LNA with vertical inductors. The voltage gain reaches 12.8 and 13.4 dB, respectively, with a 3 dB-bandwidth of 20 GHz. Both input referred 1-dB-compression points are higher than −12 dBm making the chips attractive for communication standards with high linearity requirements. The chips consume 53 mW DC power and the LNA with active inductors occupies a core area of only 0.0018 mm², whereas the version with vertical inductors requires 0.021 mm².

Keywords: Low-noise amplifiers, Passive components and circuits, Vertical inductors

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I. INTRODUCTION

Increasing interest toward smart homes and internet of things (IoT) has emerged the recent years. Transceiver providing different services to communicate and control different sensors for home automation becoming more and more attractive. Services such as ZigBee, wireless local area network (WLAN), and Bluetooth are popular and share the frequency bands up to 5.8 GHz. Covering also the K_u band, additional standards such as digital video broadcasting - satellite can be provided. Combining for example WLAN and DVB-S exceeds in a multimedia entertainment for satellite television and videos on demand.

To make such transceiver cost-effective and therefore accessible for the broad population demands for a highly scaled complementary metal-oxide semiconductor (CMOS) technology suitable for mass production. Designing compact analog circuits in such a technology benefits from a future implementation of a complete transceiver on a system on chip (SoC). A SoC combines the advantages of fully integrated high-performance digital signal processing with compact analog circuits. Additionally to the radio frequency (RF)-building blocks, a SoC provides the opportunity to efficiently integrate the baseband and built-in-self-calibration circuitry on the chip [1, 2].

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Despite these advantages highly scaled field effect transistor (FET) in bulk CMOS technology are known for their low intrinsic gain, their low breakdown voltage, their leakage currents, and their high flicker noise. The available technology is optimized for digital low-power design and does not support analog design components in term of RF transistor devices and models, metal insulator metal (MIM) capacitors and inductors [1, 2]. To optimize the low-noise amplifier (LNA) for high voltage gain is challenging and can be only obtained at the expense of DC power consumption and high NF. To compensate the increase in NF, the width of the transistor can be adapted and which in turn affects the bandwidth. Another possibility to increase the voltage gain is the approach of a multi-stage topology consisting of several common source or cascode stages [1, 3].

Many different approaches of broadband LNA in scaled CMOS can be found, most commonly they consist of common gate stages, sometimes with noise canceling [4] or common source and cascode topologies with feedback. The feedback can be implemented as inductive source degeneration [5] or with resistive negative feedback [6, 7]. Other promising architectures are distributed LNAs [8, 9]. However, one disadvantage of these architectures are, that the bandwidth defines the chip area and the power consumption and makes this not suitable for ultra compact and wideband LNAs.

The work in [10] combines the idea of feedback and multi-stage topology with differential amplifiers. The differential design rejects power supply and substrate noise and minimize second-order distortion, which is a key parameter for direct conversion receivers [4]. However, differential designs need

an additional balun to be connected to the antenna, which itself reduces the gain. The LNA in [10] is designed in a 180 nm BiCMOS technology and shows promising results. In this work, a similar topology is optimized and implemented in the 28 nm CMOS process.

In the following sections, two ultra compact LNAs with different peaking elements are designed and both versions are compared by measurement results. In Section II, the circuit is introduced and the FETs are dimensioned using the g_m/I_D-based method suitable for highly scaled low-power bulk CMOS technologies. The RF transistors are sized for a tradeoff between noise, gain, and bandwidth. To guarantee the application of the LNA in multi-band operation inductive peaking of the loads is required. The Section II-C investigates three possibilities for the realization of these components and their advantages and disadvantages. Finally, the implementation of the two versions is described and measured in Section III.

II. DESIGN CONSIDERATIONS

A) Overview

The design goals for the LNA are a high bandwidth to cover multiple frequency bands up to the K_u of maximum 18 GHz, a moderate voltage gain and NF, and a compact layout. The basic schematic representation of the proposed LNA with feedback is shown in Fig. 1. Since the variety of components of the schematic only includes resistors and transistors, the size of the layout is expected to be low and mainly linked by the impedances $z_{L1}(\tau)$. The circuit consists of two cascaded differential amplifiers and two feedback loops. One feedback loop describes an overall feedback, which influences input and output impedances, as well as the gain. The other feedback loop only includes the second differential amplifier stage and can be used for fine tuning. Negative feedback improves bandwidth, lowers temperature variations, and ripples on the gain curve. These advantages come at the cost of voltage gain.

This circuit is designed with a broadband input power matching to the differential system impedance of 100 Ω. According to this requirement and with the simplified model in Fig. 2 the feedback resistors R_{fb1} will be dimensioned.

The sum of all currents at the input node is zero and yields

$$I_{in} - \frac{V_{in}(1+\alpha_v)}{R_{fb1}+R_{L2}} = 0. \quad (1)$$

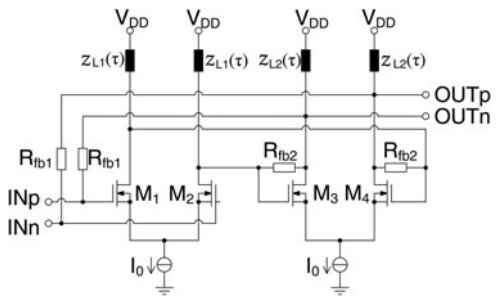

Fig. 1. Schematic representation of the LNA.

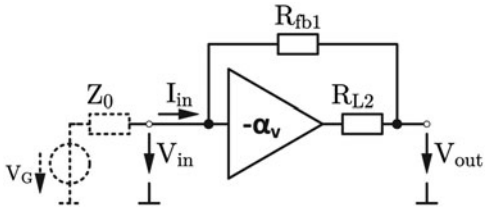

Fig. 2. Simplified model of the LNA [10].

The input impedance should be equal to the system impedance Z_o and together with (1), R_{fb1} can be calculated to

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{R_{fb1}+R_{L2}}{1+\alpha_v} \overset{!}{=} Z_o \quad \text{and} \quad (2)$$

$$R_{fb1} = Z_o(1+\alpha_v) - R_{L2} \quad (3)$$

Both differential pairs reveal an open-loop gain of $\alpha_v = 5.7 \hat{=} 15.1$ dB. The open loop-gain depends on the tail current I_o and the loads R_{L2}. The value for the tail current will be discussed in the next section and R_{L2} is set to 70 Ω for a compromise between gain, moderate losses and a low output resistance for the implementation as buffer. With these values and (3), R_{fb1} can be calculated to 265 Ω. Due to finetuning of the circuit, the feedback resistor is implemented with 260 Ω.

The following paragraphs investigate the dimensioning of the active devices and detailed considerations of possible load implementations of the differential amplifiers.

B) Active device sizing

One of the first steps to dimension FET is the decision for a DC operation region and thereby an inversion level. The IV-diagram of long channel transistors has defined regions with sharp transition between weak, moderate, and strong inversion. However in this highly scaled technology, categorizing the IV-behavior according to the inversion level is a challenge. The transitions between the different regions are smooth and without a break. The expected behavior of the transistor like a voltage controlled current source in strong inversion does not occur. In every region the transistor react more or less like a voltage controlled resistor. Also the well-known current equations of the transistor are only an approach.

To overcome these issues, a suitable method to characterize the transistor behavior and to find a suitable operation region is described in [11, 12]. This method also fits to short channel devices and is called the g_m/I_D method. According to this approach, the FET $M1 - M4$ of Fig. 1 are dimensioned.

In these works, the characterization of the transistor is based on the transconductance efficiency as a central parameter. The transconductance efficiency is defined as g_m/I_D and describes which value of g_m can be reached by minimum current.

Important plots for the characterization of the transistors according to the g_m/I_D method are Figs 3–6. The plots of Figs 3 and 4 show the intrinsic gain and the transit frequency versus the transconductance efficiency. These plots are necessary to determine the suitable transconductance efficiency. To

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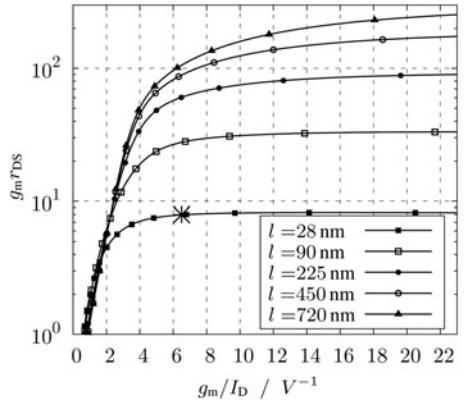

Fig. 3. Intrinsic gain g_m/r_{DS} versus transconductance efficiency g_m/I_D.

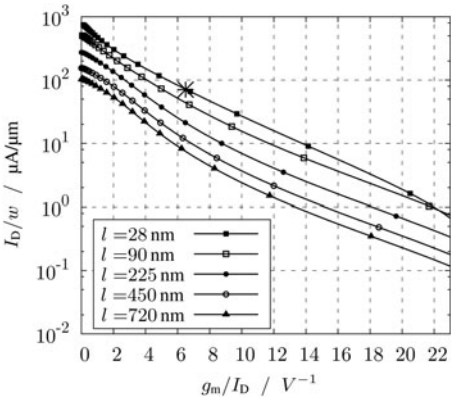

Fig. 6. Current per width I_D/w versus transconductance efficiency g_m/I_D.

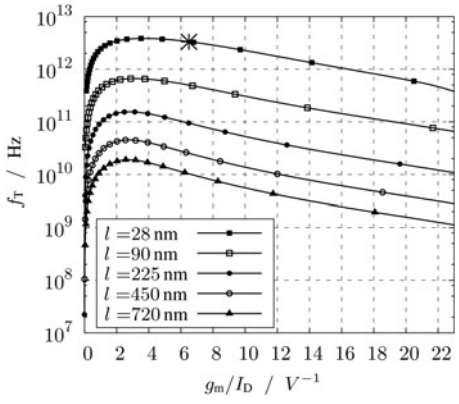

Fig. 4. Transit frequency f_T versus transconductance efficiency g_m/I_D.

set the correct transconductance efficiency in the circuit, the required V_{GS} can be read in Fig. 7. By a known transconductance efficiency and current, the width of the transistor can be read off the plot Fig. 6. The saturation voltage $V_{DS,sat}$ of Fig. 5 shows by a given g_m/I_D the minimum V_{DS}.

The value of the transconductance efficiency depends on the optimization goals of the circuit. For low-power circuits with large voltage swing, the transconductance efficiency has to be high. A high g_m/I_D means a high g_m by minimum current. For high g_m/I_D the intrinsic gain according to Fig. 3 is high, too. The intrinsic gain $g_m r_{DS}$ influences the voltage gain and due to the low r_{DS} of highly scaled transistors this is an important parameter. Dimensioning a circuit with high g_m/I_D defines an inversion level of the transistor to the weak inversion. The drawback of this operation region is a low transit frequency f_T and thereby a low bandwidth. Typical curves of f_T are shown in Fig. 4.

To optimize the circuit for a high f_T, the transistor must be in strong inversion. In strong inversion, not only the intrinsic gain decreases, but also the power consumption increases.

Operating in moderate inversion is optimal when the transit frequency, the intrinsic gain and the power consumption are valued equally. This inversion mode match to the requirements of this LNA, which requires a high f_T to ensure a high bandwidth and a moderate voltage gain and power consumption.

The inversion level can be set by V_{GS}. For low V_{GS} and thereby working in low inversion the g_m/I_D is high and f_T is low. A high V_{GS} means operating in high inversion and a low g_m/I_D as well as high f_T.

To find the optimal value of V_{GS} in moderate inversion, the product of the transit frequency and the transconductance efficiency is defined and plotted in Fig. 7. Interestingly the product of both peaks at V_{GS} of 650 mV. This value determines the $g_m/I_D = 6.5V^{-1}$ of the circuit. The circuit of the LNA is designed for this V_{GS}. Besides this setting V_{GS}, includes no information. In the following paragraphs, the behavior of the transistors is described by just g_m/I_D. In each plot, the implemented g_m/I_D of the LNA is marked by a star.

The big advantage of the description by g_m/I_D is the width independence due to the normalization of the parameters. Only the length is set as parameter in the following plots

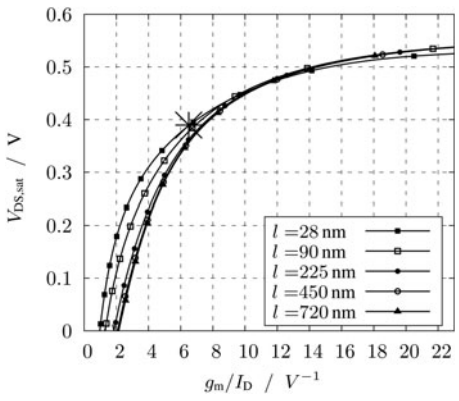

Fig. 5. Saturation voltage $V_{D,\,sat}$ versus transconductance efficiency g_m/I_D.

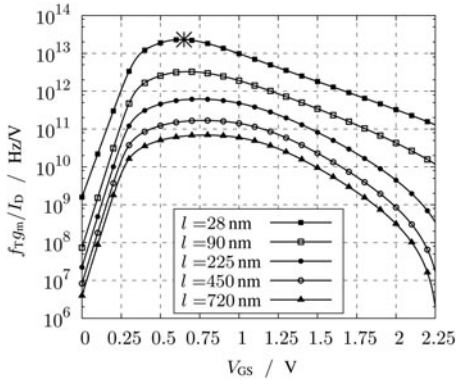

Fig. 7. Product of transconductance efficiency and transit frequency.

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(Figs 3, 4 and 5). The choice of length and thereby if a short channel device is implemented means to get a high f_T, whereby a long-channel device defines a high intrinsic gain. For this design the minimal length of 28 nm is chosen to benefit from the high bandwidth of the technology.

In Fig. 3 the intrinsic gain is shown. At a g_m/I_D of 6.5 V^{-1} the intrinsic gain of short channel devices has almost reached its maximum. The high dependence of the intrinsic gain to the length can be recognized in the plot. For higher channel lengths r_{DS} increases and for the lengths of the plotted parameter set the intrinsic gain is multiplied by the factor of more than 10.

However, this positive behavior differs from the curves of Fig. 4, where the transit frequency versus g_m/I_D is depicted. At the g_m/I_D of 6.5 V^{-1}, the maximum value of f_T has slightly fallen, but is still very high. Here the reached value gains from the low transistor length.

The $V_{DS,sat}$ plot of Fig. 5 states how the minimum voltage across the transistor must be to operate in saturation. The values should be considered carefully, because like mentioned before the IV-diagram of short channel devices is not sharply defined. It is more like a a gradual increase. For this circuit the V_{DS} is set to 500 mV. This value includes enough margin to $V_{DS,sat} = 380$ mV. With a V_{DD} of 2.2 V the current source I_o and the loads should also obtain enough voltage headroom.

To finalize the dimension the width can be determined by a given current and the current per width. The plot of the current per width versus g_m/I_D is shown in Fig. 6. With a g_m/I_D of 6.5 V^{-1}, at minimum length and according to Fig. 6, the current per width of the transistor can be read to 80 μA/μm. To determine the optimum current, simulations of the LNA with ideal pure resistive loads of 70 Ω are carried out. In Fig. 8 the minimum noise figure for different tail currents and with constant current per width of 80 μA/μm is shown for different frequencies. For low currents the minimum noise figure achieves maximum values. By spending around 6 mA the minimum noise figure is below 3 dB. To reduce the noise figure by further 1 to 2 dB, the current has to be doubled. For a tradeoff between current consumption and low noise, the current I_D is set to 6 mA. With this current and a current per width of 80 μA/μm, the width can be calculated to 75 μm.

C) Bandwidth enhancement

This section describes bandwidth extensions such as peaking, which are necessary to meet the requirements of a bandwidth higher than 20 GHz. Generally for peaking, the loads are replaced by an inductor in series with a resistor.

Over frequency the voltage gain without bandwidth enhancement degrades. To avoid too much losses, an

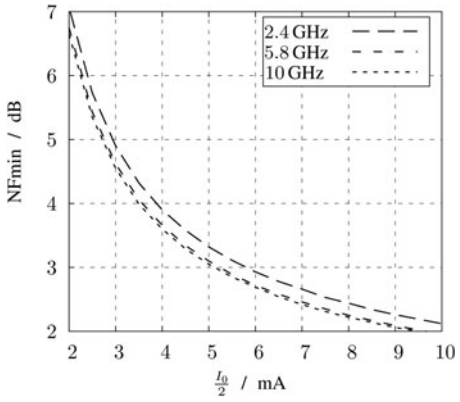

Fig. 8. Minimum noise figure versus current at constant I_D/w.

increased magnitude of the load impedance counteracts this decline. At a frequency of 15 GHz the voltage gain is reduced by 20%. A series connection of the load resistor of 70 Ω and an inductance of 0.5 nH reveal an increased magnitude of the impedance of 20% compared with a pure resitive load and compensates the losses.

$$0.8\left|(R_{1|2} + j\omega L)\right| = R_{1|2} \quad \text{for} \quad f = 15\,\text{GHz} \tag{4}$$

In this design, the peaking inductor is optimized for a high inductance value per area to obtain the advantage of a small chip area. The quality factor and thereby the equivalent resistance can be neglected for the simple reason that there the already existing series resistor can be lowered by the parasitic resistance of the inductor. However, the inductor has to be designed to carry 6 mA, which is about half of the tail current.

One other important issue for the implementation of the inductors are the local density requirements of the technology. Due to the fact, that the technology is optimized for digital design there are no exceptions for the local density of inductors. The layers with low local metal density have to be filled to fulfill the density rules. But filling degrades the RF performance of the inductor and the results are not suitable anymore for the design.

Here three possibilities to implement the peaking element are described: a planar inductor, an active inductor, and a vertical inductor.

1) PLANAR INDUCTOR

Generally planar inductors are associated to be bulky and consume a lot of area. Unfortunately their size does not scale in technology. Indeed the quality factor of these

Table 1. Comparison of inductive components.

Inductor type, ref	Basic planar [13]	Enh. planar [14]	Active	Vertical
Symmetrical	No	Yes	No	Yes
L/nH @ 2.4 GHz	0.49	1.0	–	1.0
$\Im(Z_{in}/\omega)$@2.4 GHz	–	–	1.2	–
size/μm²	112 × 102	35 × 35	12 × 12	75 × 140
ind./area/nH/mm²	42	816	4167	95
Q_{max} @ f/GHz	11.8	5.4 @ 27.5	–	1.7 @ 27
SRF/GHz	≈ 21	50	–	45
Metal density	Low	Low	Moderate	High

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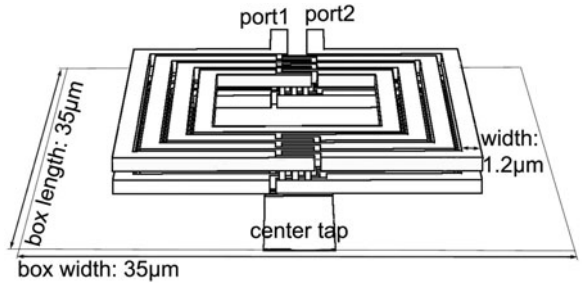

Fig. 9. Setup of a enhanced symmetrical planar inductor.

inductors is pretty high, but the inductance per area is very low. In Table 1, the parameters of an ordinary planar inductor, fabricated in a 65 nm technology, are shown as specified in [13]. The inductance per area of only 42 nH/mm² makes this inductor not suitable for a size-optimized design.

One idea to reduce the size of planar inductors fed by differential signals is to design symmetrical inductors. The setup of such a symmetrical inductor is depicted in Fig. 9, the differential signal inputs are port 1 and port 2 and by the center tap the DC voltage is connected. If a circuit like this LNA is designed for differential signals, the area of one symmetrical inductor is lower compared with the design of two single inductors.

Another possibility to reduce the size is to run the lateral windings through two metal layers. Often the metal stack provides several top metals with high current density and hence they are a good choice for inductors. Figure 9 shows the setup of such an enhanced symmetrical inductor. It can be seen that the turn starts at the differential input on the upper metal and at the center tap, there is a contact to the lower metal to finish the turn on this metal.

In [14] all optimization techniques are combined and an enhanced planar symmetrical inductor is realized in a similar metal stack. For the comparison, this proposed inductor is modified in terms of inductance and quality factor to fit to the design requirements and to simplify the comparison. Figures 10 and 11 show the inductance and quality factor (Q) simulated in the 2.5 D EM-simulation software *Sonnet*. The values of this inductor version are also listed in Table 1. The inductance per area with 816 nH/mm² achieves a very high value due to the fact, that only the upper metals with a high current density are carrying the current. As a result the width of windings must be only 1.2 µm. The quality factor of maximum 5.4 at 27.5 GHz is moderate, but for peaking issues applicable. The self resonance frequency (SRF) achieves the highest value of 50 GHz of the comparison table. In this configuration, the inductor is not bulky and is a good choice for the design.

However, the layout of both planar inductors only uses the upper metal layers and therefore the local density of the lower metals cannot be met without filling. The RF performance degrades and the design is therewith not suitable for this design.

2) ACTIVE INDUCTOR

Another implementation of an element with inductive behavior is an active inductor. One possible topology is a pmos transistor as load with a resistor and a capacitor connected at the gate. In Fig. 12 the schematic representation of the

Table 2. State-of-the-art.

Ref.	Tech	BW(GHz)	A_v (dB)	$\lvert S_{21}\rvert$(dB)	$\lvert S_{11}\rvert$(dB)	NF(dB)	$P_{in,1dB}$(dBm)	IIP_{IM3}(dBm)	area(µm²)	P_{DC}(mW)	Comment
[4]‡	65 nm CMOS	0.2...5.2	13...15.6	6.6	<−10	<3.5	–	>0	110 × 80†	21	Balun-LNA
[6]‡	45 nm CMOS	10	18	–	<−7	<3	−14.5	−6.6	–	32	
[2]‡	45 nm CMOS	2.3...9.8	9.3	–	<−18	<6	–	–	680 × 570	1.5	planar FETs
		2.3...9.8	12.5	–	<−15	<6.5	–	–	700 × 236	5.3	FinFETs
[7]	65 nm CMOS	2.6...6.6	–	13.6	<−13	<6.5	17.6	–	1080 × 940	6.8	with ESD cells
[17]‡	65 nm CMOS	4.5, 8	15–18	>15	<−15	4	−1	16	–	10.8	Balun-LNA, WLAN Blockers
[18]‡	65 nm CMOS	0.05...5	–	0–24	<−10	<3.5	−25	−8	150 × 250†	12	tunable gain
[1]	28 nm CMOS	18	–	>10.8	<−11	4	−12.5	–	750 × 500	24	@ 60 GHz
[8]	90 nm CMOS	0–21	–	15.4	<−8	4.4	–	−6.6	900 × 460	12	distributed LNA, low power
[9]	180 nm CMOS	0–20	–	8	<−13	3.5	–	–	1050 × 370	34.2	distributed LNA
This	28 nm CMOS	20	12.8	10.6	−14	5.2	−12	−13	40 × 45†	53	act. inductor
		21	13.4	12.2	−15	4.3	−10	−8	300 × 70†	53	vert. inductor

*Measured on PCB.
†Core area.
‡Simulation results.

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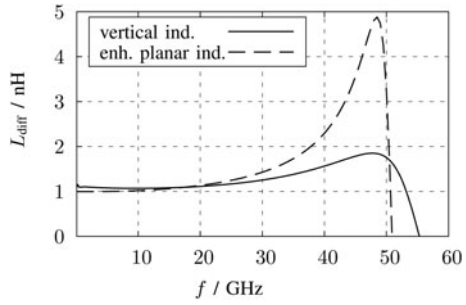


Fig. 10. Inductance of the symmetrical enhanced planar and the symmetrical vertical inductor versus frequency.

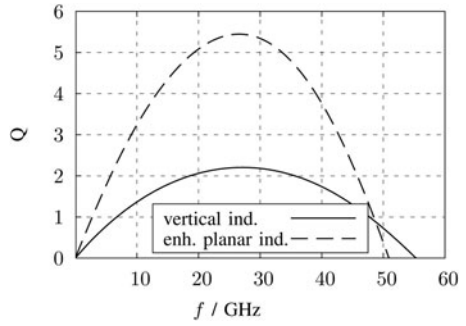


Fig. 11. Quality factor of the symmetrical enhanced planar and the symmetrical vertical inductor versus frequency.

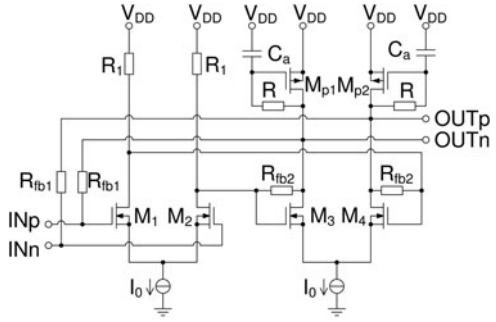
LNA with active inductors as replacement of $z_{L_1}(7)$ is shown. Unfortunately this inductive component adds noise to the LNA like other active devices.

The input impedance $\underline{Z}_{in}$ of the active inductor is a key parameter and can be calculated with the small signal model shown in Fig. 13. The model includes the capacitances C_{GS}, C_{GB}, C_{DS}, C_{DB} as well as r_{DS}.

Following definitions simplify the model:

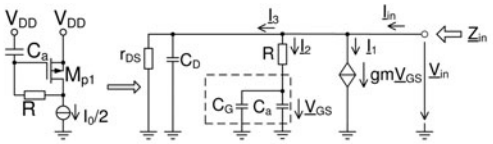
$$C = C_a + C_{GS} + C_{GB}, \qquad C_D = C_{DS} + C_{DB},$$

According to the model, the currents $\underline{I}_1$, $\underline{I}_2$, and $\underline{I}_3$ are defined



$R_1 = 125\,\Omega$ $R_{fb1} = 260\,\Omega$ $R_{fb2} = 5\,k\Omega$
$R = 300\,\Omega$ $C_a = 75\,fF$ $I_0 = 12\,mA$
$V_{DD} = 2.2\,V$ $l_{p1/2} = 28\,nm$ $w_{p1/2} = 90\,\mu m$
$l_{M1\text{-}4} = 28\,nm$ $w_{M1\text{-}4} = 75\,\mu m$

Fig. 12. Schematic representation of the LNA with active inductors.



$C = C_a + C_G$ $C_a = 105\,fF$ $C_G = C_{GS} + C_{GB} = 43.2\,fF$
$r_{DS} = 148\,\Omega$ $R = 300\,\Omega$ $C_D = C_{DS} + C_{DB} = 23.7\,fF$
$g_m = 38.8\,mS$ $I_0 = 6\,mA$

Fig. 13. Small signal model of the active inductor.

as

$$\underline{I}_1 = g_m \underline{V}_{GS} = g_m \frac{\underline{V}_{in}}{1 + j\omega RC}, \tag{5}$$

$$\underline{I}_2 = \frac{\underline{V}_{in}}{R + (1/\, j\omega C)}, \tag{6}$$

$$\underline{I}_3 = \frac{\underline{V}_{in}}{r_{DS}}\left(1 + j\omega r_{DS} C_D\right). \tag{7}$$

The input current $\underline{I}_{in}$ can be derived from Kirchhoff's law at the input node. Together with equations (5)–(7) yielding

$$\begin{aligned}\underline{I}_{in} &= \underline{I}_1 + \underline{I}_2 + \underline{I}_3 \\ &= \underline{V}_{in}\left(\frac{g_m + j\omega C}{1 + j\omega RC} + \frac{1 + j\omega r_{DS} C_D}{r_{DS}}\right).\end{aligned}$$

The input impedance is then calculated as

$$\begin{aligned}\underline{Z}_{in} &= \frac{\underline{V}_{in}}{\underline{I}_{in}} \\ &= \frac{r_{DS}\left(1 + j\omega RC\right)}{r_{DS}\left(g_m - \omega^2 RCC_D\right) + 1 + j\omega(RC + r_{DS}(C + C_D))}.\end{aligned}$$

With the parameters listed in Fig. 13, the magnitude of $\underline{Z}_{in}$ is also plotted together with the simulation results in Fig. 14. At lower frequencies both curves show the inductive behavior by increasing the magnitude of the impedance over frequency. This behavior is required to counteract the decline of the voltage gain of the LNA. To understand the active inductor, in Fig. 15 the impedance is splitted in real and imaginary

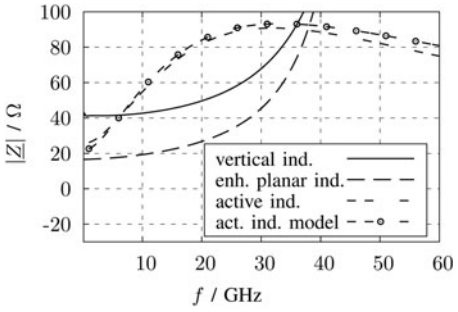


Fig. 14. Magnitude of the impedance of the inductors versus frequency.

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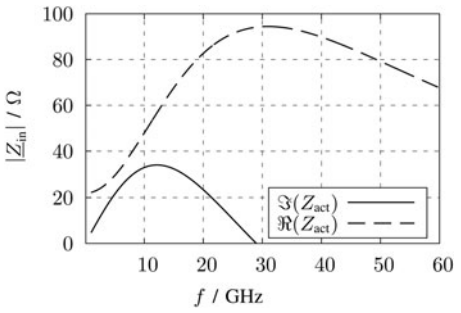

Fig. 15. Real and imaginary parts of the impedance of the active inductor.

parts. The imaginary part shows no broadband behavior and reaches zero before 30 GHz. Nevertheless, the magnitude of the impedance achieves its maximum at about 30 GHz. This effect comes from the frequency depending real part of the impedance, which is also shown in Fig. 15. The DC resistance is only 22 Ω, which reduces the DC losses.

The capacitances and resistors of the transistor model are defined by the transistor width and length. The width is high enough to carry the tail current and the length is set to the minimum length to obtain a high bandwidth. Remaining parameters are C_a and R, which are plotted with different values in Figs 16(a) and 16(b). By increasing C_a or R, the slope of $|\underline{Z}_{in}|$ also getting higher. C_a defines the decline toward higher frequencies and R affects the maximum of $|\underline{Z}_{in}|$. For this design, $C = 105$ fF and $R = 300$ Ω are selected as a compromise for a minimum decline toward higher frequencies and for a maximum $|\underline{Z}_{in}|$ at about 20 GHz to counteract the decline of voltage gain of the active inductor.

An advantage of this inductive element is, that the lower metal layers are covered by transistors and resistors. With a considered layout and the connection of the capacitor the metal density rules of the upper metals fullfilled.

3) VERTICAL INDUCTOR

Another idea to design inductors with low size are vertical inductors. The implementation of these inductors is described

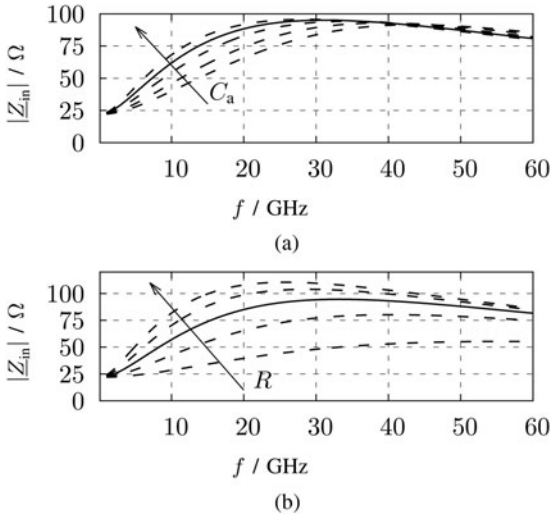

Fig. 16. Magnitude of the impedance of the small signal model active inductor. (a) $R = 300$ Ω; $C_a = [40$ fF, 150 fF]. (b) $C_a = 105$ fF; $R = [100$ Ω, 500 Ω]

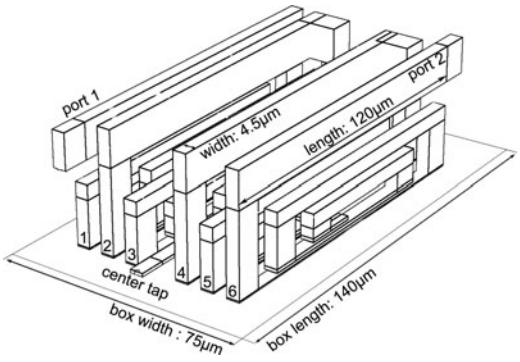

Fig. 17. Setup of the vertical inductor.

in [15, 16]. The turns are not planar to the substrate plane but run across the metal stack. The windings begin at the upper metal, run through the via stack to the lower metals and finally ends in the middle of the metal stack. The setup of the vertical inductor is shown in Fig. 17. The windings run through six conductor planes. To reduce the area, the inductor is designed as symmetrical inductor. The central tapping is on the lowest metal, whereas the contacts are on the top metal.

This geometry implicates a high dependency on the metal stack, so there is no degree of freedom for the designer. The distances of the conductor planes are fixed and change over the metal stack. Due to the fixed distances, the inductance can only be increased by connecting several inductors in series or by increasing the numbers of windings, which in turn are limited to the metal stack. In addition, the small distances of the lower metals decrease the SRF. For this LNA six smaller vertical inductors are connected in series to achieve the necessary differential inductance value of 1 nH. By changing the geometry the inductance cannot be achieved.

The width of the inductor is defined by the maximum current of the metals. Contrary to planar inductors, the vertical inductor also uses the low layers of the metal stack, which are often made of thin copper. This results in a higher width of 4.5 µm. Additionally, the contact area has to be large enough for the current and is defined by the low value of the current per via of the lower metals. This also increases the area compared with enhanced planar inductors. The advantage of the layout is that the local density rules can be easily fulfilled.

In Table 1, the key parameters of the vertical inductor are listed. The SRF of 45 GHz is sufficient and can be easily improved by spending more area and more distance to the guard ring of the inductor. Due to the use of lower metals and creating the inductor by six single inductors the area is moderate and hence the inductance per area reaches 95 nH/mm².

The quality factor versus frequency is depicted in Fig. 11 and its maximum value of 2.2 at 27 GHz is low, but not a problem for this application.

4) COMPARISON OF INDUCTIVE COMPONENTS

Table 1 reports the comparison of the inductors. Two of them are symmetrical solutions: the enhanced planar inductor and the vertical inductor. For an equitable comparison the required area, the size of the single inductors has to be doubled for the implementation in a differential design. The area includes the whole area of the inductor including the guard ring, which influences the EM-field.

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The most informative value is the inductance per area. Here strong distinctions can be demonstrated. The active inductor has a high equivalent inductance in a very compact size which results in inductance per area of 4167 nH/mm². All passive versions achieve a much lower value, but there are marked differences, too. Compared with the vertical inductor, the enhanced planar inductor benefits from the high-current density of the upper metal layers and reaches a higher inductance per area.

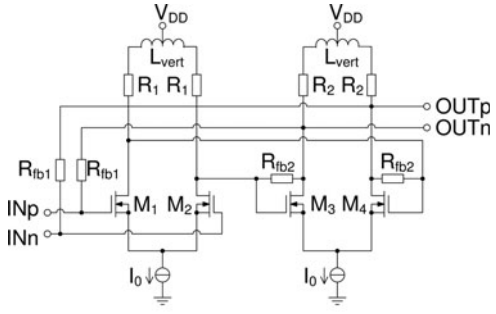
A critical issue of the technology is the metal density. The local density of the lower metals of [13, 14] cannot be met without filling. By contrast, the active inductor solve this problem by a sophisticated layout and the vertical inductors by using all layers of the metal stack.

According to the analysis of this section two different versions of the LNA were implemented: one version with with active inductor and the other with vertical inductor. The first LNA shown in Fig. 12 is designed with an active inductor, which increases the NF, but has the smallest size. To keep the NF within limits only the load impedances of the second differential pair is replaced. This version benefits from the very small active inductor of 12×12 μm². The second version implements a resistor and a vertical inductor in series as loads of both differential amplifiers. It is a remarkable example for the passive, but still small-sized solutions. The schematic representation of this version is depicted in Fig. 18.

III. MEASUREMENT RESULTS

The LNAs were implemented in a low-power 28 nm bulk CMOS technology. Each circuit consumes $P_{DC} = 53$ mW from a supply voltage of 2.2 V. The photographs of the fabricated dies are shown in Figs 19 and 20. In both pictures, the core areas are marked. The core area of the die with active inductors is 40 × 45 μm² and 310 × 75 μm² for the LNA with vertical inductors. The active inductors inside this area are so small that they cannot be recognized. On the contrary in Fig. 20, the vertical inductors can be easily identified due to their characteristic striped shape. On the top and on the bottom of each FET core, there is an array of six single vertical inductors.

The circuits were verified by measurements. For small signal measurements and the large signal 1 dB compression point the LNA were characterized on chip with the *R&S ZVA-67*. The other measurements were completed on



$R_{1/2} = 56\,\Omega$ $R_{fb1} = 260\,\Omega$ $R_{fb2} = 5\,k\Omega$
$L_{vert,diff} = 1.0\,nH$ $I_0 = 12\,mA$ $V_{DD} = 2.2\,V$
$l_{M1\text{-}4} = 28\,nm$ $w_{M1\text{-}4} = 75\,\mu m$

Fig. 18. Schematic representation of the LNA with vertical inductors.

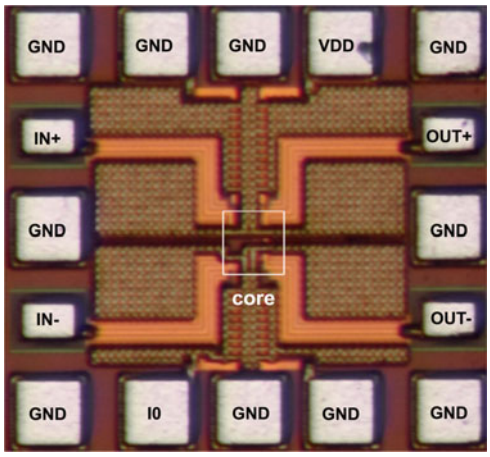


Fig. 19. Photograph of the die of the LNA with active inductors.

printed circuit board (PCB) with the bonded chips. Both dies are part of a larger die, which could not be cut and therefore the bond wires of the outputs are very long. Due to this fact the RF behavior deteriorates. For the differential noise measurement, it was necessary to add low temperature cofired ceramic (LTCC) baluns to be connected to the single-ended measurement equipment. For the results the baluns were deembedded. With this test setup the noise figure were measured with the *R&S FSW-67* with the noise source *NC346V* of *NOISECOM*. The large signal two-tone measurements for determining IM3 are performed by the *R&S SMBV* and *FSV-7*.

In Figs 21 and 22, the measured and simulated *S*-parameters are depicted. The input reflection coefficient and the forward transmission were verified for both LNA by measurements.

The magnitude of $\underline{S}_{21}$ in Fig. 21 is constant over frequency for both LNA versions. Besides the degradation of the measurement results at low frequencies, there is a good agreement between measurements and simulations of both LNAs. This decline can be explained by a series DC block required for the measurement. The simulations are performed by an ideal switch, which also blocks the DC but do not show any high-pass characteristic.

$\underline{S}_{21}$ of the LNA with active inductors with 10.6 dB is lower compared with the other chip with 12.2 dB. The

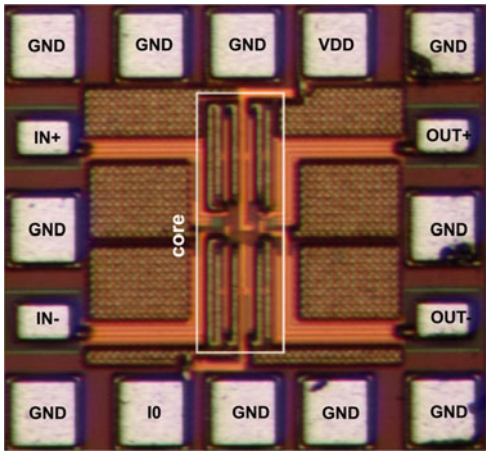


Fig. 20. Photograph of the die of the LNA with vertical inductors.

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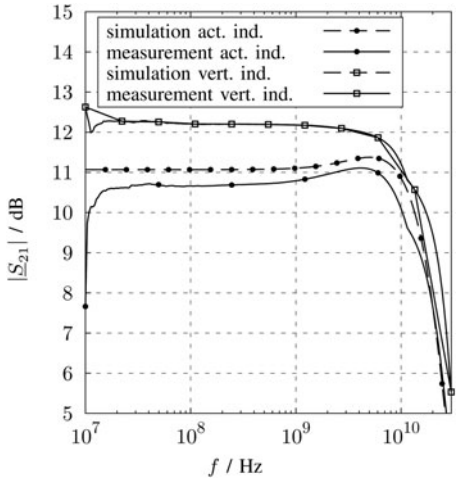

Fig. 21. Measurement and simulation results of the forward transmission.

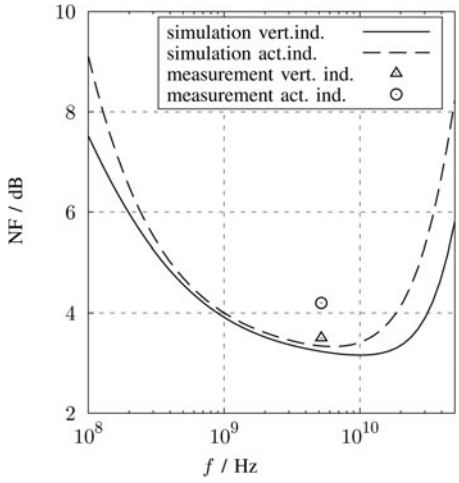

Fig. 23. Noise figure versus frequency.

3 dB-bandwidth of both circuits is similar and with about 20 GHz it covers frequency bands up to the 5.8 GHz ISM bands. For system setup, it can be mentioned that the voltage gain is about 2 dB higher than the power gain. The chip with vertical inductors was designed with a voltage output with a low output resistance of 40 Ω and the one with active inductors with 26 Ω, respectively. A low ohmic output is beneficial for the bandwidth if the subsequent stage have a capacitive input like a IQ switching mixer.

Over the frequency range of 10 GHz, the $|\underline{S}_{11}|$ is lower than −12 dB for both LNA versions. This broadband behavior could only be achieved by resistive power matching.

The noise figure could only be measured with the help of narrow band baluns with the result that only values at single frequencies can be specified. The lowest NF could be measured at the frequency of 5.2 GHz with 4.2 dB for the LNA version with active inductors and with 3.5 dB for the LNA with vertical inductors. Over the whole frequency range the LNA with vertical inductors shows lower NF values than the LNA with active inductors. In Fig. 23, the noise figure of the postlayout simulation is shown. Compared with the simulation values the measurement results are approximately 1 dB higher than the measurement results.

Characteristic parameter for the large signal measurement is the 1 dB-compression point. In Fig. 24, the compression point over frequency of the postlayout simulation for both LNA are shown. In the measurement, the compression point occur at least at −12 and −10 dBm input power for the LNA with active inductors and for the LNA with vertical inductors, respectively.

An intermodulation distortion measurement was carried out using the RF input frequencies of $f_{RF} = f_{RFn} \pm 500$ kHz for one measurement with $f_{RF_1} = 2.4$ GHz and the other with $f_{RF_2} = 5.8$ GHz. In the 1 dB-compression point the LNA with vertical inductors achieves maximum IM3 = −14 dBc with corresponding intermodulation intercept point of $IIP_{IM_3} = -13$ dBm and the LNA with vertical inductors IM3 = −19 dBc and $IIP_{IM_3} = -8$ dBm, respectively.

Both circuits are unconditional stable in differential and common mode.

Table 2 shows state-of-the-art broadband LNA in highly scaled CMOS technologies. Besides the work of [1] all listed LNA are designed in the same low frequency range up to 20 GHz like this work. The authors of [1] are the only one presenting a LNA in a comparable technology. However, the working frequency is much higher and the design is narrow

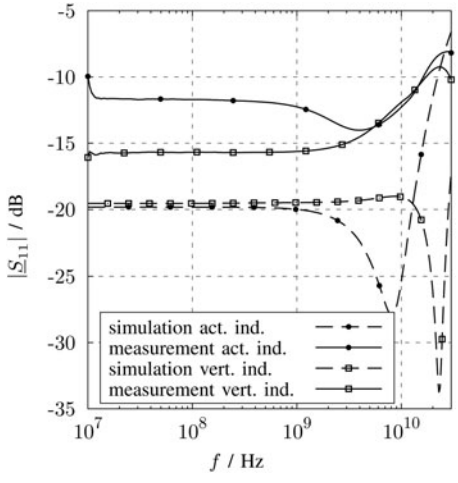

Fig. 22. Measurement and simulation results of the input reflection coefficient.

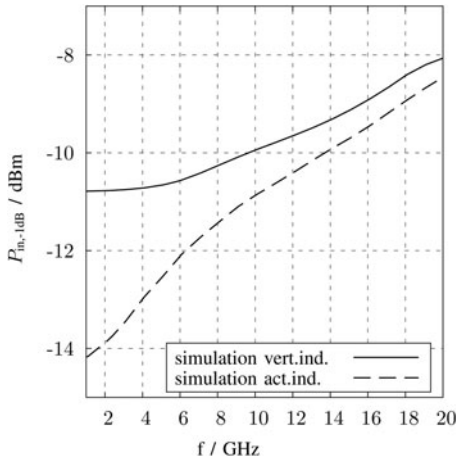

Fig. 24. Compression point versus frequency.

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band. All other LNA are designed in a CMOS technology with higher minimum transistor length.

The works of [1, 4, 7, 18] show measurement results and thereby suitable for comparison.

The proposed LNA in Table 2 are among those with the highest bandwidth and smallest chip area. In [8, 9] two wideband distributed LNAs are introduced. Especially [9] show a very good overall performance and even has a low -power enhancement. Nevertheless, it suffers from its high chip size. The core area for the chip with active inductors is the smallest, the size of the LNA with vertical inductors is comparable with [4]. The 1 dB-compression point of theses proposed LNAs is among the best in Table 2 making this design suitable for communication frontends with like quadrature amplitude modulation (QAM)-64. Small signal gain and noise figure compare well with the other works. In comparison, the power consumption is rather high, which is mainly due to the optimization requirements of moderate noise figure and gain. Additionally, a challenge for the design is the low intrinsic gain of this CMOS bulk technology, which can be more or less compensated by increasing the current. In general, it can be stated, that a broadband LNA in a very compact size, which is applicable for the use for different communication services, was designed. At the best of the authors knowledge these are the first compact LNAs in 28 nm CMOS for this frequency range and the smallest of the state-of-the-art.

IV. CONCLUSION

In this work, two different versions of LNA implemented in a 28 nm bulk CMOS technology are presented. Both versions include inductive peaking components, one with vertical inductors and the other with active inductors. Investigations toward transistor design are done by the g_m/I_D-method to challenge the parameter of highly scaled transistors. There is a good agreement between measurement and simulations. A NF of 4.2 dB for the LNA with active inductors and 3.5,dB for the LNA with vertical inductors at 5.2 GHz were measured. The voltage gain amounts to 12.8 and 13.4 dB, respectively, at a high 3 dB-bandwidth of 20 GHz.

Compared with the state-of-the-art of compact LNA up to 20 GHz these LNA are the ones with the smallest active area at a high bandwidth with moderate voltage gain and NF.

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