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INDUSTRIAL AND ENGINEERING PAPER

Design and development of Ka-band carrier generator for IRS applications

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A Ka-band carrier generator using phase-locked loop (PLL) frequency synthesizer is presented in this paper. The design uses integer-N PLL chip PE83336 as the important hardware support. The key idea of generating Ka-band frequency signal with low-phase noise is to generate a high-quality X-band frequency signal using PLL frequency synthesizer and employ a frequency multiplier to deliver the high-frequency output at the desired frequency band. Experimental measurements of the frequency synthesizer demonstrate the excellent performance, which is achieved with the Ka-band output with a frequency resolution of 5.7 MHz and phase noise better than −70 dBc/Hz at 1 kHz.

Keywords: Phase-locked loop (PLL), Frequency multiplier, Phase detector (PD), Loop filter, Voltage-controlled oscillator (VCO), Divide by 8 prescaler

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I. INTRODUCTION

In the past few years, we have witnessed a growing amount of Ka-band capacity launched in many regions of the world. Fuelled by the growth of bandwidth hungry applications, the demand for satellite capacity has grown similar to other wire line and wireless communications technologies [1].

Considering the scope of transmission at Ka-band, this paper is devoted to the design and development of carrier generator using phase-locked loop (PLL) frequency synthesizer at Ka-band for Indian remote sensing (IRS) applications.

The modern technology of frequency synthesis has been classified into three main categories. They are direct synthesis (DS), digital direct synthesis (DDS), and PLL frequency synthesis. DS has excellent performance in terms of short frequency switching time, but it consumes more power as it needs to integrate filter, mixer, etc. DDS can provide high-resolution and low-phase noise signals, but it has limited operating range and shows weak spurious suppression. PLL synthesizer has a wide output range and a great suppression of spurious frequencies. A PLL design can be integer (N)-based PLL or fractional (F)-based PLL.

In this paper, integer N-type PLL frequency synthesis structure is proposed and implemented. The main idea is to generate X-band carrier signal using PLL frequency synthesizer [2, 3] and multiply it to Ka-band signal using a frequency tripler [4]. The output of the X-band carrier generator is fed to the frequency multiplier with the multiplication factor ($N = 3$) generating a signal at Ka-band.

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The implemented model has excellent performance with resolution of 5.7 MHz, output at Ka-band and phase noise better than −70 dBc/Hz at 1 kHz offset. The measured result for Ka-band carrier phase noise matches with the theoretical values, as described later in this paper.

II. WORKING PRINCIPLE

The block diagram of the PLL frequency synthesizer is shown in Fig. 1. The PLL compares the phase between the signal F_p obtained by dividing the frequency of voltage-controlled oscillator (VCO) by Prescaler and programmable divider and F_c obtained by dividing the reference frequency F_r, and generates a phase error signal which is applied to the VCO through a loop filter to control the output frequency of VCO. This continues till the loop gets looked, i.e., VCO gets locked to the frequency and phase of temperature compensated crystal oscillator (TCXO). The frequency resolution is given by equation (1).

$$F_c = F_r \div (R + 1). \qquad (1)$$

The highly stable reference signal (F_r) of PLL is given by a TCXO. The phase detector input F_p is derived by equation (2)

$$F_P = F_{\text{in}} \div [10(M + 1) + A], \qquad (2)$$

where M and A are the counter values. The output signal from the VCO is fed to the divide by-8 prescaler. This output frequency F_{in} is given by equation (3)

$$F_{\text{in}} = [10(M + 1) + A] \times [Fr \div (R + 1)]. \qquad (3)$$

In the locked condition both equation (1) and (2) must be satisfied. After generating X-band carrier frequency, the output is fed to frequency tripler to generate carrier at Ka-band.

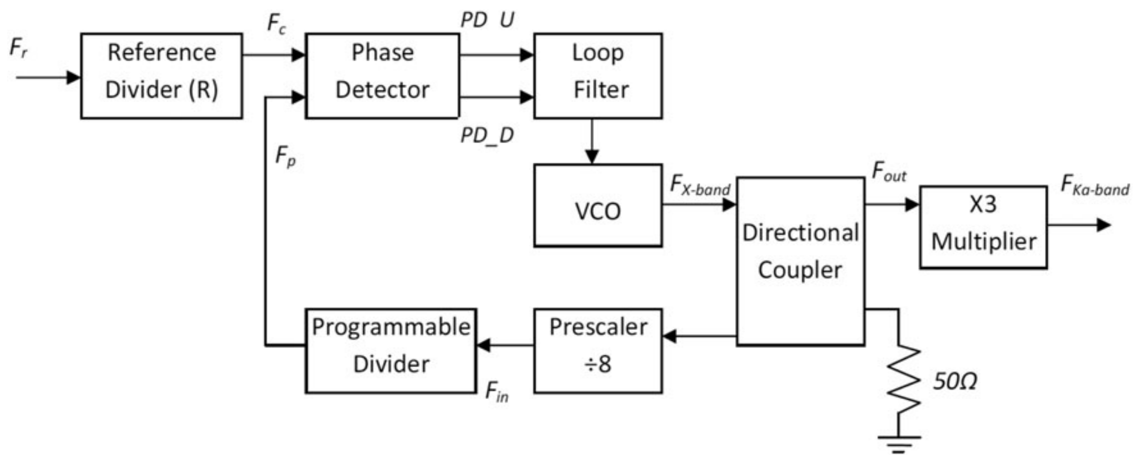

Fig. 1. Block diagram of N-type PLL frequency synthesizer.

III. CIRCUIT IMPLEMENTATION

The described analysis in Section II is used to realize X-band frequency synthesizer and frequency tripler. The circuit design is described in the following parts:

A) Part A

Peregrine's PE83336, a high-performance integer-N PLL chip capable of frequency synthesis up to 3.0 GHz is used. The *PE83336* consists of a prescaler, counters, a phase detector, and control logic as shown in Fig. 2. The dual-modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters "R" and "M" divide the reference and F_{in}, respectively, by integer values stored in a 20-bit register. An additional counter ("A") is used in the modulus select logic. The phase frequency detector generates up and down frequency control signals. The control logic includes a selectable chip interface. Data can be written via serial bus, parallel bus, or hardwired direct to the pins.

The stable reference frequency is given by TCXO. The circuit realization using PE83336 is shown in Fig. 3.

B) Part B

Figure 4 represents the active loop filter used in conjunction with the differential output of the PE83336 phase detector. Since all the parameters of PLL are fixed and specific to the components

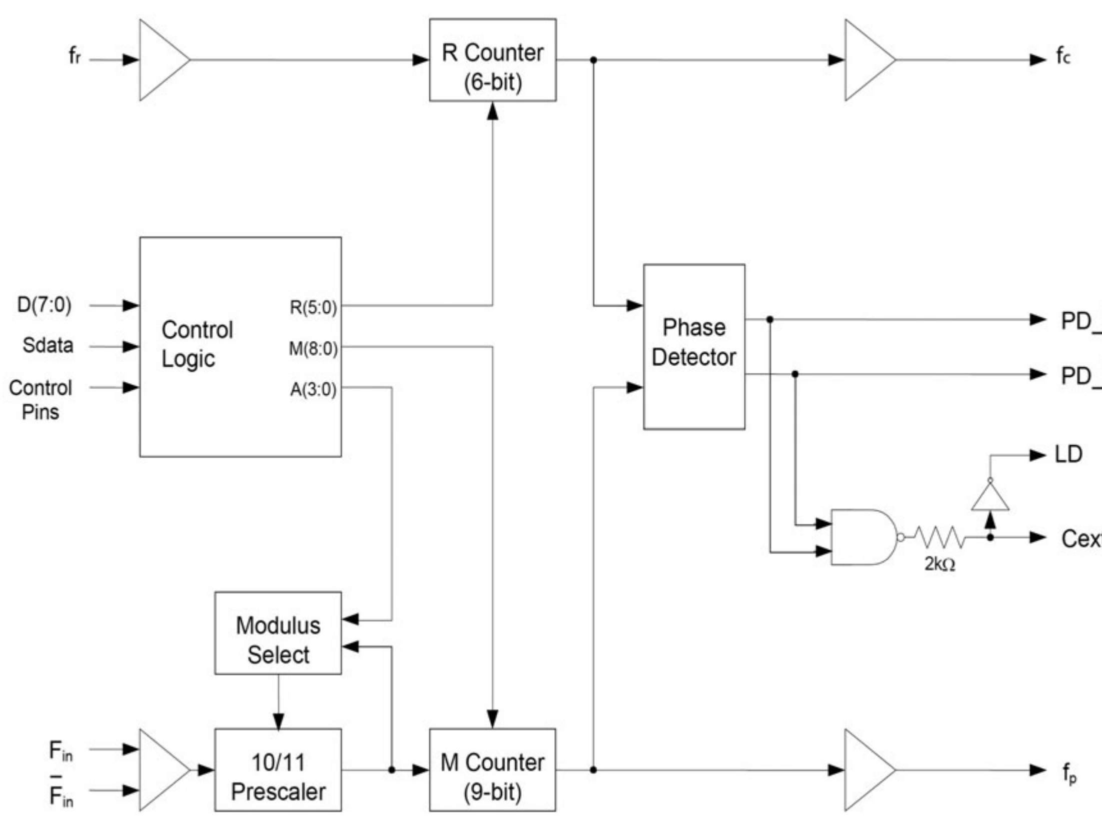

Fig. 2. Functional block diagram of PE83336 IC.

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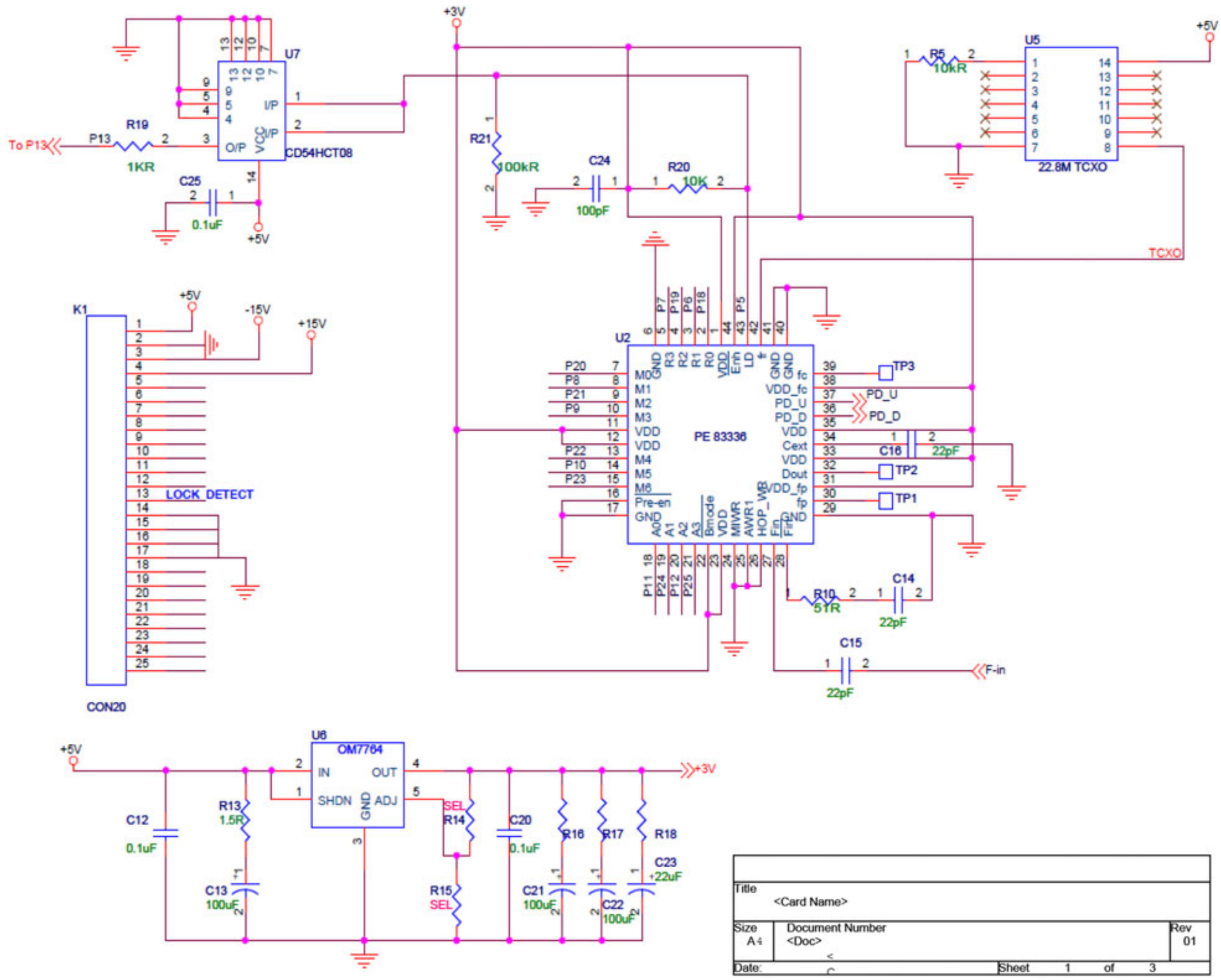

Fig. 3. Circuit realization of phase detector.

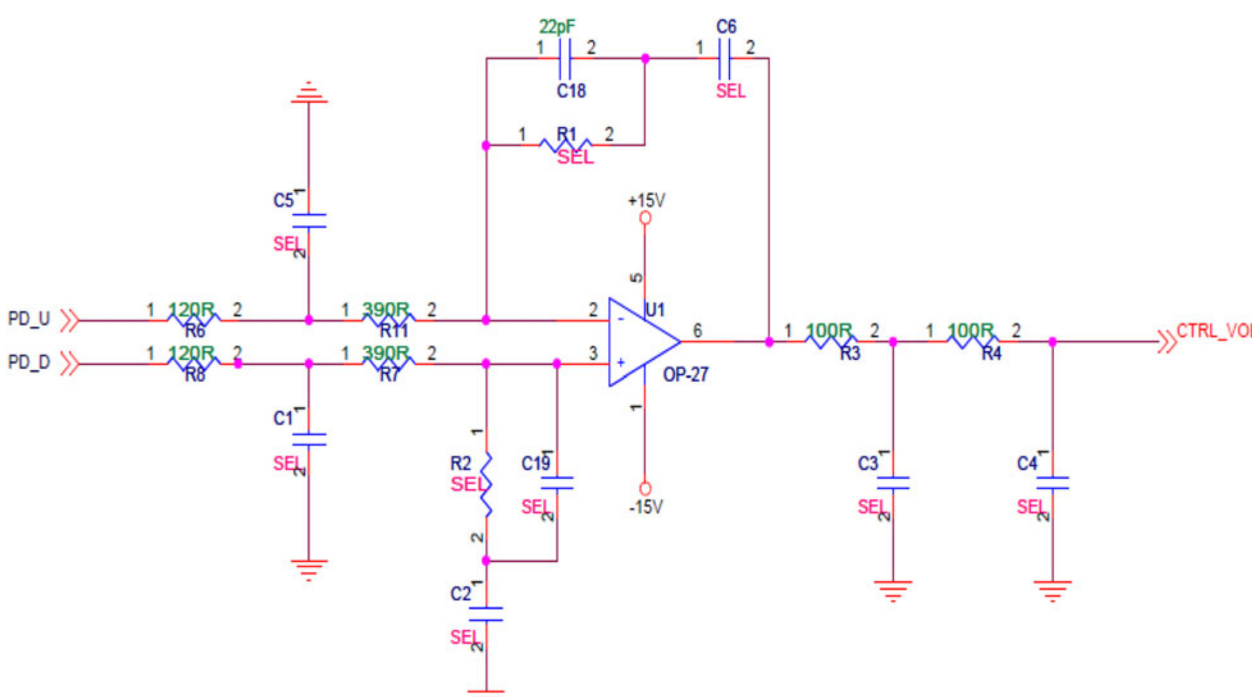

Fig. 4. Circuit realization of loop filter.

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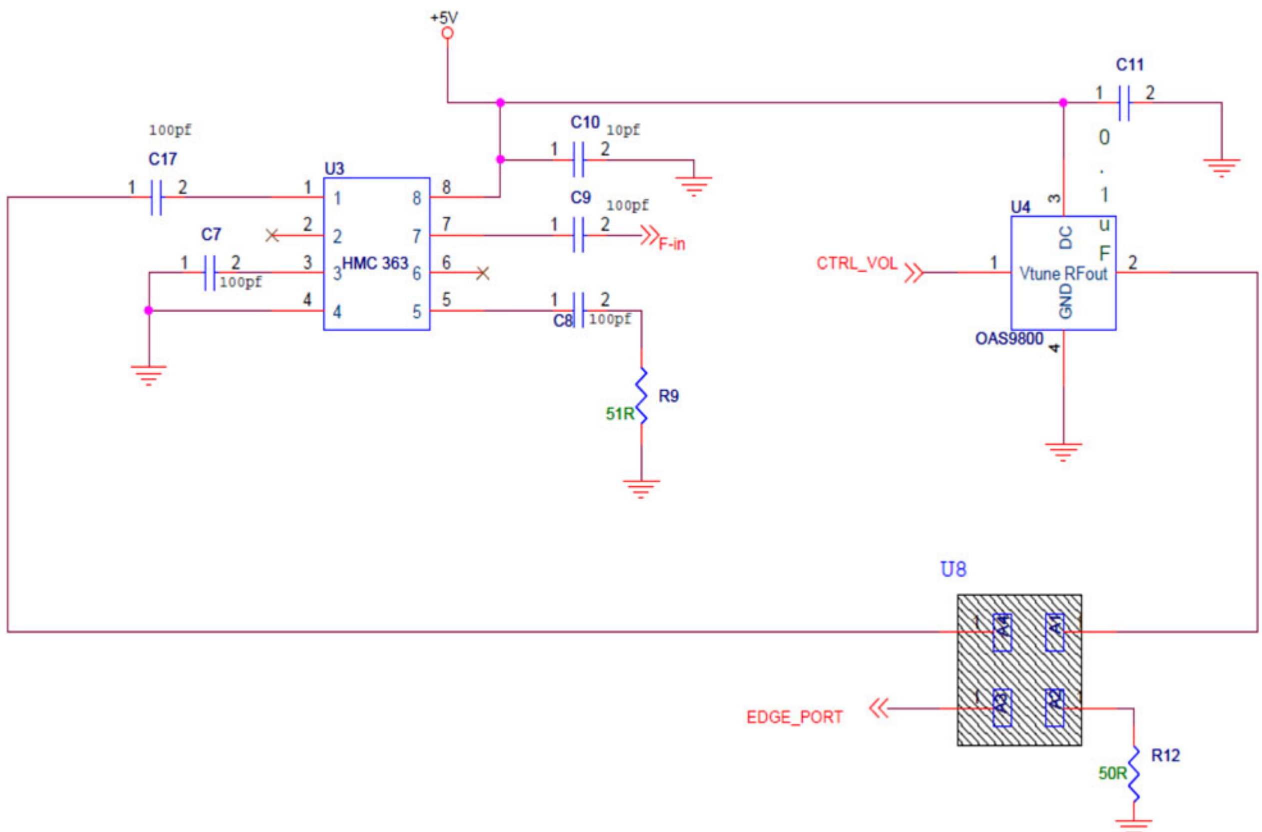

Fig. 5. Circuit realization of VCO and prescaler.

used, the loop filter is the only block that gives a degree of freedom with regard to the design of the PLL, in terms of close-in phase noise characteristics and the lock time. The ideal values of resistor and capacitor in loop filter are gotten from the simulation carried out on Agilent Systemvue software.

The loop bandwidth is chosen such that the phase noise transition from TCXO to VCO is smooth. It is well known that the phase noise inside the loop bandwidth follows the TCXO phase noise multiplied by 20 × log (VCO operating frequency/TCXO operating frequency) and that outside the loop, follows the VCO phase noise. The loop bandwidth of 50 kHz is chosen in our application.

C) Part C

A Teledyne Cougar OAS 8900 VCO with the tuning range of 6900 to 8900 MHz is shown in Fig. 5. The output of the VCO (OAS 8900) is fed back to the PLL IC (PE83336) through a 10-dB coupler and a Divide-by-8 prescaler, so that L-band signal reaches the F_{in} of the PLL IC.

D) Part D

TriQuint TG4040 with an operating band of 17–43 GHz is used for performing frequency multiplication. TG4040 is a medium power amplifier and a multiplier. The part has been developed by TriQuint using its 0.15 um power pHEMT production process. It provides a nominal 25 dB small signal gain with 22 dBm output power at 1 dB gain compression. For X3 Multiplier Function, TGA4040 provides 15 dBm typical Output Power at 9 dBm Pin. The TGA4040 is 100% DC and RF tested on-wafer to ensure performance compliance.

IV. TESTING AND HARDWARE REALIZATION

The design of the Ka-band frequency synthesizer consists of the X-band carrier generator as the first circuit followed by a frequency multiplier. The main technical requirements of the frequency synthesizer are given in Table 1.

The phase noise of the X-band carrier deteriorates from the phase noise of TCXO at 22.8 MHz due to the multiplication effect and can be calculated from equation (4).

$$\text{X} - \text{band carrier phase noise} = \text{Phase noise of TCXO} + 20\ \log\left(F_{out}/F_r\right). \quad (4)$$

The phase noise value of the TCXO is taken from Fig. 6. The X-band carrier phase noise is calculated from (4) and

Table 1. Desired specification.

Specification	Value
Operating frequency band	Ka-band
Phase noise	≤− 70 dBc/Hz at 1 kHz offset
Harmonic suppression	≤− 30 dBc
Spurious	≤− 50 dBc
Reference frequency	22.8 MHz
Output power	7 dBm (minimum)

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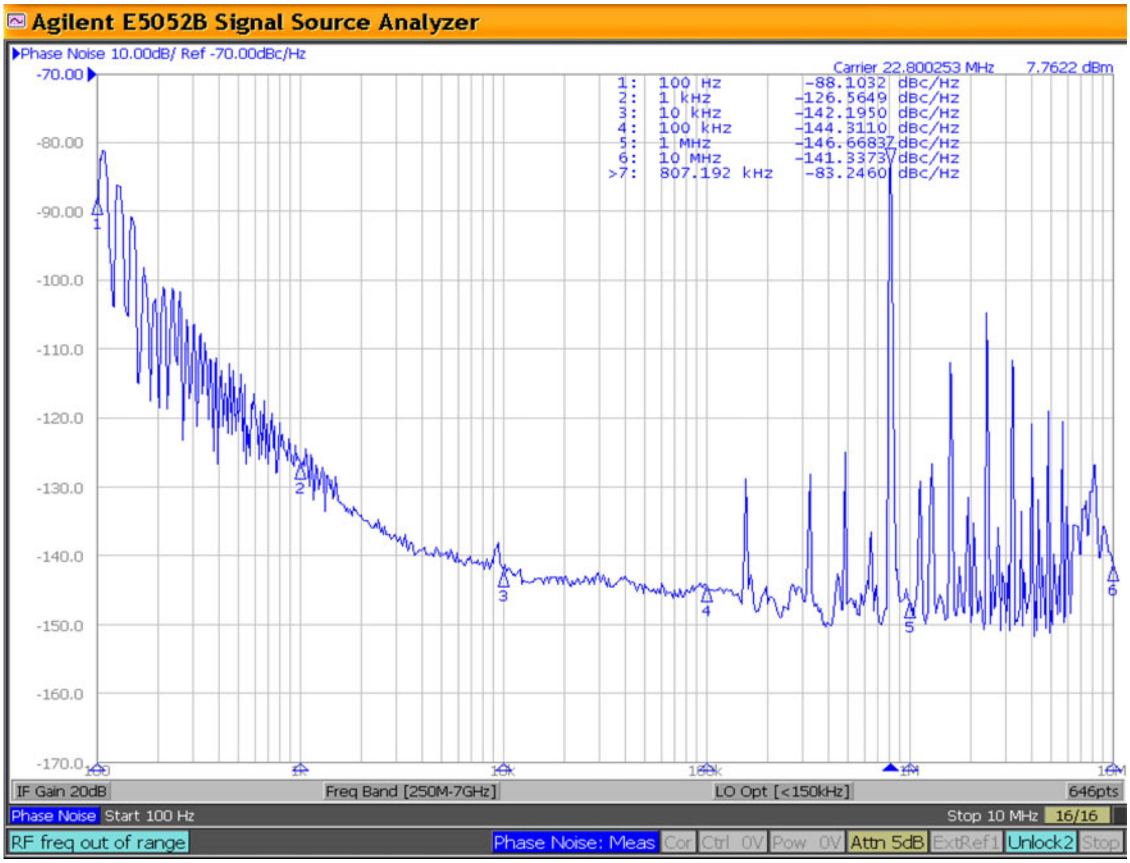

Fig. 6. Phase noise of TCXO.

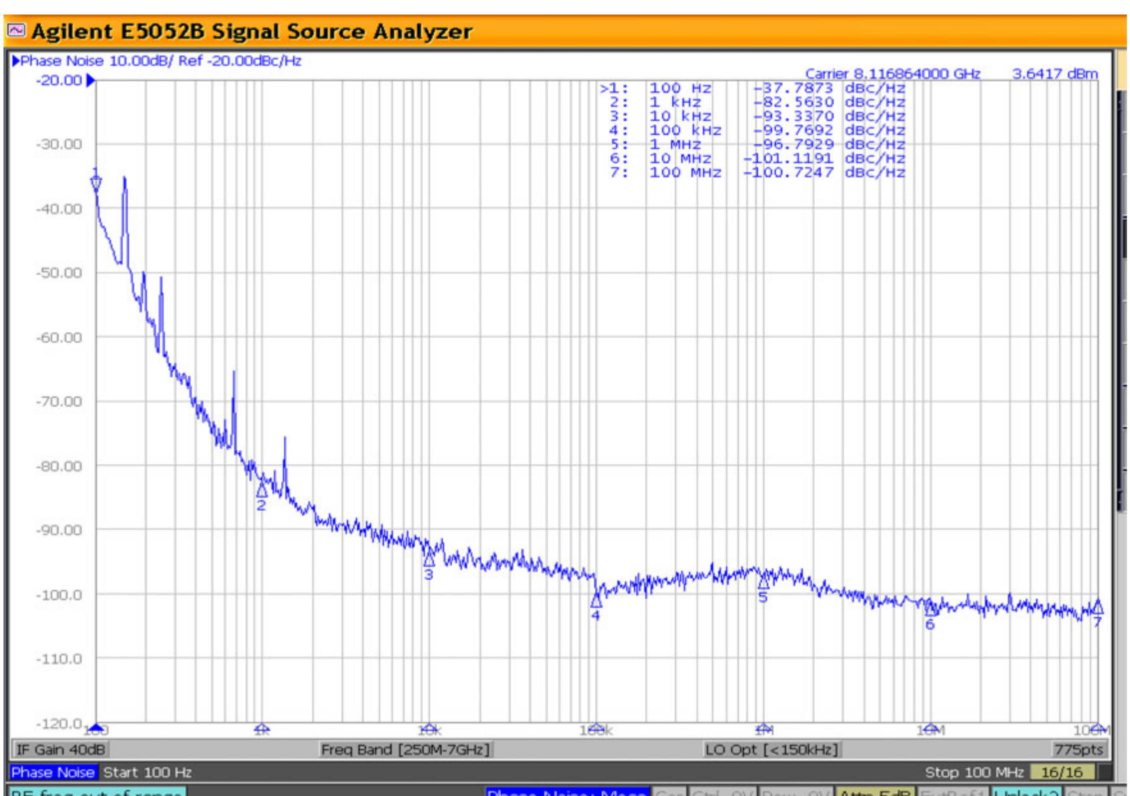

Fig. 7. Phase noise of PLL at X-band.

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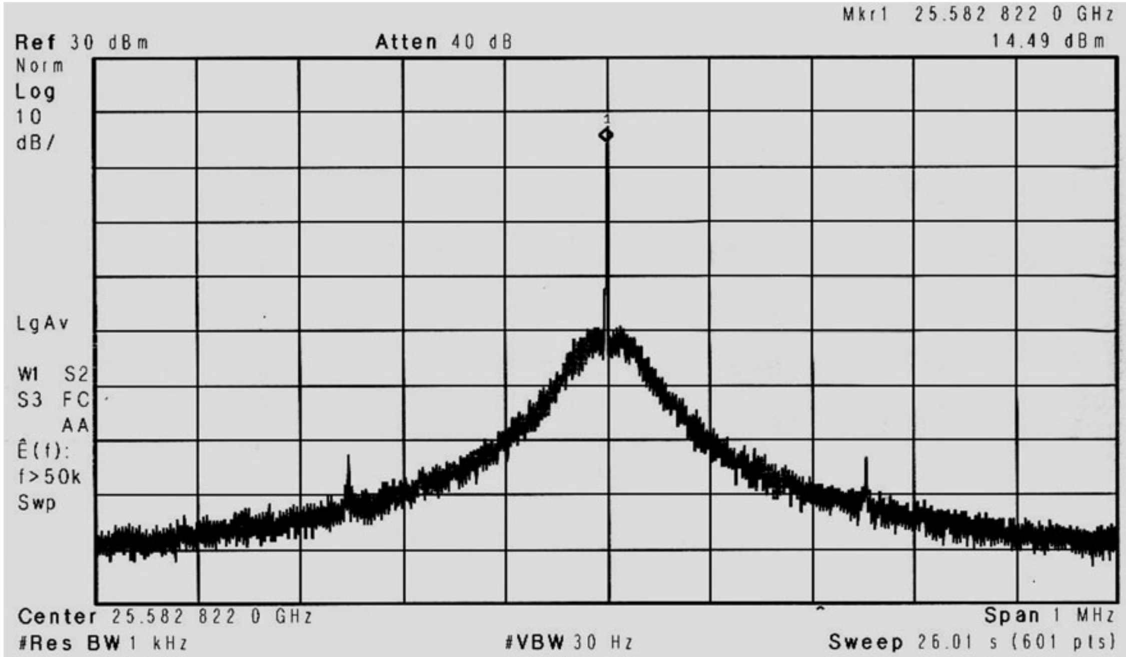

Fig. 8. Frequency synthesizer output at Ka-band for measuring phase noise.

compared to that obtained practically from Fig. 7. The X-band carrier phase noise is −82 dBc/H at 1 kHz offset.

The output of the X-band PLL is multiplied by a frequency tripler and driven through driver amplifier. The minimum phase noise degradation, caused by an ideal frequency multiplier is:

$$\text{Phase noise degradation} = 20 \times LOG(N), \quad (5)$$

where N is the multiplication factor [5]. Thus, a frequency tripler ($N = 3$) degrades phase noise by at least 9.5 dB. The phase noise of X-band carrier is: −82 dBc/Hz at 1 kHz offset. Using a multiplier ($N = 3$), degrades this phase noise by $20 \times \text{LOG}\ (3) = 9.5$ dB, yielding: −82 dBc/Hz + 9.5 dB = −72.5 dBc/Hz at 1 kHz offset at Ka-band. Both X-band carrier and Ka-band carrier phase noises are measured, agreeing with the theoretical estimated phase noise.

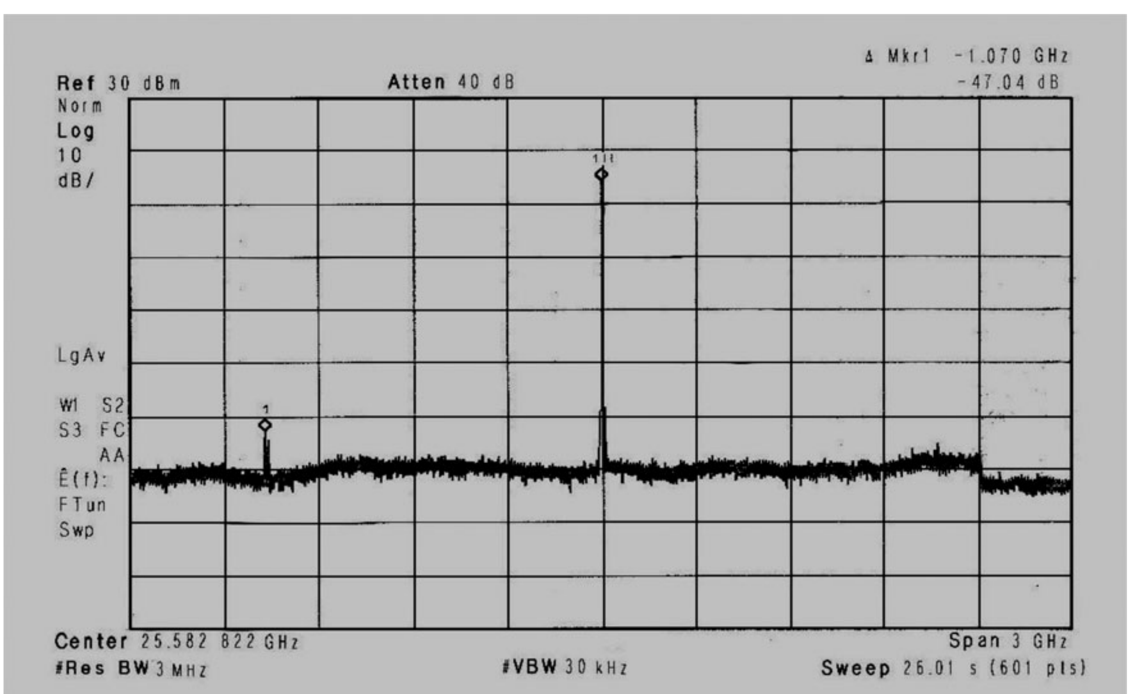

Fig. 9. Frequency synthesizer output at Ka-band showing the spectral purity

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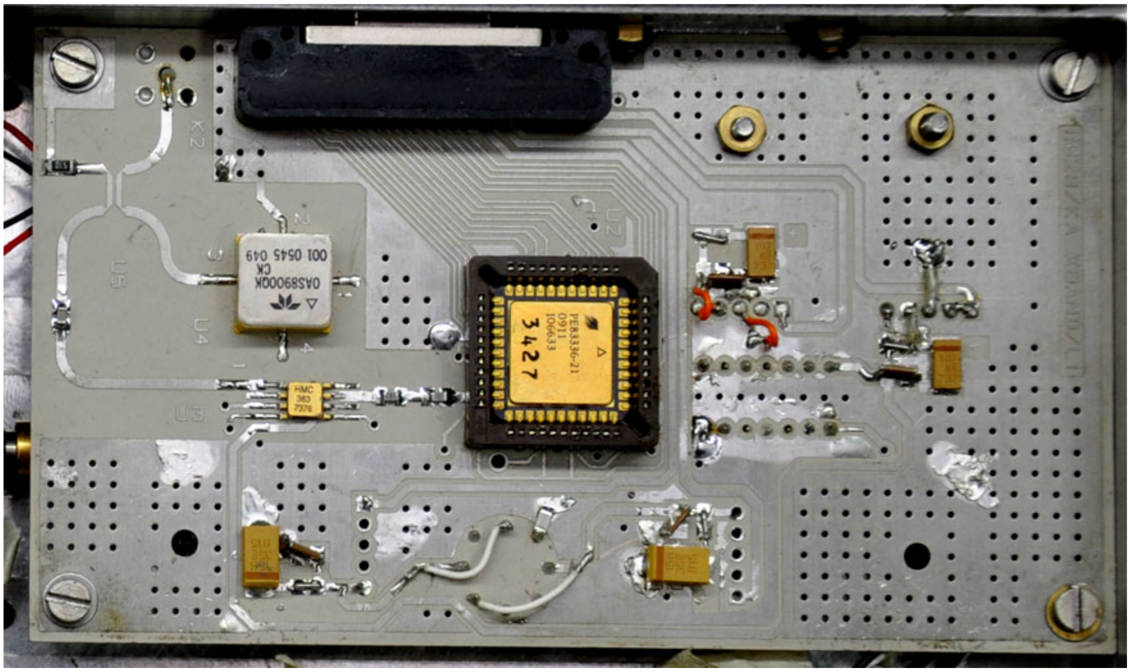

Fig. 10. Top view of fabricated X-band carrier generator on RT-duroid 6010 substrate.

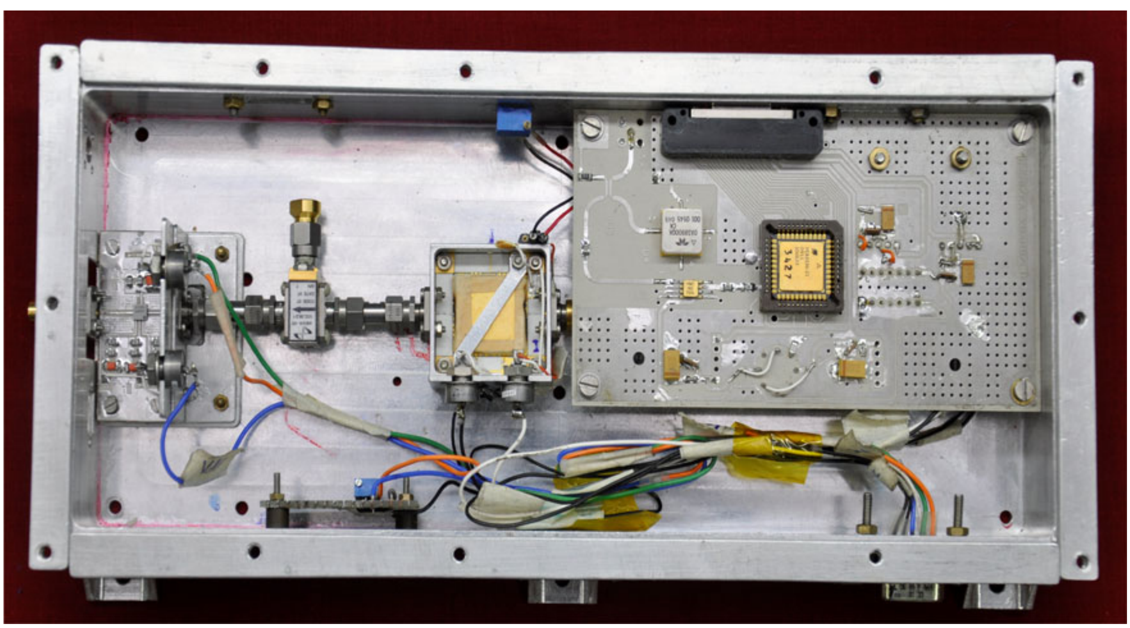

Fig. 11. Top view of X-band carrier generator with X3 multiplier and driver amplifier.

Figures 8 and 9 show the spectrum of the frequency synthesizer output at Ka-band. A spurious of −47 dBc is observed, as seen in Fig. 9, at an offset of 1070 MHz from the carrier, which marginally misses the desired spurious level of −50 dBc or lesser. Hence, an additional bandpass at Ka-band is required, which would provide an attenuation of at least 3 dB at the spurious frequency. Also the phase noise of −70 dBc/Hz at 1 kHz is obtained as seen in Fig. 8, satisfying the theoretical phase noise.

V. CONCLUSION

In this paper, Ka-band frequency synthesizer with PE83336 chip on RT-duroid 6010 substrate is implemented. The proposed model provides an excellent flexibility of carrier generation at both X- and Ka-band frequencies (Figs 10 and 11). The flexibility for changing the frequency at X-band is obtained by the ability to change any of the counter values. The carrier generator achieves the frequency resolution of 5.7 MHz, and phase noise better than −70 dBc/Hz at 1 kHz offset at Ka-band is achieved.

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