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RESEARCH PAPER

A SiGe-based fully-integrated 122-GHz FMCW radar sensor in an eWLB package

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High-performance SiGe HBTs and advancements in packaging processes have enabled system-in-package (SiP) designs for millimeter-wave applications. This paper presents a 122-GHz bistatic frequency modulated continuous wave (FMCW) radar SiP. The intended applications for the SiP are short-range distance and angular position measurements as well as communication links between cooperative radar stations. The chip is realized in a 130-nm SiGe BiCMOS technology and is based on a fully differential frequency-multiplier chain with in phase quadrature phase receiver and a binary phase shift keying modulator in the transmit chain. On-wafer measurement results show a maximum transmit output power of 2.7 dBm and a receiver gain of 11 dB. The chip consumes a DC power of 570 mW at a supply voltage of 3.3 V. The fabricated chip is integrated in an embedded wafer level ball grid array (eWLB) package. Transmit/receive rhombic antenna arrays with eight elements are designed in two eWLB packages with and without backside metal, with a measured peak gain of 11 dBi. The transceiver chip size is 1.8 mm × 2 mm, while the package size is 12 mm × 6 mm, respectively. FMCW measurements have been conducted with a sweep bandwidth of up to 17 GHz and a measured range resolution of 1.5 cm has been demonstrated. 2D positions of multiple targets have been computed using two coherently linked radar stations.

Keywords: Radar, Semiconductor devices and IC-technologies, mm-wave SiGe HBTs

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I. INTRODUCTION

Since the past few years SiGe BiCMOS technology has proven itself as the technology of choice for high performance, highly integrated millimeter-wave (mm-wave) systems especially for commercial applications and markets where cost reduction holds a central importance. SiGe technology has been able to stand up to the III–V semiconductor competition because of its high integration capability, cost effectiveness, and high-temperature performance. On the other hand, as compared with CMOS only systems, SiGe BiCMOS has proven better output power (on account of its higher breakdown voltages) and flicker or 1/*f* noise performance [1, 2]. Furthermore, advancements in packaging techniques and processes supporting mm-wave have added an extra dimension in system approach and design. These milestones have enabled mm-wave and even sub-mm-wave radar and local positioning systems [3], distance and gesture recognition [4], active/passive imaging [5], and ultra-high-speed communication systems [6].

The D-band frequency range, which spans from 110 to 170 GHz, is especially suited for realizing highly compact systems, mainly due to the smaller size of the antennas. Furthermore, systems can still be designed in fundamental mode, because of the sufficiently available gain. The allowable 1-GHz bandwidth in the industrial, scientific and medical (ISM) band provides the extra opportunity for many commercial applications, such as compact sensors for drones/remotely operated aircrafts, automotive radars [7] and for detection and recognition of vulnerable road users [8]. For facilitating such tasks with even better accuracy and resolution, front-ends with higher level of integration and improved system methodology are required. One important and often the most crucial step in system design, which also directly affects the overall cost, are to avoid/improve the bond wire transitions from the chip to the on-Printed circuit board (PCB) antennas. Since there exists no simple possibility to considerably modify the electrical characteristics of these bond wire transitions, one has to tolerate their losses and the bandwidth limitation effects. One way to avoid the bond wire transitions is to utilize an antenna-on-chip (AoC), which however would consume valuable chip area and has inherently low radiation efficiency because of high permittivity and low resistivity of the silicon substrate. Even though the performance of AoCs can be improved by using several techniques such as backside etching [9], proton implantation, and dielectric lenses, all of these techniques, however, require additional processing steps and sometimes even manual procedures, which increase the cost, are time consuming and reduce the reliability of the whole system [10]. A better alternative in terms of performance, robustness, and ease of integration, is to have

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antenna-in-package (AiP) designs, which have a redistribution layer (RDL) for the chip-to-package transitions. This work is an extended version of the reported 122-GHz radar sensor in [11], which focuses on the circuit and antenna design/simulation details, more comprehensive frequency modulated continuous wave (FMCW) radar measurements, as well as using the integrated binary phase shift keying (BPSK) TX modulator to determine two-dimensional (2D) positions of multi-static targets. This paper is organized as follows: Section II presents the overall system-in-package (SiP) concept, architecture, and a comparison with other package solutions. The fully-integrated transceiver design, the circuit topology, and the schematics are described in Section III. This section also presents the simulation results of most of the building blocks. Section IV explains in detail the TX/RX AiP and its optimization process. Section V discusses the on-chip measurement results as well as far-field measurements of the package. The demonstration of the FMCW radar measurements and the determination of the system-level range resolution follows in Section VI. The 2D target localization measurements are also presented in this section.

II. SIP CONCEPT AND ARCHITECTURE

Many successful demonstrations of AiP solutions [12, 13] in the mmW region have established its premise of being an elegant and reliable solution, and its capability of mainstream high-volume production [10]. However, the electrical/radiation performance of the AiP is strongly dependent upon the frequency of operation and the particular packaging technology or material being used. The LTCC (low-temperature co-fired ceramic) process has been used to demonstrate numerous planar antennas or antenna arrays capable of being integrated with MMICs in the W-band [14] and in the D-band [15]. Recently, a packaging solution based on flip-chip technology was presented, which also eliminates bond wire transitions by routing through the antenna substrate. The packaging solution uses flexible polyimide substrate and demonstrated an AiP with 10 dBi gain and 80% radiation efficiency [16]. The embedded wafer ball grid array (eWLB) on account of its small form factor, higher I/O density, integration flexibility and superior mm-wave electrical performance has certainly a distinct advantage over the traditional packages such as BGA or quad flat no leads package (QFN) [17]. One of the major advantages of an eWLB package is the use of a RDL for implementing the chip–package transitions. The electrical behavior of the RDL line can be designed as per the requirements by modifying its layout. The minimum width in the order of a few tens of micrometer of this layer also provides much more flexibility in impedance selection and matching at the chip–antenna interface. It has been shown that a chip–package transition insertion loss in an eWLB package can be about 1 dB better as compared with a very thin QFN package (VQFN) [17].

Figure 1(a) presents a perspective view of the eWLB package, while the RDL transition from the chip pads to the package through a via, is shown in Fig. 1(b). This RDL can eventually feed an AiP or in case of DC/IO pads connects to the BGA, which is finally soldered on a low-cost PCB. Figure 1(c) shows the architecture of the radar sensor, which is based on the fully-integrated 122 GHz transceiver chip. The transceiver chip is integrated in the eWLB package and all the chip-to-package transitions are implemented using the RDL. Since the only high-frequency signal is the 4 GHz or 20 GHz LO signal, the SiP can be mounted on a low-cost PCB via the BGA. This clearly demonstrates the flexibility and cost effectiveness of this solution. It thus provides a platform for easy integration of multiple SiP for MIMO applications. The SiP consists of a single TX and a single RX antenna array arrangement, which forms an FMCW bistatic radar. The bistatic radar provides improved isolation, avoids the use of a hybrid-coupler and is not too much prone to DC-offset problems.

III. FULLY INTEGRATED TRANSCEIVER DESIGN

The block level diagram of the 122-GHz transceiver chip is shown in Fig. 1(c), which is realized in Infineon's advanced SiGe BiCMOS technology B11HFC. The process features HBTs with a minimum effective emitter width of 130 nm, an f_T/f_{max} of 250/370 GHz and a collector–emitter breakdown voltage BV_{CEO} of 1.5 V. Two thick copper layers are available for RF transmission lines, and additional four thin layers for interconnections. The transceiver chip is based on a frequency multiplier chain, as opposed to the alternate solution of using a mm-wave voltage controlled oscillator (VCO) and a subsequent frequency divider. The multiplication factor (M) increases the output phase noise by 20 log M. Off-the-shelf VCOs are available with phase noise in the range of −95 to −100 dBc/Hz at a center frequency of 22 GHz and @100 kHz offset (e.g. Hittite's HMC738LP4 MMIC VCO), which makes the final phase noise performance comparable with or in most of the cases even better than that of mmW VCOs. The receive section of the transceiver consists of a differential in phase quadrature phase (IQ) receiver with Gilbert cell-based down-conversion mixers and a single-stage low noise amplifier (LNA). The quadrature phase is generated using a differential microstrip 3-dB hybrid coupler. The power loss of the LO signal at the coupler is compensated by a buffer amplifier. The transceiver runs on 1.8 and 3.3 V power supplies and consumes only around half a Watt, which is much lower than the maximum power dissipation rating for this package size. It does not require any additional heat sinks, which itself is a major advantage in terms of realizing larger systems.

A) Wideband active balun and buffer

Figure 2(a) shows the simplified schematic of the active balun and the buffer stage. An active balun occupies much less chip area as compared with a passive balun, especially at low microwave frequencies. The active balun is based on a simple AC-coupled common-emitter (CE) topology. In an ideal condition, when no load current is drawn, the collector and emitter terminals of the Q_1 transistor would be 180° out of phase. However, there would be some amplitude imbalance due to the voltage gain provided by the transistor at the collector terminal. To avoid loading Q_1, emitter-followers (EFs) are used together with a fully-differential CE amplifier with resistive degeneration. This increases the common-mode-rejection ratio and thus reduces the amplitude imbalance at the load. The simulated results of the balun and the buffer

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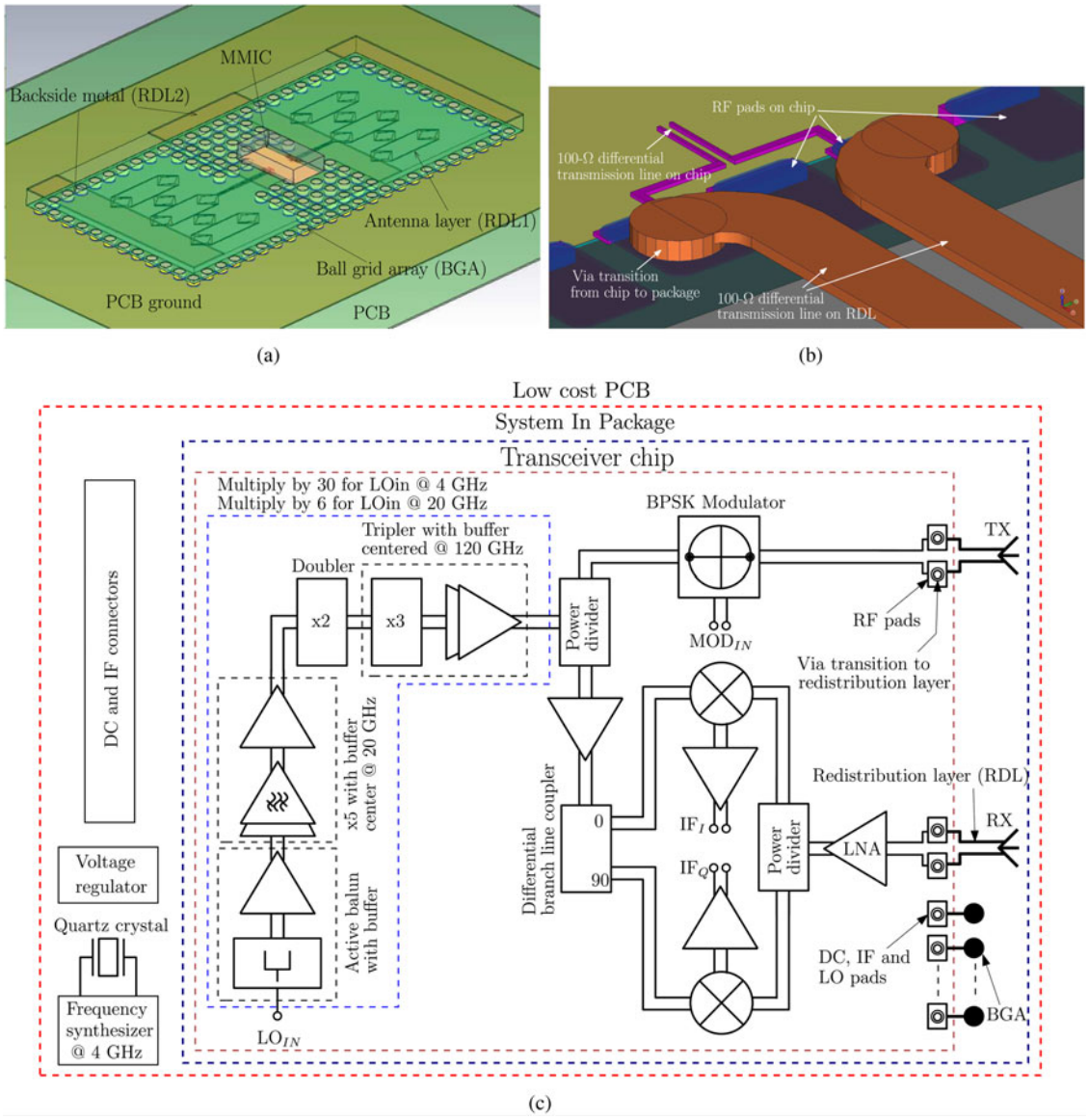

Fig. 1. (a) Perspective view of 122-GHz TRX chip integrated in eWLB package with TX/RX antenna in RDL1 and secondary backside metal in RDL2. (b) Chip-to-package transition in the eWLB package. (c) Block level diagram of the 122-GHz radar sensor showing the chip, SiP, and PCB.

are provided in Fig. 2(b). The circuit shows a wideband performance with a maximum amplitude imbalance of about 1.5 dB and a phase imbalance of $\pm 9^{\circ}$ from 2 to 22 GHz. The simulated compression curves at 4 and 20 GHz plotted in Fig. 2(c), show a saturated power of −3 and 2 dBm, respectively.

B) Frequency multiplier chain

The multiplier chain of the transceiver is designed to provide either a multiplication factor of 30 or 6 depending upon the input frequency of 4 GHz or 20 GHz. The 4 GHz input allows one to utilize low-cost off-the-shelf frequency synthesizers on low-cost PCB. This however produces many harmonics with a separation of 4 GHz. The 20 GHz input signal can still be generated using commercially available VCOs and PLL chips, although they are more expensive. This option however, allows one to attain a much more harmonically clean spectrum.

1) 20-GHz × 5 frequency multiplier and buffer

The ×5 frequency multiplier functionally acts as a fifth-harmonic extractor or as a 20 GHz bandpass filter, depending upon the input frequency. The simplified schematic of the multiplier and the buffer is shown in Fig. 2(d). The core circuit consists of a cascode amplifier whose output frequency is tuned to 20 GHz using a parallel LC resonator at the collector terminal. The 270 pH inductors are realized using two turn spirals. The selectivity of the circuit is enhanced by employing three cascades of the core circuit followed by EFs and a resistively degenerated fully-differential CE amplifier. The simulated results are plotted in Fig. 2(e) for an input power of 0 dBm. The undesired third and seventh harmonic are more than 30 dB down for the LO signal of 4 GHz. For an input LO signal of 20 GHz, the circuit simply behaves as an amplifying stage. As shown in Fig. 2(f), the 20-GHz signal is already saturated at an input power level of −10 dBm.

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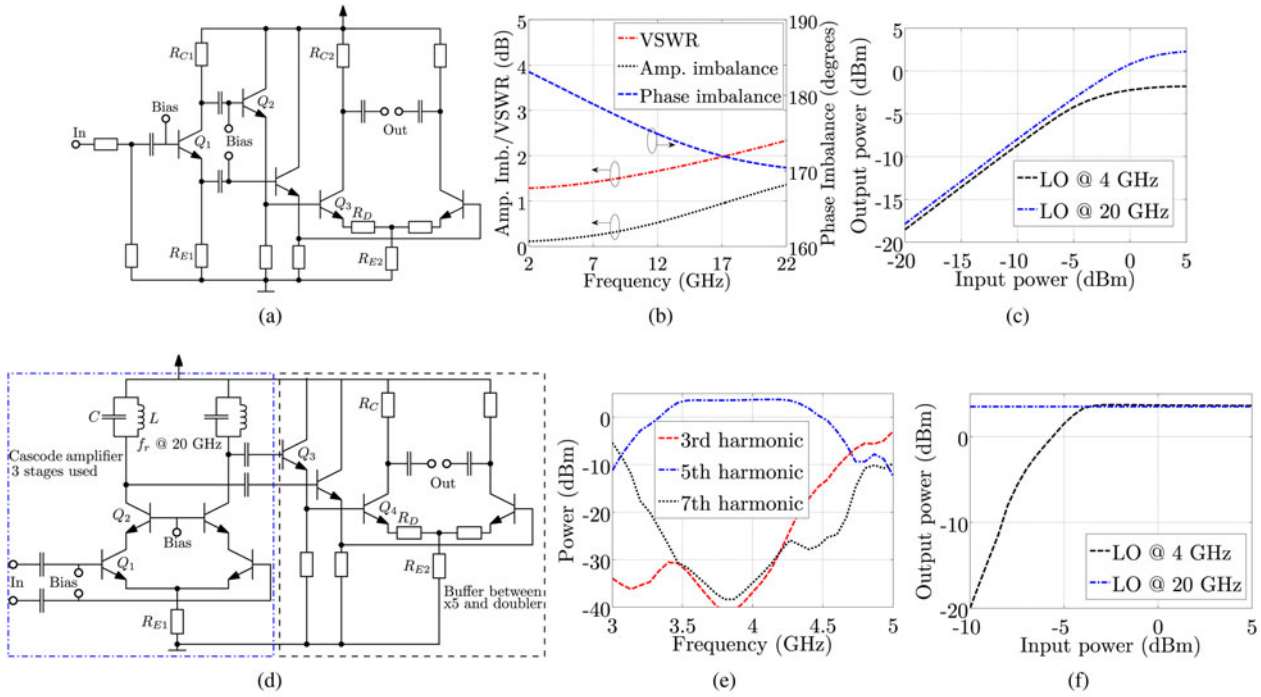

Fig. 2. (a) Simplified schematic of the active balun and buffer capable of working with 4 GHz or 20 GHz LO input signal. (b) Simulated amplitude/phase imbalance and VSWR. (c) P_{OUT} versus P_{IN} curves showing a 1-dB output compression point of −1 and 2.8 dBm at 4 and 20 GHz, respectively. (d) Simplified schematic of the ×5 frequency multiplier and buffer for an input frequency of 4 GHz. (e) Simulated output power of the third, fifth, and seventh harmonic of the ×5 multiplier circuit, at an input power of 0 dBm. (f) P_{OUT} versus P_{IN} (5th harmonic) curves when the input LO signal is 4 and 20 GHz.

2) 40-GHz frequency doubler and active balun

Frequency doubling can be achieved either by using a Gilbert-cell or by a push–push stage. A Gilbert-cell-based doubler requires quadrature phase and stacking of transistors, and therefore requires elevated supply voltage for sufficient gain. However, it produces a differential output signal. On the other hand, a push–push circuit is much simpler and can easily be operated at a lower supply voltage. Therefore, the 40-GHz frequency doubler is designed in a push–push configuration. The balun still can be realized using a single transistor, as shown in Fig. 3(a). The simulated differential output power of the second and fourth harmonic are plotted in Fig. 3(b). This includes the loss incurred at the active balun. The doubler saturates around −1 dBm, as shown in Fig. 3(c).

3) 120-GHz frequency tripler and cascode buffer

This is the last frequency multiplication section in the multiplier chain and governs its overall frequency response. The simplified schematic of the frequency tripler circuit along with the cascode based buffer amplifer is shown in Fig. 3(d). The core circuit is again a CE based amplifier stage which is tuned to the third harmonic of the input signal using a shunt-series output matching network. Since the third harmonic is at a very low amplitude, two cascaded stages of cascode amplifiers are used to boost the signal. The output of the buffer is matched to a differential 30-Ω impedance. This impedance is chosen in order to match it to the parallel combination of the modulator and the LO buffer, which both have a differential input-impedance of 60 Ω. A three-reactive element matching topology is used both for the input and the output, for a wideband operation. A simple T-type differential transmission line power divider is used for splitting the LO signal between the transmit and the receive section. The simulated output power of the third, fifth, and seventh harmonics are shown in Fig. 3(e) at an input power of 0 dBm, indicating a wide bandwidth of more than 30 GHz. For an efficient and wide bandwidth performance it is ensured that each subsequent multiplying unit is saturated in the chain. The tripler/buffer circuit is driven well into saturation by the preceding doubler stage and shows a simulated saturated power of about 3 dBm, as shown in Fig. 3(f).

C) 120-GHz BPSK modulator

The modulator is based on a fully-differential Gilbert-cell topology, as shown in Fig. 4(a). The input modulating signal is directly coupled to the upper quad, while the input RF signal is fed to the transconductance pair. The BPSK modulator is operated on a 3.3-V supply, to provide output power above 0 dBm. The modulator uses HBTs with 9 and 8 μm effective emitter-lengths, respectively.

D) Fully differential IQ receiver

Figure 1(c) shows the receiver architecture. A single-stage cascade-based LNA with an input and output impedance of 100 and 30 Ω, respectively (cf. Fig. 4(c)), is used for moderate amplification. A passive power divider splits the input power to the two down-conversion mixers. Each of the mixers is based on fully-differential Gilbert cell topology, as shown in the simplified schematic in Fig. 4(b). All the HBTs in the quad and the transconductance stage have an effective-emitter

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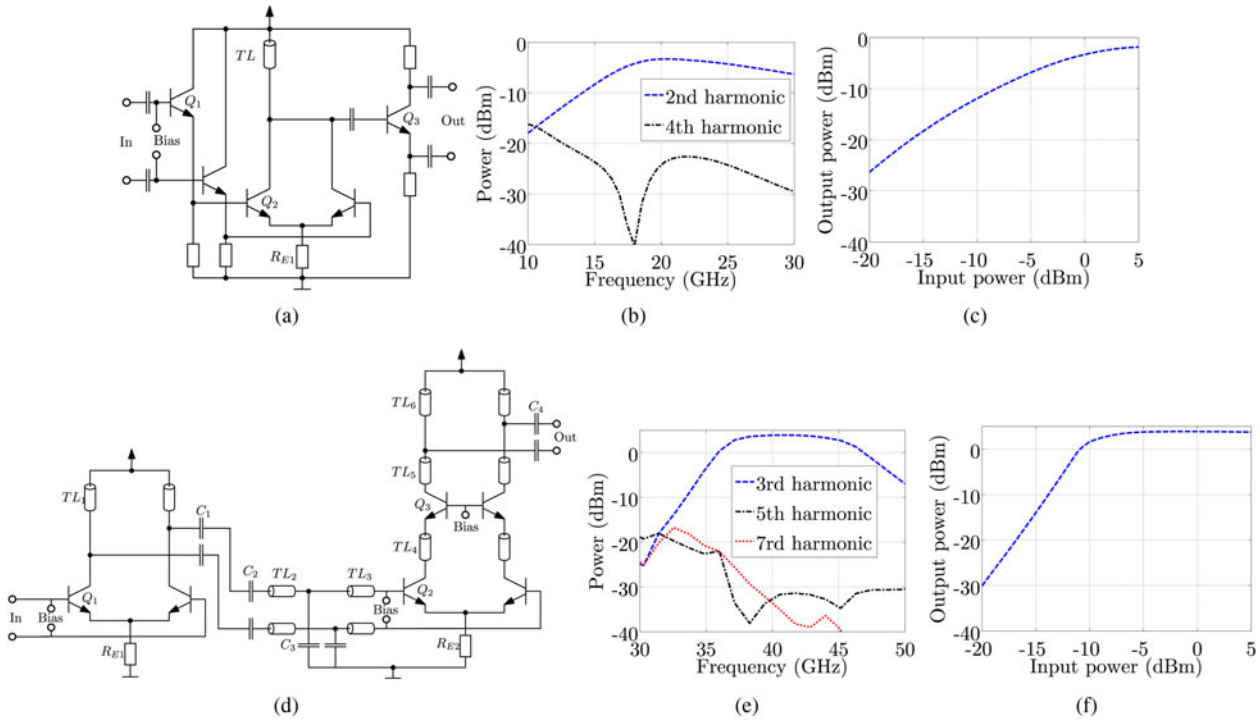

Fig. 3. (a) Simplified schematic of the 40-GHz frequency doubler and active balun. (b) Simulated output power of the second and fourth harmonic, at an input power of 0 dBm. (c) P_{OUT} versus P_{IN} curve at input LO signal of 20 GHz. (d) Simplified schematic of the 120-GHz frequency tripler with cascade-based buffer amplifier. (e) Simulated output power of the third, fifth, and seventh harmonic, at an input power of 0 dBm. (f) P_{OUT} versus P_{IN} curve at input LO signal of 40 GHz.

length of 7 μm and are biased around peak $f_T/2$ current density. EFs utilizing high-voltage HBTs are used at the collector to buffer the output intermediate frequency (IF) signals. To generate the IQ signals for the receiver, a differential 3-dB 90° hybrid coupler was simulated and optimized in Sonnet. A folded structure is selected for reducing the footprint. The coupler achieves a simulated amplitude and phase imbalance of 0.7 dB and 8° over the 110–130 GHz frequency range.

IV. AIP DESIGN

The basic antenna element design for the proposed antenna array configuration is a rhombic AiP with each side length equal to $\lambda_g/4$ (where λ_g is the guided wavelength at 122 GHz), similar to the one presented in [12]. This shape of the antenna is well suited for designing an N-element array, which is fed using a single element and the subsequent elements are connected using half-wavelength lines. Such a configuration reduces the unwanted radiations from the interconnecting feedlines on account of opposite flow of current. In order to fully utilize the fan-out area an eight-element antenna array configuration is selected. Full-wave 3D EM simulations of the packaged antennas are performed in CST Microwave Studio, as can be seen in Fig. 5(a). For improving the return-loss bandwidth of the rhombic element, tapered lines are used instead of uniform widths. The lines are 85 μm at the thickest point (along the y-axis) and linearly tapered to a width of 35 μm. Fig. 5(b) shows the simulated input reflection coefficient of the AiP,

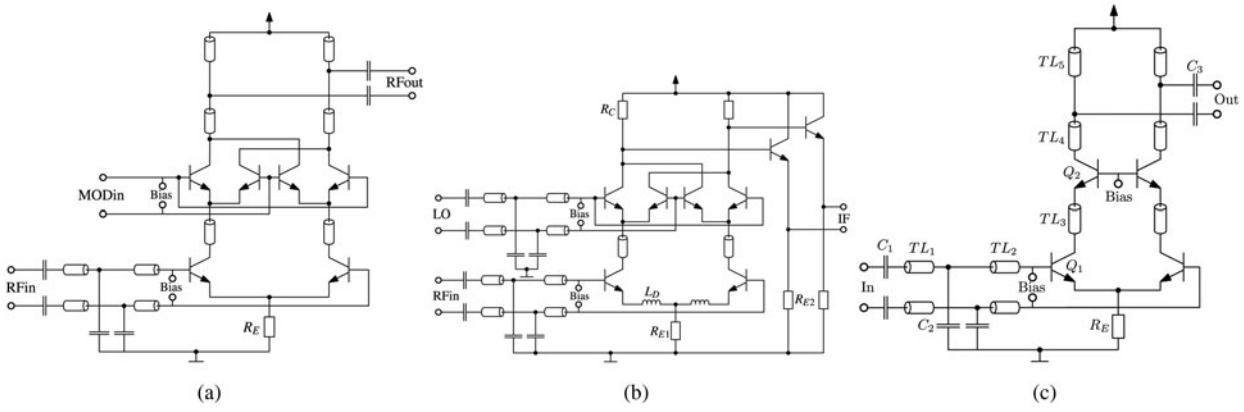

Fig. 4. Simplified schematic of (a) 120-GHz Gilbert-cell-based differential BPSK modulator. (b) 120-GHz Gilbert-cell-based fully differential down-conversion mixer with emitter followers. (c) 120-GHz fully-differential cascade-based low-noise amplifier.

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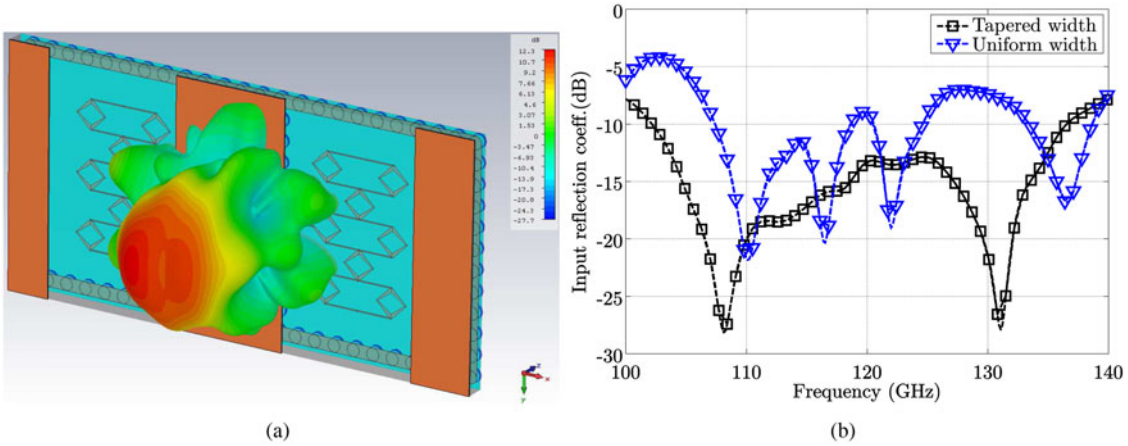

Fig. 5. AiP simulations in CST Microwave Studio. (a) Perspective view of the eWLB package showing the AiP with the backside metal and the 3D far-field simulation results. (b) Simulated input reflection coefficient of the AiP with uniform and tapered lines. It can be seen that the tapering considerably improves the return loss of the antenna.

using elements having uniform-widths and tapered-widths. The improvement in the reflection coefficient magnitude as well as the bandwidth, using the tapered lines, is evident. By using the tapered lines a 10-dB return loss bandwidth of around 30 GHz is achieved. Furthermore, the tapering of the lines does not significantly affect the gain or the radiation pattern. The simulated input impedance of the antenna array is 162 Ω, which is then matched to a 100-Ω

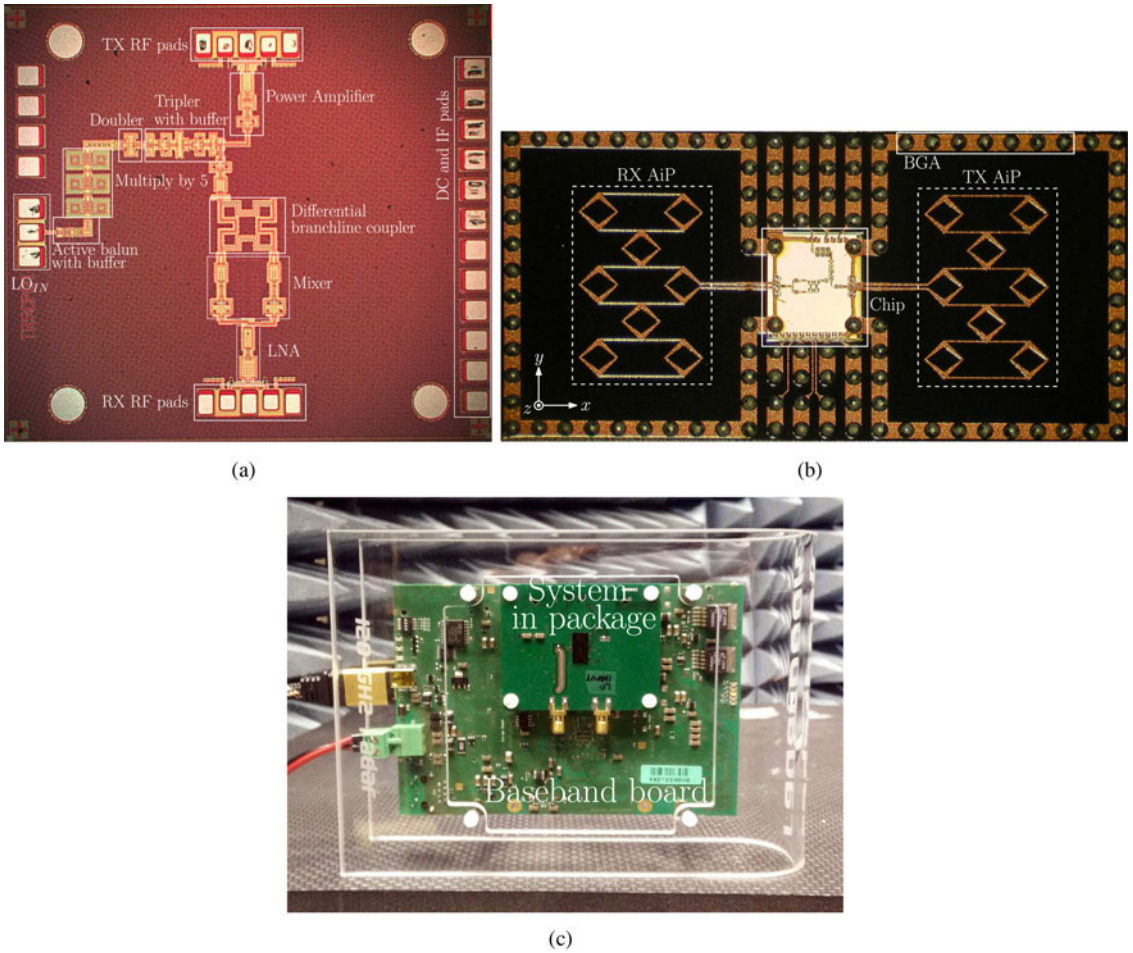

Fig. 6. From chip to system. (a) The 122-GHz transceiver chip with building blocks indicated. Size: 1800μm × 2006μm. (b) The bottom side of the fabricated 122-GHz eWLB package, showing the transceiver chip, the RX/TX antennas on the RDL and the BGA. Size: 12 mm × 8 mm. (c) The 122-GHz package soldered on a low-cost PCB connected to the FPGA-based baseband board with high-performance analog IF processing chain (referred to as the Radar Book (http://www.inras.at/en/products/radarbook.html)).

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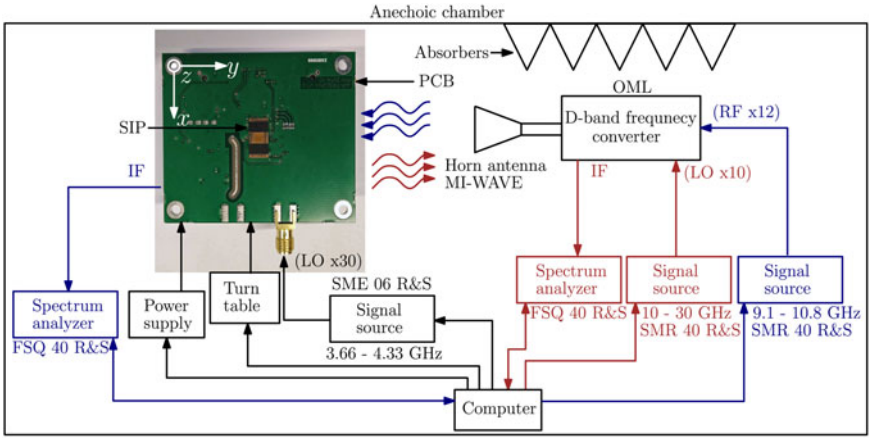

Fig. 7. Block diagram of the measurement setup inside an anechoic chamber. The setup is used for measuring EIRP and the receiver gain, from which antenna gain is calculated. The blue lines and the red lines indicate measurements when the SiP is in receive-only mode and transmit-only mode, respectively. The black lines are used for both transmit and receive measurements.

differential line using a quarter-wave transformer of 126 Ω characteristic impedance. One inherent problem faced while designing antennas in an eWLB package is the generation of standing waves in the package, which tend to produce undesired ripples in the radiation pattern. This effect is especially significant at higher frequencies or when the electrical size of the package is significantly large (more than 3 λ_g) as compared to the operating wavelength. One method to reduce this, as proposed in [18] is to use a backside metal on the RDL2 layer. The tangential components of the electric fields are reduced to zero, providing a secondary aperture. For the proposed AiP, this aperture opening was optimized for higher gain and improved radiation symmetry. For comparison purpose one package was

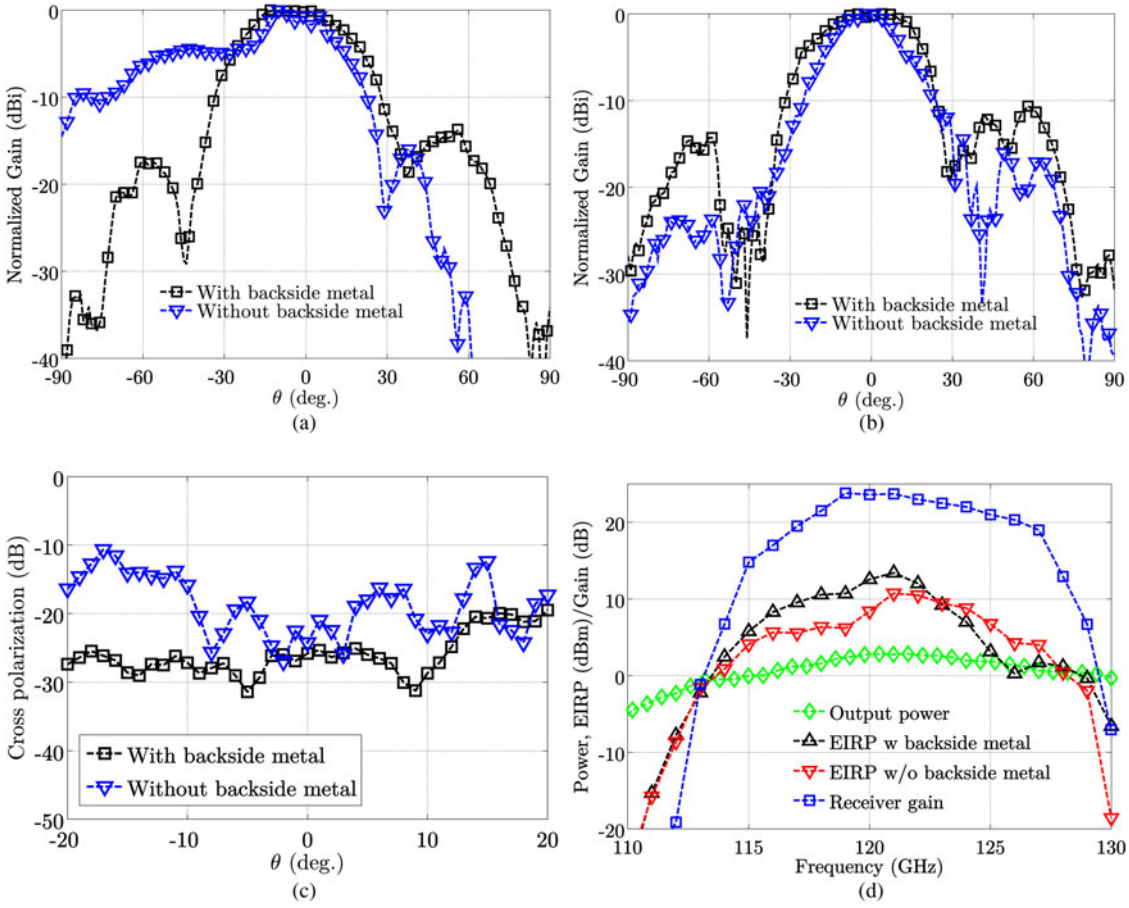

Fig. 8. (a) Measured *H*-plane and (b) *E*-plane radiation pattern of the AiP with and without backside metal at a frequency of 122 GHz. (c) Measured cross-polarization level of the AiP with and without backside metal. (d) Measured on-chip output power, EIRP (with and without backside metal) and receiver gain (including receive antenna).

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Table 1. Performance comparison of D-band radar sensors.

Technology	f_o (GHz)	G_{RX} (dB)	NF (GHz)	P_{1dB} (dBm)	P_{OUT} (dBm)	P_{DC} (mW)	G_{AiP} (dBi)	EIRP (dBm)	BW* GHz	Ref.
0.13 μm SiGe	122	13	11.5	−20	3.6†	0.9	6‡	3.6§	8.7	[19]
0.13 μm SiGe	120	12–36	9.5	−11	0	0.35	11‡	11¶	–	[20]
0.13 μm SiGe	122	23	14	−9	−2.5	0.99	–	–	–	[21]
0.13 μm SiGe	140	8.3**	19.3**	−3**	−1	0.65	–	–	30	[22]
0.13 μm SiGe	122	12	11**	−12**	2.7	0.55	11††	13.7	17	This work

*3-dB BW measured on-chip.
†At transmitter output not including −6 dB antenna coupler.
‡Antenna-on-chip.
§Estimated – does not include focusing lens.
¶Estimated – no direct EIRP measurements shown.
**Simulation results.
††Antenna-in-package.

designed without the backside metal. A simulated peak realized gain of 12.3 dBi is achieved for the AiP with the backside metal (cf. Fig. 5(a)).

V. ON-WAFER AND FAR-FIELD MEASUREMENTS

Figure 6(a) shows the micrograph of the transceiver chip. The dimensions of the chip are 1800 × 2006 μm², which corresponds to 3.6 mm². The on-wafer measurements were carried out using D-band GSG wafer-probes (by GGB), and the second RF-pad was terminated on-chip via laser fuses. The RF power was measured using Agilent's power meter E4416A and a W-band power sensor W8486A. The input LO signal was swept from 3.67 to 4.67 GHz to characterize the ×30 multiplication. The multiplier chain becomes saturated at an input power level of −5 dBm. Far-field measurements for radiation pattern, EIRP and receiver gain are conducted using a waveguide standard gain horn antenna from Mi-Wave (25 dBi) and a D-band OML frequency converter. The detailed measurement setup is shown in Fig. 7. The conversion loss of the D-band frequency converter is de-embedded from the measurements. The radiation pattern of the AiPs with and without the backside metal is measured using an electronically controlled turntable. The measured radiation patterns at a frequency of 122 GHz are presented in Figs 8(a) and 8(b). Both the *E*-plane patterns are quite symmetrical; however, the improvement is much more prominent in the *H*-plane. Furthermore, using the backside metal the antenna has a comparatively wider beam width, which becomes very useful for detecting short-range targets at steep angles. A cross-polarization measurement was performed with the AiPs with and without backside metal. Measurement results presented in Fig. 8(c) show an overall better performance with the backside metal. Figure 8(d) shows the measured on-wafer output power, EIRP of the two packages with and without backside and the receiver gain. The first step is the measurement of EIRP, when the D-band frequency converter is used in a receive mode by connecting an LO signal:

$$\text{EIRP}_{SiP} = P_R + L_{FS} - G_{std}, \tag{1}$$

where P_R is the received power measured at the D-band converters, L_{FS} is the free-space loss, and G_{std} is the gain of the standard gain horn antenna. The AiP gain (G_{AiP}) is then calculated using the measured on-chip output power of the chip. In the second step, the D-band converters are used in transmit mode by connecting the RF signal to the converters. The in-package receiver gain including the AiP gain is then

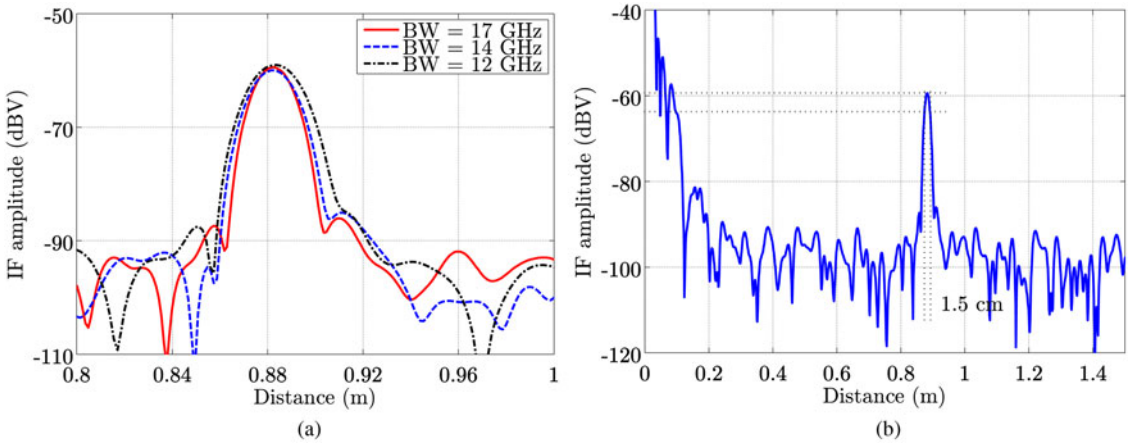

Fig. 9. Measured IF amplitude spectrum with a single static corner reflector using a Hann window. (a) Comparison of measured IF amplitude spectrum for sweep bandwidths of 12, 14 and 17 GHz. (b) Zoomed-out amplitude spectrum of the target with a 17 GHz sweep bandwidth showing a 3-dB width of 1.5 cm, to demonstrate the achieved resolution.

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calculated using

$$G_{RX} + G_{AiP} = P_{IF} + L_{FS} - \mathrm{EIRP}_{converter}, \quad (2)$$

where G_{RX} and P_{IF} are the on-chip receiver gain and measured IF power of the chip.

The SiP achieves a peak EIRP of 13.7 dBm (cf. Fig. 8(d)), which is the highest reported EIRP for D-band radar sensors without using a lens (cf. Table 1). It has a −10 dB EIRP bandwidth (when driven by the 4-GHz LO signal) of more than 10 GHz. The in-package receiver gain is more than 20 dB at 122 GHz.

VI. FMCW RADAR SYSTEM MEASUREMENTS

A) Range resolution measurements

For determining the system-level bandwidth performance of the SiP, which translates to the achieved range resolution, the 122-GHz radar SiP mounted on the Radar Book was tested in an anechoic chamber with a small corner reflector with a radar cross-section (RCS) of −3.5 dBsm. A 20-GHz Hittite MMIC VCO stabilized by a phase-locked loop (PLL) is configured with the Radar Book to generate broadband linear FMCW chirps. A ramp duration of 1.2 ms was used for all the measurements. Two sets of measurements were

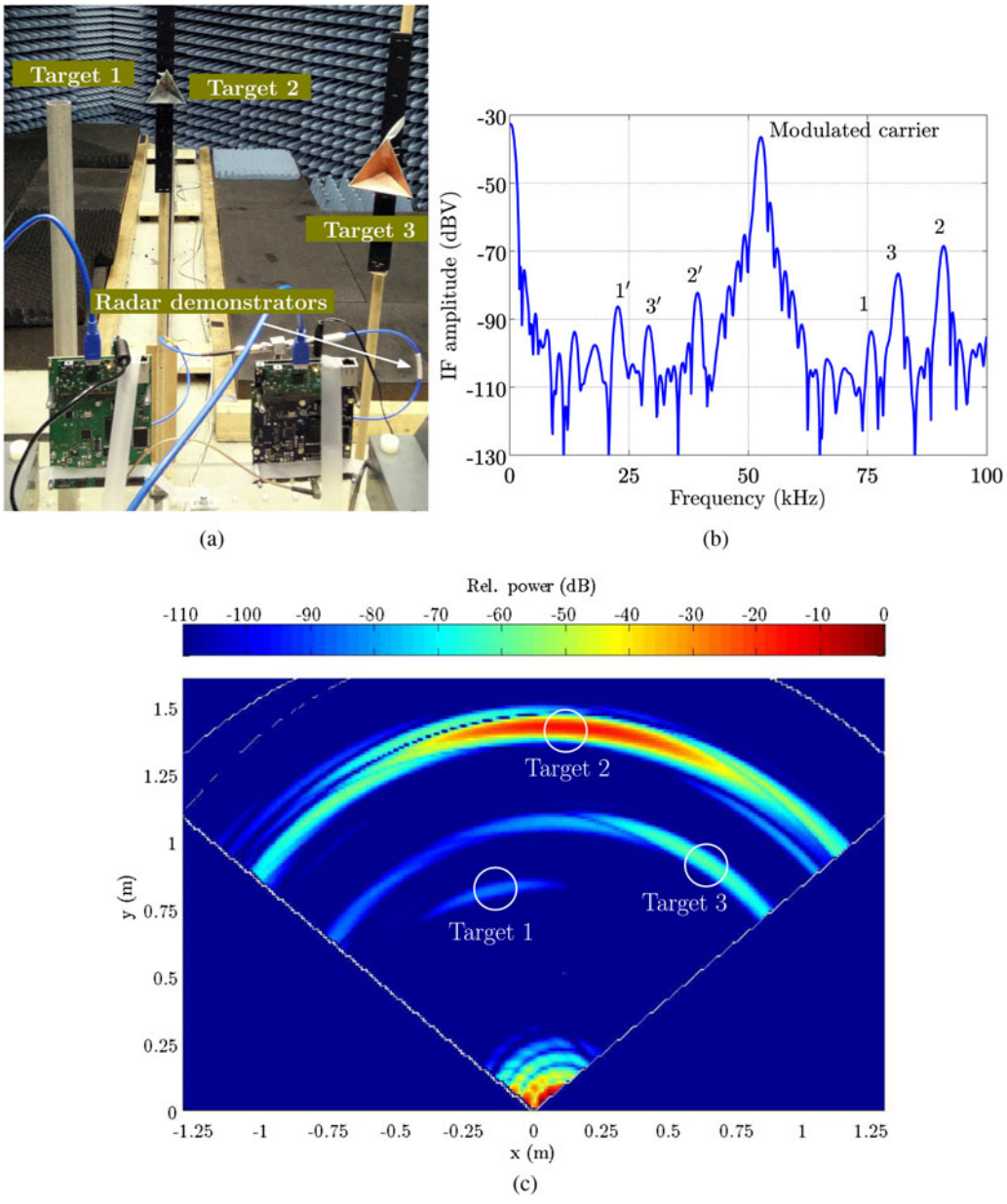

Fig. 10. (a) Static multi-target setup in an anechoic chamber consisting of a metallic pole (target 1) and two corner reflectors (targets 2 and 3). Measurements are taken using two synchronized radars placed 20 cm apart. Radar 1 is working in a classical FMCW configuration with no modulation, while radar 2 utilizes an identical chirp with a BPSK-modulated signal at a bit-rate of 104 kbps. (b) Measured IF spectrum of the radar 2. The modulated carrier is seen at a frequency of 52 kHz. Peaks representing 1′, 2′, and 3′ are the target signals from radar 1 TX, whereas peaks indicated by 1, 2, and 3 are the target signals from the modulated chirps (radar 2 TX). (c) Calculated 2D position of the three targets by using the measured IF spectra.

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performed with a sweep bandwidth of 12 and 14 GHz with an f_{start} of 114 GHz. A third measurement was taken with an f_{start} of 113 GHz and was swept for 17 GHz. The measured IF amplitude spectra are presented in Fig. 9(a). The null-to-null distances for the case of 12, 14, and 17 GHz sweep bandwidths are 5.4, 4.8, and 4.1 cm, respectively, which correspond well to the theoretical values (which are 5, 4.2, and 3.5 cm, respectively), considering that the measurements now include the bandwidth limitation due to the chip-to-package transition, as well as the antenna. A 3-dB width of 1.5 cm is achieved with a 17 GHz sweep bandwidth demonstrating the attained range resolution, as shown in Fig. 9(b). To further evaluate the quality of the measurement results, 500 individual range measurements were taken showing a standard deviation of about 90 μm.

B) 2D Position measurements using BPSK TX modulator

To demonstrate one possible application of a BPSK-modulated FMCW radar, a static multi-target setup was arranged in an anechoic chamber, as shown in Fig. 10(a). Target 1 is a metallic pole (19.4 dBsm), while targets 2 and 3 are small corner cube reflectors (14.0 dBsm), placed at different angles and distances. Two radar systems with identical chips ($f_{start} = 119$ GHz, $f_{stop} = 123$ GHz, $T_{sweep} = 1.2$ ms) are placed 20 cm apart. Radar 1 uses unmodulated chirps, while radar 2 utilizes a BPSK-modulated TX signal with a data rate of 104 kbps. In this scenario, each radar receives the reflected version of its own transmitted signal as well as from the other station. The reflected signals from the two radars remain isolated from each other because of the BPSK modulation. Figure 10(b) shows the IF signal received at the radar 2, showing the direct targets signals (1, 2, and 3, with overall higher amplitude) and the target signals transmitted by the radar 1 (1′, 2′, and 3′). Since the distance between the radars is known and the distances of the targets from each radars are measured, the 2D position of the targets can be computed. This is shown in Fig. 10(c). Each of the targets is marked with a circle. The signals at the origin represent the TX–RX crosstalk. The 2D positions are computed with direct target responses from radars 1 and 2 using a single measurement, and do not utilize the indirect target responses (from radar 1 to radar 2, and vice versa), which can still lead to further accuracy improvement.

VII. CONCLUSION

This paper has presented a 122-GHz FMCW SiP with a BPSK transmit modulator. Detailed characterizations of the transceiver chip and the AiP have been shown. The SiP demonstrates the highest EIRP for D-band radars, without using any external lens. A performance comparison of the presented SiP is presented in Table 1. FMCW measurements show a range resolution up to 1.5 cm at a sweep bandwidth of 17 GHz. The application of the TX BPSK modulator in determining 2D positions of targets has been demonstrated. The SiP with its less than half-a-Watt power consumption, good EIRP and bandwidth of 17 GHz is an excellent candidate for being used for imaging applications, cooperative radars, and air-borne target localization as well as for other sophisticated MIMO applications.

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