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Fully integrated 60 GHz transceiver in SiGe BiCMOS, RF modules, and 3.6 Gbit/s OFDM data transmission

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A fully integrated transmitter (TX) and receiver (RX) front-end chipset, produced in 0.25 μm SiGe:C bipolar and complementary metal oxide semiconductor (BiCMOS) technology, is presented. The front-end is intended for high-speed wireless communication in the unlicensed ISM band of 9 GHz around 60 GHz. The TXand RX features a modified heterodyne topology with a sliding intermediate frequency. The TX features a 12 GHz in-phase and quadrature (I/Q) mixer, an intermediate frequency (IF) amplifier, a phase-locked loop, a 60 GHz mixer, an image-rejection filter, and a power amplifier. The RX features a low-noise amplifier (LNA), a 60 GHz mixer, a phase-locked loop (PLL), and an IF demodulator. The measured 1-dB compression point at the TX output is 12.6 dBm and the saturated power is 16.2 dBm. The LNA has measured noise figure of 6.5 dB at 60 GHz. Error-free data transmission with a 16 quadrature amplitude modulation (QAM) orthogonal frequency-division multiplexing (OFDM) signal and data rate of 3.6 Gbit/s (without coding 4.8 Gbit/s) over 15 m was demonstrated. This is the best reported result regarding both the data rate and transmission distance in SiGe and CMOS without beamforming.

Keywords: 60 GHz, Transmitter, Receiver, SiGe BiCMOS

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I. INTRODUCTION

At 60 GHz an unlicensed frequency bandwidth from several GHz up to even 9 GHz is available all over the world. It offers unprecedented bandwidth for ISM-band applications and creates the opportunity for wireless communication applications with data rates in the order of several Gbit/s. In recent years, with the availability of millimeter-wave SiGe BiCMOS and CMOS technology, intense research started out in the area of highly integrated silicon transceivers for 60 GHz. The promise of Gbit/s wireless connectivity and low cost due to large-scale integration of digital logic with the RF transceiver on a single die evoked very strong interest of the industry, too. This led to various standardization activities of 60 GHz MACs and PHYs within IEEE 802.15.3c and ECMA-387. IEEE 802.11ad is expected to be released soon.

The first integrated silicon transmitter (TX) and receiver (RX) chips operating in the 60 GHz range were published in 2006 by IBM [1] and IHP [2]. Since then 60 GHz, wireless technology was continuously improved. Nowadays, three main trends can be observed. The first is the increase in the performance, i.e. larger data rates and larger communication distance. The second trend is the shift from SiGe BiCMOS to CMOS technology to reduce the power dissipation and cost. The third trend is the introduction of beamforming. Beamforming is implemented to boost the link budget and to allow non-line-of-sight communication.

This review paper summarizes in a comprehensive way our work on a 60 GHz single-antenna SiGe BiCMOS RF transceiver. The transceiver design was specifically targeted on compliance with the IEEE 802.15.3c standard which includes OFDM signaling, and a range of at least 10 m.

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II. RF IMPAIRMENTS AND 60 GHZ OFDM TRANSCEIVER DESIGN

A) Linearity and output power back-off

OFDM signals exhibit high peak-to-average power ratio (PAPR) and are much more sensitive to non-linear effects than single-carrier-modulated signals. Non-linear signal processing causes cross modulation of OFDM sub-carriers which results in a degradation of the sub-carrier signal-to-noise ratio (SNR). Besides that, non-linearity in the TX causes an increase of side-band power which may cause a violation of the spectral mask by the TX ("spectral regrowth"). Due to these effects, power amplifiers (PAs) and complete transmitters are operated with significant output power back-off (PBO) from their 1 dB compression point (P1 dB) with the PBO being close to the range of the PAPR. In order to achieve high transmit power and range, a major design goal was as high as possible P1 dB. Most critical TX components in this regard are the up-mixer and the PA which were specifically optimized for a high P1 dB [3, 4] and will be described in Section III.

System simulations including RF impairments were performed to assess the effect of the SiGe PA non-linearity on the OFDM signal [5]. The PA from [3] has a maximum output P1 dB of 17 dBm. Its characteristic was simulated on transistor level and modeled by fitting the Rapp model to the PA characteristic. OFDM signals with similar parameters to IEEE 802.15.3c were used as input signals. Simulations with different input powers showed that for a PBO >3 dB AM-to-PM distortion was smaller than 1° and, hence, negligible. Spectral regrowth was simulated as well and showed that for a PBO equal or larger than 4 dB the IEEE 802.15.3c mask was not violated. Finally, the BER and sub-carrier SNR for a 16-QAM with three-fourth coding at different input signal powers were simulated. The simulation showed that the sub-carrier SNR degradation is less than 1 dB if the PBO is at least 4 dB. In summary, the system simulations indicated that a PBO of 4–5 dB seems sufficient with the given PA in order to achieve negligible OFDM signal degradation and fulfill the spectral mask. In our transmission experiments the estimated PBO is 4–5 dB.

B) Phase noise requirements

The IEEE 802.15.3c WPAN task group and the WirelessHD consortium have agreed on important common parameters such as center frequencies and channel bandwidth. The standard was designed to be compatible with silicon-based low-cost implementations such as CMOS or SiGe BiCMOS technologies. For the IEEE standard, four frequencies from 58.32 to 64.8 GHz must be synthesized. The AFE presented in this paper features a PLL that provides one of the four frequencies, and the next version will integrate a new PLL that covers all four frequencies.

The effect of phase noise becomes serious if OFDM is used, since phase noise in the synthesizer destroys the orthogonality between the sub-carriers in an OFDM system. The main contributor to the rms phase error in an integrated PLL for 60 GHz is the integrated voltage controlled oscillator (VCO), especially if a large tuning range is required. Another critical noise source is the crystal oscillator, especially in case of a low-frequency crystal reference. The third major contributor is the charge pump noise. As discussed in [6], the rms phase error of the PLL frequency synthesizer should be below 3° for an acceptable bit-error rate (BER) in a transceiver using 16-QAM OFDM transmission. For minimizing the phase error, the input noise (crystal oscillator, charge pump) must be traded off against VCO noise. Fortunately, the bandwidth trade-off is much relaxed by the digital baseband filtering, where the common phase error is eliminated after down-conversion of the intermediate frequency (IF) signal to the baseband. This has an equivalent high-pass effect on the phase noise spectrum modeled as $H_{OFDM}(f) = 1 - \mathrm{sinc}^2(fT_u)$, where $T_u =$ 193.93939 ns is the useful symbol time – the inverse of the sub-carrier spacing $\Delta f =$ 5.15625 MHz [6]. These numbers are valid for both the IEEE 802.15.3c standard and the emerging 802.11ad standard for wireless personal area network in the 60 GHz band.

III. 60 GHZ TRANSMITTER

Figure 1 shows the TX front-end block diagram. The TX front-end consists of a 12 GHz I/Q mixer, an IF amplifier, a PLL, a 60 GHz mixer, an image-rejection filter, and a PA [7]. Differential I and Q input signals are fed into a quadrature mixer. The mixer consists of linearized double-balanced Gilbert cells. It is followed by an IF buffer. The input signals are up-converted with a quadrature 12 GHz signal from the PLL. The quadrature mixer biasing can be controlled with an integrated serial peripheral interface (SPI). The dc currents of the two branches of each double-balanced mixer can be separately controlled. This allows optimization of side-band suppression and conversion gain. A double-balanced Gilbert cell is used as upconversion mixer core for the second upconversion. The upconverter is optimized for high output P1 dB. The IF signal is upconverted in the mixer with the 48 GHz oscillator signal from the integrated PLL. The result is a double-side-band spectrum with a signal at 60 GHz and an out-of-band image at 36 GHz.

The PLL is a critical component for the performance of the whole system because OFDM signals are sensitive to the phase noise of the PLL signal. The spur level is not critical, but it should be below −45 dBc to keep the integrated phase error small. The measured PLL phase noise at 48 GHz is −98 dBc/Hz at 1 MHz offset. The measured PLL bandwidth is 150 kHz, and the tuning range is from 47.2 to 49.6 GHz.

The purpose of the filter is to attenuate both the image at 36 GHz and the VCO feed-through at 48 GHz. A strong feed-through signal would affect the linearity of the RX front-end, because the TX and RX antennas are placed in close proximity. The *Q*-factor of integrated inductors for the 60 GHz range is low (typically 15–20) resulting in high insertion loss and limited selectivity [8]. For a compact design, a lumped element filter type was chosen. The measured insertion loss is 3.3 dB at 60 GHz. The image rejection at 36 GHz is 27.7 dB. The VCO feed through at 48 GHz is attenuated by 12 dB. The filter dimensions are 0.22 × 0.09 mm².

The PA features a three-stage differential cascode topology [3]. A cascode offers a high gain of around 11 dB per stage in IHP technology, and good matching at both input and output. To achieve the required amplification, a three-stage topology was implemented. The PA, as the rest of the chip, is fully differential for a double output power which is combined with a differential antenna. The TX and especially the PA require good on-chip ground for stable operation. To achieve this, the ground connection needs many short bond wires. In addition to this, the PA layout is drawn symmetrically utilizing the ac ground for the differential signal at the symmetry line of the layout. The matching topology between stages is an L–C structure. The inductances were realized as lines in the top metal layer. They were bent in the layout in order to end at the symmetry axis to utilize the ac ground. The modulation scheme used for data transmission is OFDM which is sensitive to non-linear distortion. This means that the PA has to be optimized for high output P1 dB rather than for saturated output power. To achieve a high P1 dB – a class–A PA was chosen. The PA draws 190 mA from a 3.7 V supply.

The TX chip was measured on-board. The TX was first measured with a 100 MHz sine-wave input. The transmitted 60.1 GHz signal was measured with a V-band waveguide antenna with a gain of 22.5 dBi, a power sensor and a power meter. The power at the output of the TX was calculated from the measured received power by subtracting the antenna gain and adding the free-space loss (62 dB at 0.5 m). Figure 2 shows the measured output power for the swept input power. The calculated TX conversion gain after 2.5 dB correction for the cable and balun loss is 33 dB. Saturated output power is 16.2 dBm and P1 dB is 12.6 dBm.

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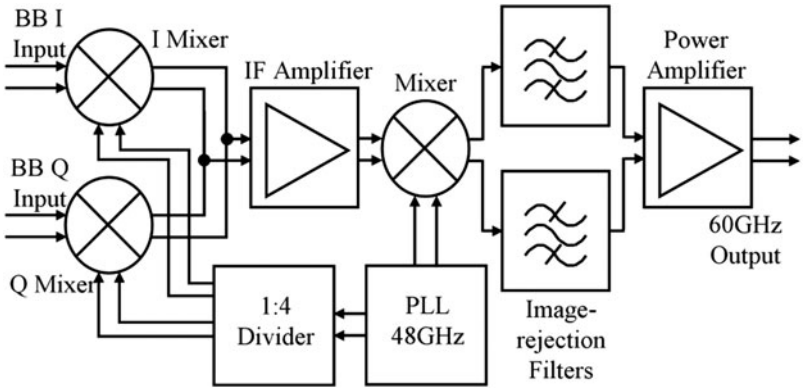

Fig. 1. TX architecture.

The measured phase noise of the sine wave at 1 MHz offset is −97 dBc/Hz. The TX consumes 1300 mW from three different supplies: 3.7, 3.3, and 2.5 V.

IV. 60 GHZ RX

The 60 GHz RX utilizes a sliding-IF architecture. Its building block diagram is shown in Fig. 3. A differential architecture is adopted from antenna to baseband because of its robustness with respect to bond wires and its common-mode rejection ability. The quadrature LO signals for the second down-conversion mixers are generated by a divide-by-four circuit in the PLL chain, which gives perfect IQ signals because both I and Q signals respond only to the rising edge of the 48 GHz VCO output. By contrast, if a divide-by-two circuit were used to generate the quadrature LO signal, a phase rotator would be needed to correct the phase error caused by the non-50% VCO duty cycle. This is because the I and Q signals respond to both the rising and falling edges of the VCO output [1].

The RX front-end consists of a low-noise amplifier (LNA), a mixer, a PLL, and an IF demodulator. The LNA is a three-stage common-emitter amplifier with 18 dB gain and 22 GHz bandwidth. Its main design and implementation issues have been shown in [2]. Minor modifications have been made to the LNA for technology and process migration. However, only the simulated overall noise figure was given in [2] due to the lack of noise measurement. Figure 4 shows the gain circles and noise figure circles for the HBTs used in the first stage for the given biasing condition at 60 GHz. Input tradeoff is made at the solid triangle marker where noise figure increases by 0.2 dB and gain reduces by 0.4 dB. After adding the input matching structure, the noise figure further increases by 0.6 dB due to losses. The second and third stages contribute another 1.3 dB noise figure due to the insufficient gain in the first stage. Thus, the overall noise figure is the sum of NF_{min} (4.5 dB), tradeoff with gain (0.2 dB), input loss (0.6 dB), and later stages (1.3 dB), i.e. 6.6 dB. Old HBT models were used in [2], which gave 0.2 dB higher noise figure. Simulated and measured noise figures are shown in Fig. 5. The measured noise figure is from 6.4 to 7.2 dB at the frequency band of 57–66 GHz, which agrees well with the simulated results. The 60 GHz mixer design is based on [9], where the output and load are re-optimized to match to 12 GHz IF band. Conversion gain is designed to be the same as in [9]. The mixer has not been measured separately because it is designed and integrated in the first shot. Its simulated noise figure is 14 dB, which contributes only slightly to the overall noise performance of the RX due to the high gain LNA.

The 12 GHz demodulator is designed to have a conversion gain of 50 dB with more than 30 dB gain control range. An SPI is introduced for the gain and IQ VGA mismatch control, thereby reducing the number of bond pads. The complete RX analog front-end has a 78 dB conversion gain. The RX consumes 980 mW from two different supplies: 3.3 and 2.5 V.

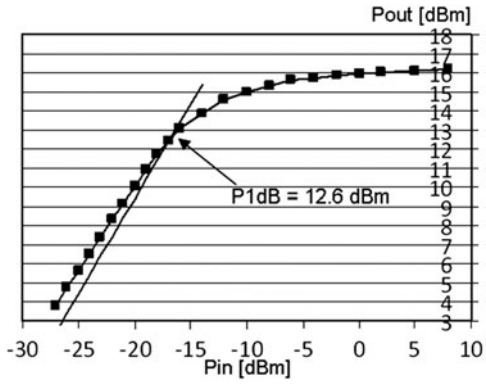

Fig. 2. Output power versus input power sweep of a 100 MHz sine wave signal.

V. PLL SYNTHESIZER

The realization of an RF PLL at frequencies from 58.32 to 64.8 GHz is very challenging, especially for the VCO and the first frequency divider stage. Using a sliding-IF topology as suggested in [6], the PLL frequency is reduced to 80% of

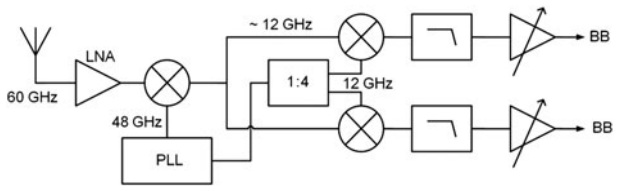

Fig. 3. Simplified 60 GHz sliding IF RX architecture.

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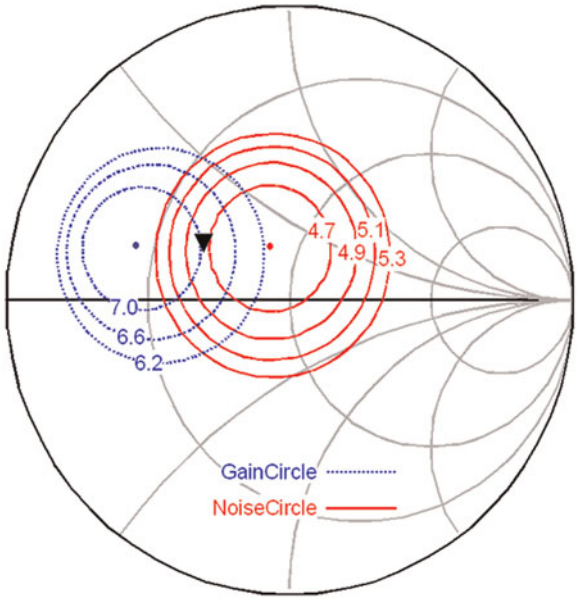

Fig. 4. Gain and noise trade off in the first stage of the LNA.

these values. As a result, the following frequencies must be generated: 46.656, 48.384, 50.112, and 51.84 GHz. If two VCOs selectable by a digital command are used, a VCO tuning range of $2.16 \times 0.8 = 1.728$ GHz plus safety margin is required. The feasibility of such a solution was first shown in [10], where an integrated 48 GHz PLL in SiGe-BiCMOS with 2.4 GHz tuning range has been demonstrated. The PLL, unlike other TX and RX blocks, features both bipolar and CMOS transistors. The VCO and static dividers are realized with bipolar transistors, whereas the PFD and charge pumps feature CMOS transistors. The 48 GHz band PLL is used to down-convert the 60 GHz RF signals to a 12 GHz band. A sliding IF of about 12 GHz is generated from the 48 GHz VCO using a 1:4 frequency divider, which is used for the down-conversion to baseband with an I/Q demodulator. Figure 6 shows the basic PLL architecture suggested in [6]. The VCO output frequency is divided by four to generate quadrature signals at the IF of about 12 GHz. This signal is divided by the programmable divider consisting of a 1:45 bipolar divider and a programmable low-speed CMOS divider. The phase-frequency detector (PFD) compares the 9.6 MHz signal of the divided crystal frequency with the

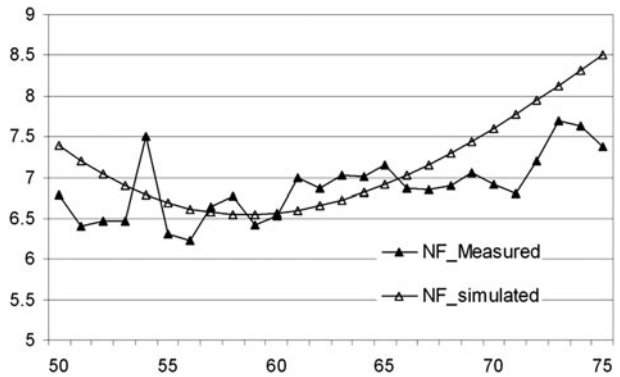

Fig. 5. Measured and simulated noise figure of the 60 GHz LNA.

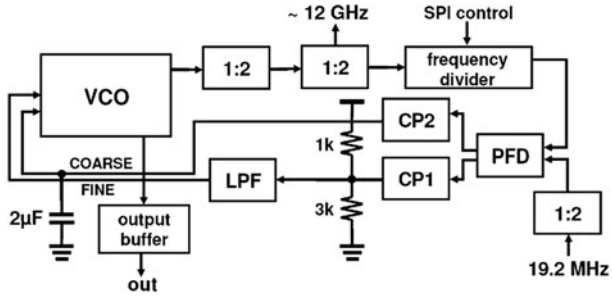

Fig. 6. Schematic of frequency synthesizer.

divided VCO frequency. The PFD output is connected to a high-current charge pump (CP1) for VCO fine tuning and a low-current charge pump (CP2) for coarse tuning. The two parallel tuning loops allow a low phase noise, a low level of reference spurs, and a large tuning range to be achieved simultaneously. The voltage divider at the output of CP1 keeps the dc voltage at the VCO fine tuning input roughly constant [11], which makes the loop bandwidth fairly independent of device parameter variations with process, supply voltage, and temperature (PVT). The total tuning range is defined by the slow coarse tuning loop, in which the noise of CP2 is almost eliminated by a large external capacitor. In this transceiver, a 48 GHz PLL as described in [10] containing only one VCO is used. An IEEE compatible PLL using an array of two VCOs as proposed in [6] has been tested successfully and will be included in a future design. The measured PLL phase noise at 1 MHz offset was −98 dBc/Hz [10]. This corresponds to an integrated rms phase error after baseband filtering below 1.5°, which is more than sufficient for 16-QAM OFDM transmission [6].

VI. RF MODULE WITH INTEGRATED ANTENNA

Figure 7 shows the RF module of the transceiver [7]. A thin film of Rogers 3003 with a thickness of 125 µm is used as the substrate. In order to make the board mechanically stable and reliable, an FR4 Epoxy layer is laminated beneath

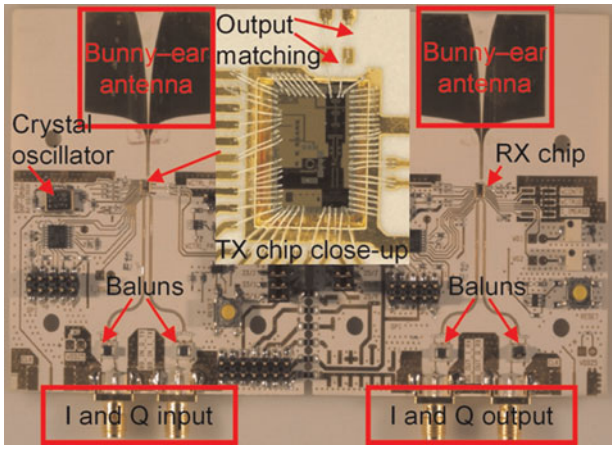

Fig. 7. TX and RX RF module with integrated antenna.

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the Rogers 3003. The chips are mounted in a metalized cavity with a ground ring (see Fig. 7). The depth of the cavity equals the chip's thickness of 250 μm. In this way, one can have the shortest distance between the chips' ground and the module's ground, so that the inductance introduced by the bond wire is reduced. Each chip has around 30 ground pads to further improve the interconnections between the on-chip and on-board grounds.

The transceiver chips have 60 GHz differential input/output, which requires a differential antenna. Otherwise, a balun would be required. Moreover, this antenna needs to cover the full 60 GHz frequency band with acceptable gain. A Vivaldi antenna is a good candidate due to its theoretically unlimited operating frequency range with almost constant beamwidth. However, in practice the bandwidth is limited by the transition from the feeding microstrip transmission line to the slot line of the antenna. A Bunny-Ear Antenna (BEA) is a derivative of the Vivaldi antenna which can offer a transition from the differential microstrip transmission line to the antenna slot line, while maintaining the wideband radiation characteristics. Therefore, a BEA is adopted in both TX and RX modules. Bond wires are used to interconnect the transceiver chips and the modules. However, at 60 GHz this introduces considerable inductances and causes a mismatch. In order to overcome the mismatches caused by the bond-wire inductances, a T-type L–C–L compensation structure, realized by double bonding and a metal pad, is employed as the matching scheme (see Fig. 7). In addition, the FR4 under the antenna would cause excessive loss, so the FR4 below the antenna was removed. Most of the current concentrates along the slot edges of the antenna where the electric field is the strongest, so that only a small hole in the size of 29 mm × 10 mm around the slot area is cut out. With this hole the radiation performance is significantly improved while the mechanical stability of the board is hardly affected. This antenna was characterized in [12]. It has a measured gain of 12–10 dBi in the frequency band of 57–65 GHz.

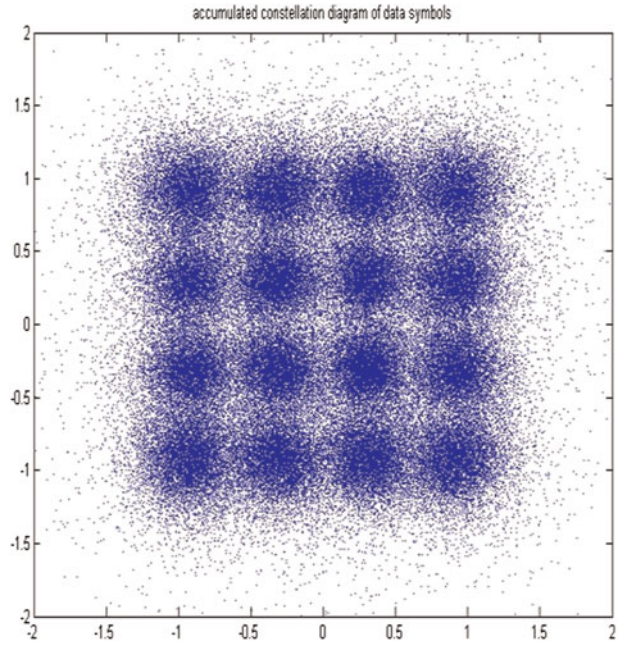

Fig. 8. Constellation diagram for 16QAM, three-fourth coding, OFDM signal with 3.6 Gbit/s data rate over 15 m distance.

Table 1. Comparison of 60 GHz analog front-ends.

Ref.	Technology	Topology	Power dissipation (mW)	Chip area ()(mm²)	Antenna gain (dBi)	Data rate (Gbit/s)	Max distance (m)	Equivalent Max. distance (m)
This work	SiGe 0.25 μm	Sliding IF	TX: 1300, RX: 980	TX: 3.15, RX: 3.36	11.5	3.6 (raw 4.8)	15	15
[13]	SiGe 0.13 μm	Sliding IF	TX: 822, RX: 547	TX 6.4, RX: 5.6	8	2	3.5	7.8
[14]	CMOS 65 nm	ZIF	TX&RX, 374	TX and RX: 1.04	25	3.5 (raw)	2	0.09
[15]	CMOS 90 nm	ZIF	TX&RX, 300	TX and RX: 6.88	25	4 (raw)	1	0.045
[16]	CMOS 90 nm	ZIF	TX&RX, 200	TX and RX: 6.25	No antenna	3.5 (raw)	Cable connection	Cable connection
[16]	CMOS 90 nm	Beamforming 4 elements	N.A.	TX: 17.5, RX: 17.5	No antenna	15 (raw)	Cable connection	Cable connection
[17]	SiGe 0.13 μm	Beamforming 16 elements	TX: 6200	TX: 43.8	7 + 12 from beamforming	5.6	N.A.	N.A.

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VII. OFDM LINK DEMONSTRATION

The analog front-end (AFE) was measured for data transmission with an OFDM signal. The used PHY parameters of the OFDM signal are similar to the IEEE 802.15.3c standard. I and Q input signals have 850 MHz bandwidth each. The TX and RX were measured in a loop: Matlab–Tektronix arbitrary waveform generator (AWG)–TX–RX–Agilent oscilloscope–Matlab. Matlab gives OFDM frames information to the AWG, which generates the frames and feeds them to the TX. The received signal is fed from the RX to the oscilloscope, and the sampled signal is analyzed by Matlab. Data transmission of 3.6 Gbit/s (4.8 Gbit/s raw – i.e. without coding) was demonstrated over 15 m with zero FER. The FER was measured for 2000 frames. The OFDM signal used 16QAM modulation scheme with three-fourth coding. SNR measured over 15 m was 10.2 dB. The measured constellation diagram is shown in Fig. 8.

VIII. CONCLUSION

Table 1 shows a comparison of the TX and RX presented in this paper with the-state-of-the-art 60 GHz TXs and RXs. Four reported systems have one antenna [13–16], and two systems implement phase-array antenna with beamforming [16, 17]. Beamforming chips are much larger and consume much more power than those w/o beamforming (see table for [17]). As such, they belong to a different class and should not be directly compared.

The TX and RX presented in this paper are the best reported AFE in SiGe without beamforming regarding both the data rate and transmission distance. Since the maximum distance of communication depends on the gain of the implemented antennas, the last column in Table 1 presents equivalent maximum distance calculated for TX and RX antenna gain of 11.5 dBi, which was used in our AFE.

The comparison presented in Table 1 shows that SiGe is an advantageous technology for 60 GHz AFEs compared with CMOS. This is primarily due to higher TX/PA output power, while the RX NF of LNAs in SiGe and CMOS is comparable. CMOS is, however, better for low-power design.

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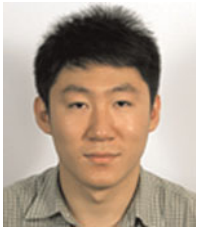

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