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RESEARCH PAPER

Optimization of a 61.44 GHz BiCMOS HBT integrated PLL for ultra-fast settling time

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The design of a 61.44 GHz integrated Phase-locked loop (PLL) on a 180 GHz BiCMOS technology is presented. The PLL was optimized for a very fast settling time of 4 μs as required by the system specifications. Because the receiver is using a carrier recovery circuit that can follow the slow changes of the carrier such as phase noise, the sensitivity of the bit error rate to phase noise at the receiver end is very low. As a result, to achieve the required dynamic behavior, the phase noise performance could be sacrificed and the loop bandwidth was increased until the needed settling time was achieved, while taking the suppression of the reference spurs into consideration. Capacitor multiplication was used to enable the integration of the loop filter (LF) on chip and the effect of the capacitor multiplier on the total PLL phase noise performance was quantified and evaluated. In addition, a very close matching between the measured and simulated phase noise of the system was achieved. The PLL consumes a power of 200 mW from 2 and 3 V supply voltages, while delivering a differential output power of −7 dBm, sufficient to drive the following I/Q modulator without additional amplification.

Keywords: Pll, HBT, Phase noise, 60GHZ

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I. INTRODUCTION

The growing demand for higher data rates in wireless transmission motivates the interest of the engineering research community in multi-Gbps wireless transceivers. The wide bandwidth required for such high data rates is currently available at 60 GHz, where up to 7 GHz of unlicensed band can be used. In this context, the design of 60 GHz building blocks suitable for integration in systems-on-chip is subject of research. One specific challenge related to the implementation of the PLL is the integration of loop filters (LFs). In [1–4] several millimeter-wave fully integrated PLLs were presented. These PLLs use on chip Metal-insulator-metal (MIM) or Metal-oxide-semiconductor (MOS) capacitors for the LF and a small loop bandwidth to optimize phase noise while sacrificing the system dynamic behavior. In this work, we discuss the use of capacitor multipliers for the integration of the PLL. In contrast to the other PLLs, the system was optimized for very fast settling time. Additionally, we investigate the impact of the capacitor multiplier on the phase noise of the PLL.

Figure 1 shows the system-level schematic of the transmitter, which relies on the PLL presented in this work. The direct up-conversion architecture was adopted. The transmitter consists of an Field programmable gate array (FPGA) that feeds two independent data streams into the in-phase (I) and quadrature (Q) paths of the analog frontend through an FPGA interfacing circuit. The I and Q data are up-converted to the 60 GHz band using an I/Q modulator and then fed into a wide-band power amplifier, which feeds the signal to the antenna. Since the target system is a transceiver operating in a time-division duplexing mode, the transmitter will continuously have to be switched on and off. In order to sustain the required effective data rate in switching mode, the PLL should be able to settle in a very fast time; a settling time of 4 μs was specified to be sufficient from the system requirements. In this context, the loop bandwidth is a crucial system parameter as it affects both settling time and phase noise, and defines the trade-off between them. But, because the receiver is using a carrier recovery circuit that can follow the slow changes in carrier such as phase noise, the phase noise performance could be sacrificed and the loop bandwidth was increased until the required settling time was achieved.

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II. SYSTEM ARCHITECTURE AND SIMULATION

The integer-N synthesizer architecture, as shown in Fig. 2, was adopted due to its lower risk and suitability for the required application. A common collector Colpitts voltage controlled oscillator (VCO) was used in a PLL system to generate the 61.44 GHz carrier. The VCO was followed by an output splitter that feeds the output of the VCO into two paths; one was used for the frequency divider and the other was used to drive the I/Q modulator. The frequency divider divides the 61.44 GHz signal to 60 MHz (the frequency of the crystal oscillator). The output of the divider was then fed into a conventional tri-state phase frequency detector (PFD), optimized to minimize the dead zone. The output of the PFD was used to

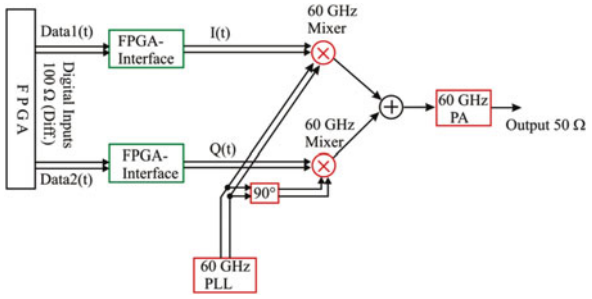

Fig. 1. Transmitter architecture.

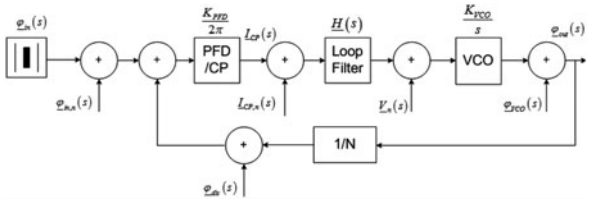

Fig. 2. Synthesizer linear model with noise sources.

drive a highly matched charge pump (CP), which, with such matching, minimizes the power of the spurs generated around the carrier and reduces the noise generated by the CP transistors. Finally, the output of the CP was connected to a second-order integrated LF. The approach of capacitor multiplying was used to enable the integration of the LF on the same chip. System simulations were used to optimize the filter parameters and resolve the trade-off between the loop dynamics, stability, spur power, and phase noise performance. Figure 3 shows the trade-off between loop bandwidth, phase noise, and settling time for three different loop bandwidths.

A) Dynamic behavior

The following parameters of the different blocks of the PLL were used for system simulations: the PFD/CP gain $(K_{PFD}) = I_{CP} = 230\ \mu A$, the VCO gain $(K_{VCO}) = 2 \times \pi \times 5$ Grad/V, the division ratio $(N) = 1024$, and a second-order LF. The system was modeled using Verilog-A and simulated for its locking dynamics; the LF parameters were chosen to give the optimum loop bandwidth and settling time. The loop bandwidth was chosen to be 1.6 MHz to enable the PLL to be as fast as required.

B) Phase noise simulations

The model shown in Fig. 2 can be used to predict the PLL's phase noise performance. The different transfer functions of the different noise sources can be derived, as shown in Table 1, and then the noise spectrum of each block can be simulated and shaped to the output using its own transfer function, as described in [5]. In an integer-N synthesizer, the noise of the PFD/CP combination is the dominant part [6]. In this case, due to the integration of the LF, the LF also highly contributes to the PLL phase noise. The noise of the PFD/CP, VCO, and the LF were simulated and shaped to the output. The result is shown in Fig. 4; the measured spectrum closely matches its simulation.

In order to investigate the effect of the capacitor multiplier on the phase noise of the system, the loop was simulated assuming a conventional filter with no capacitor multiplication and the simulation results were compared. The effect of using the capacitor multiplier has shown a degradation of around 5 dB on the phase noise inside the loop bandwidth, as shown in Fig. 4.

Table 1. Noise and loop transfer functions [5].

Forward gain	$\underline{G}_{forward}(s) = \frac{K_{PFD}}{2\pi} * \underline{H}(s) * \frac{2\pi K_{VCO}}{s}$
Reverse gain	$\underline{G}_{reverse}(s) = \frac{1}{N}$
Loop gain	$\underline{G}_{loop}(s) = \underline{G}_{forward}(s) * \underline{G}_{reverse}(s)$
VCO noise	$\frac{\underline{\varphi}_{out}(s)}{\underline{\varphi}_{vco}(s)} = \frac{N}{N + \underline{G}_{forward}(s)}$
Divider noise	$\frac{\underline{\varphi}_{out}(s)}{\underline{\varphi}_{div}(s)} = -\frac{\underline{G}_{forward}(s)}{1 + \underline{G}_{loop}(s)}$
CP noise	$\frac{\underline{\varphi}_{out}(s)}{\underline{I}_{CP,n}(s)} = \frac{2\pi}{K_{PFD}} \frac{\underline{G}_{forward}(s)}{1 + \underline{G}_{loop}(s)}$
LF noise	$\frac{\underline{\varphi}_{out}(s)}{\underline{V}_{n}(s)} = \frac{2\pi}{K_{PFD}} * \frac{1}{\underline{H}(s)} * \frac{\underline{G}_{forward}(s)}{1 + \underline{G}_{loop}(s)}$
Reference oscillator	$\frac{\underline{\varphi}_{out}(s)}{\underline{\varphi}_{in,n}(s)} = \frac{\underline{G}_{forward}(s)}{1 + \underline{G}_{loop}(s)}$

III. CIRCUIT DESIGN

A) VCO

The common collector Colpitts oscillator is well known for its good phase noise performance at high frequencies. As a result, it was adopted for this system. Design and characterization of this VCO were presented in [7].

B) Divider

The divider is used to generate a 60 MHz signal, which is suitable for comparison with the 60 MHz crystal oscillator output,

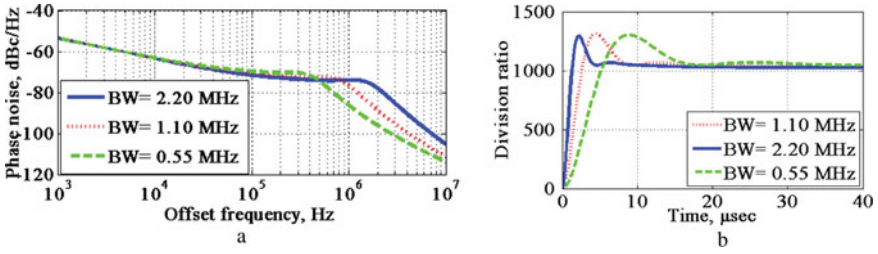

Fig. 3. Loop bandwidth versus (a) phase noise and (b) settling time.

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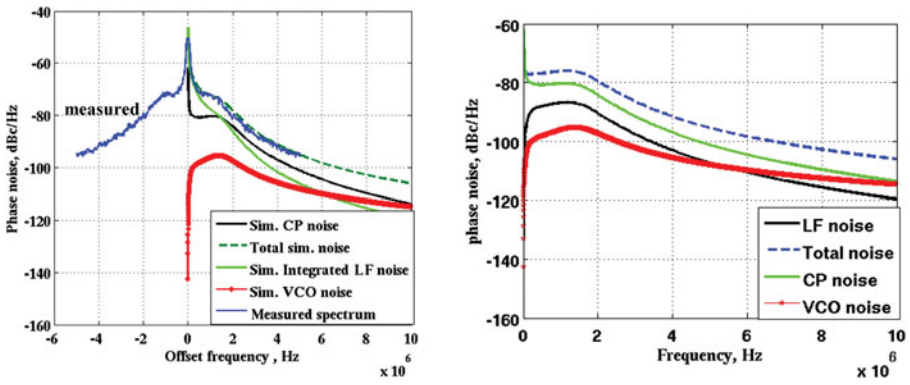

Fig. 4. SSB phase noise (a) with capacitor multiplier measured versus simulated and (b) without capacitor multiplier simulated.

from the 61.44 GHz VCO output. The division ratio of 1024 was implemented by cascading ten divide-by-two static divider stages. The split-load architecture was adopted for the latch used in the static dividers [8]. The bias current and the resistors ratio were scaled to optimize the self-oscillation frequency of each divider stage. By doing this, each stage requires minimum input power and the output power of the previous stage can be scaled down, which finally results in lower power consumption. The output spectrum of the 1024 divider is shown in Fig. 5.

C) Phase frequency detector

A conventional tri-state PFD, which uses two edge-triggered flip flops and an AND gate with a delay in the reset path to minimize the dead zone of the PFD, was used [6].

D) Charge pump

The role of the CP is to convert the phase difference between the high-quality crystal oscillator signal and the output of the divider into a linearly proportional average current, which is injected into the LF and corrects for phase and frequency differences between the reference crystal and the divider output. The phase noise and the power in the spurs around the carrier directly benefit from improvements in the matching between the up and down currents of the CP [6]. The highly matched CP architecture, shown in Fig. 6, was adopted. This architecture uses a feedback structure to minimize the effect of channel length modulation on the mismatch between the up and down currents.

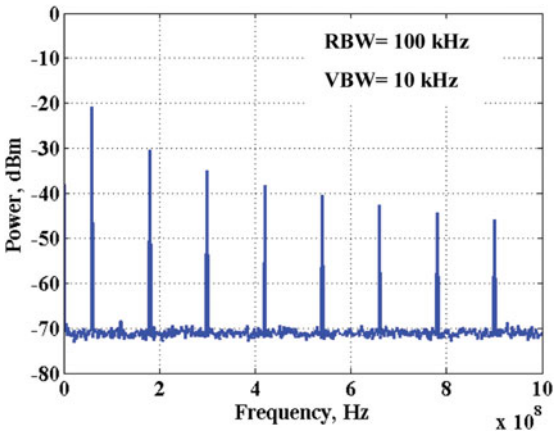

Fig. 5. The output spectrum of the 1024 divider at 61.44 GHz input frequency (60 MHz output).

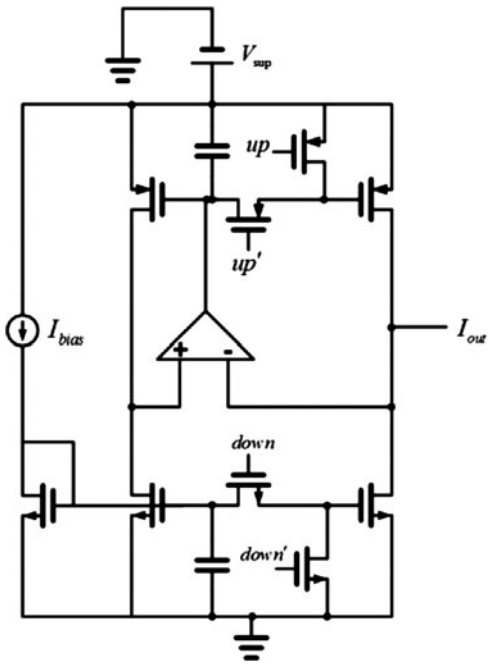

Fig. 6. Highly matched CP architecture [6].

E) Loop filter

The LF converts the output current of the CP into a voltage, which drives the loop into locking. The second-order LF

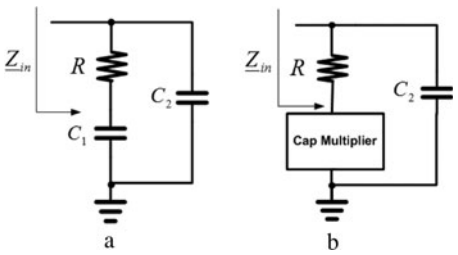

Fig. 7. Second-order LF (a) without and (b) with capacitor multiplier.

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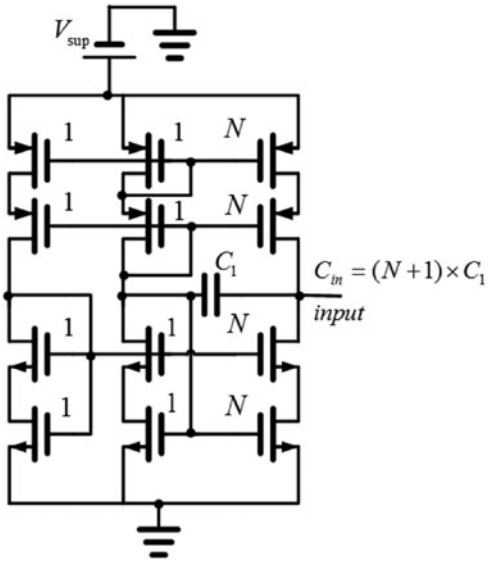

Fig. 8. Capacitor multiplier [9].

architecture is shown in Fig. 7. The large capacitance of the filter was generated by capacitor multipliers in order to enable its integration on chip. The capacitor multiplier in [9], as shown in Fig. 8, was adopted for that purpose. In Fig. 9, a comparison between the input impedance of the conventional LF versus the input impedance of the LF using the capacitor multiplier is shown. The synthesizer loop was simulated using the conventional loop filter (LF) and the LF using the capacitor multiplier: the dynamic behavior shown in Fig. 10 was obtained. The two LFs show very similar performance and a fast settling time of 4 μs.

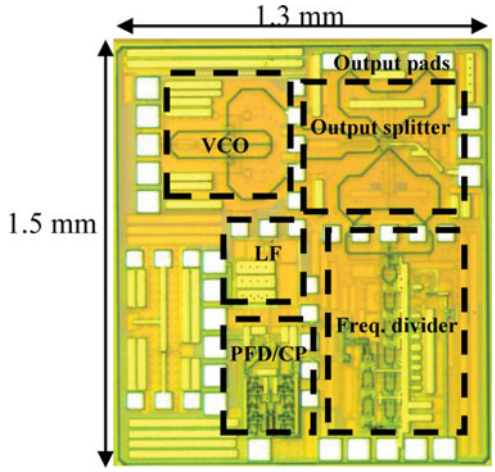

Fig. 11. Synthesizer chip photo.

F) Output splitter

The output of the VCO is fed into the input of the output splitter and two output signals are generated. One is used to drive the divider and should supply the divider with the required power for the appropriate operation. A matching network was designed to guarantee such power level. The other output of the splitter is matched to supply the mixer with −7 dBm of differential power, which is required for its optimal functionality.

IV. CIRCUIT CHARACTERIZATION

The layout of the synthesizer was designed to enable the testing of the individual high-frequency blocks used in wafer

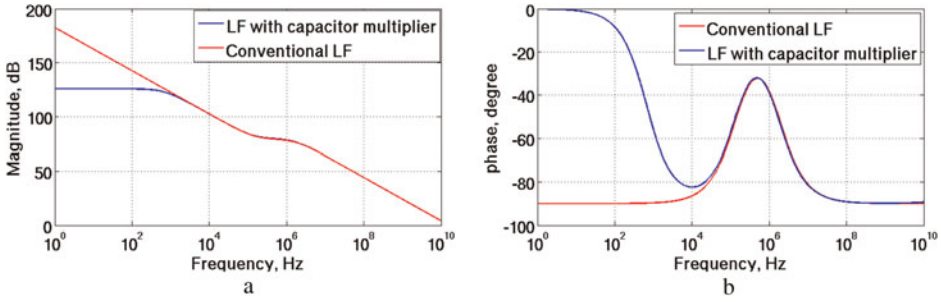

Fig. 9. Simulated impedance of the conventional LF versus LF using capacitor multiplier: (a) magnitude response and (b) phase response.

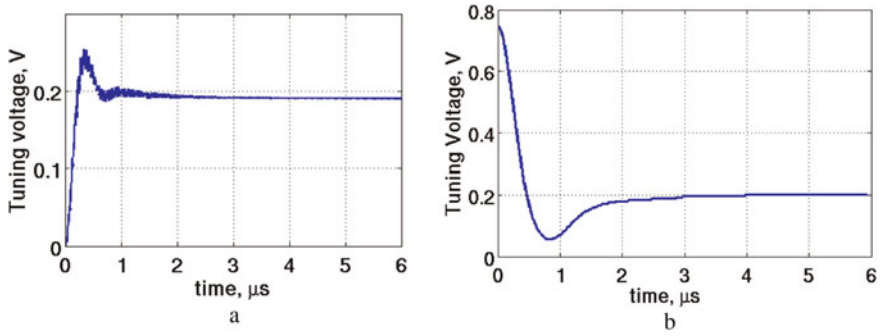

Fig. 10. Simulated dynamic behavior: (a) conventional LF and (b) LF with capacitor multiplier.

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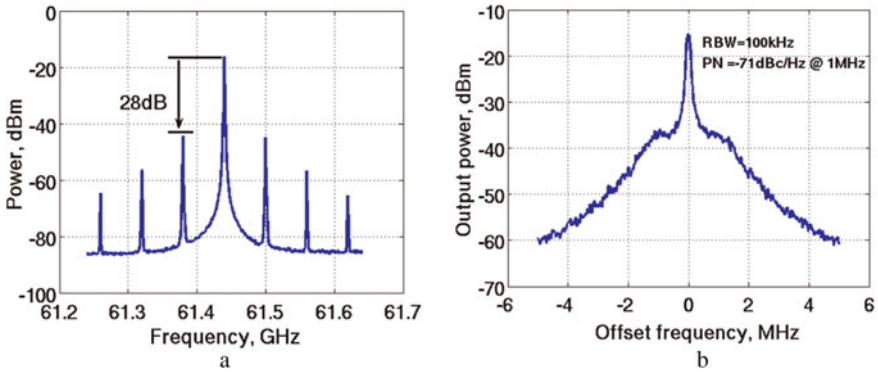

Fig. 12. Measured output spectrum: (a) spurs and (b) phase noise.

Table 2. Comparison with state-of-the-art synthesizers.

Technology	Fund. freq./ GHz	*PN* at 1 MHz dBc/Hz	Loop *BW*/kHz	Ref. freq./MHz	DC power/mW	*FOM*/ at 1 MHz dBc/Hz	Reference
0.25 μm BiCMOS	65 (fix.)	−82	200	60	650	−128	[1]
130 nm CMOS	46 (fix.)	−72	500	60	57	−123	[2]
90 nm CMOS	61 (fix.)	−80	900	60	78	−141	[3]
0.25 μm BiCMOS	50–53 (var.)	−81	1000	262	400	−127	[4]
0.25 μm BICMOS	61.44 (fix.)	−71	1600	60	200	−131	This work

measurement. Figure 11 shows a photo of the fabricated IC. For testing the closed-loop system, a printed circuit board (PCB) was designed to generate the DC bias voltages and currents for the synthesizer; the chip was wire-bonded. The output of the synthesizer was measured using an on-wafer probe, which also helped to provide one of the outputs with 50 Ω termination. The measured spectrum is shown in Fig. 12.

In Table 2, a comparison with state-of-the-art PLLs is shown. The table shows that the loop bandwidth used in this work is much larger than in other presented PLLs. This is the controlled result of a design choice dictated by the transmitter specification: the loop bandwidth was increased to achieve required settling time, taking into consideration the low sensitivity of the bit error rate at the receiver end to phase noise, due to using a carrier recovery circuit. This is the result of a trade-off involving phase noise, loop bandwidth and settling time, presented and discussed above. It was also predicted by the system simulations. For a fair comparison between different designs, the loop noise can be normalized by the division ratio (N) as this linearly amplifies the noise to the output. With this assumption, a new figure of merit (FOM) can be defined by referring all PLLs to a loop bandwidth of 1 MHz assuming roll-off behavior of 20 dB/decade for the loop; this is an upper boundary performance as 20 dB/decade is the minimum slop possible. The FOM allows the comparison of different loops with different bandwidths. The *FOM* is defined as:

$$FOM = PN - 20\log N + 20\log\frac{f_{offset}}{f_{BW}}, \quad f_{offset} > f_{BW}$$

$$FOM = PN - 20\log N, \quad f_{offset} \le f_{BW},$$

where f_{offset} is the offset frequency at which phase noise is calculated, *PN* is the phase noise at the given offset frequency and f_{BW} is the loop bandwidth.

The use of the PLL was demonstrated successfully by including it in the system and transmitting a BPSK data stream at a rate of 3.75 Gbps and receiving it error free.

V. CONCLUSION

The design of a 61.44 GHz fully integrated PLL that uses the approach of capacitor multiplying for the integration of the LF was presented. The expected degradation of the phase noise performance due to the capacitor multiplier compared to MIM capacitors was simulated: the phase noise system simulations have shown very close matching with the measured spectrum. The PLL was optimized for a very fast settling time of 4 μs, by setting the loop bandwidth at 1.6 MHz. The measured phase noise at 1 MHz offset frequency is −71 dBc/Hz. In case better phase noise is required for higher-end applications, an improvement of around 5 dB can be achieved by replacing the capacitor multiplier with MIM capacitors at the cost of more LF area. In addition, the loop bandwidth can be decreased, at expenses of system dynamics.

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