Driving Semiconductor Innovation: Moore's Law at Fairchild and Intel

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Gordon Moore designed Moore's Law as a multifunctional tool to drive process and product innovation, sell Fairchild's and Intel's microchips, and outcompete other semiconductor firms. Because Intel's ability to stay on Moore's Law depended upon other corporations developing materials and manufacturing equipment for exponential scaling, Moore and his closest associates heavily promoted Moore's Law in the microelectronics community. They also established the national and international technology roadmaps for semiconductors in order to set the direction and cadence of innovation in microelectronics at the national and, later, global scales. Moore's and his successors' relentless pursuit of Moore's Law and their deft management of the roadmaps significantly reinforced Intel's competitiveness and helped it to dominate semiconductor technology and industry until the mid-2010s.

Introduction

"Moore's Law," the cadence at which integrated circuit complexity increases over time, is widely acknowledged as being central to innovation in semiconductors and all industrial sectors depending upon microchips. Integrated circuits that consisted of a few transistors in

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1961 had up to 1.5 trillion transistors in 2019. This extraordinary increase, and the concomitant drop in the cost of transistors, thoroughly transformed old industries and led to the formation of new industrial sectors. It was also essential for the digitalization of the human-built world. However, the exact nature and social function of Moore's Law are a source of significant disagreements. Some see it as an example of technological determinism, the idea whereby technologies evolve according to their own inner logic and transform societies as result.[1] Others view it as a "deliberate human creation," a construct exploiting the economics of microchip manufacturing.[2] For some historians, it was a social fact resting on social conventions, like marriage.[3] For others, it was a self-fulfilling prophecy, the prediction of increased microchip complexity leading to the manufacture of more and more complex integrated circuits.[4] It has also been argued that Moore's Law changed over time. According to an economic analyst, it started as a self-reinforcing expectations mechanism before becoming a "formally structured process for organizing technological change" in the 1990s.[5]

This article proposes a different interpretation of Moore's Law. It argues that Moore's Law was an observation and a managerial tool developed, employed, and regularly adapted to new circumstances by Gordon Moore, the cofounder of Fairchild Semiconductor and Intel Corporation, and his associates in the microelectronics business. Moore's Law had many functions. It was a technology planning tool orienting microelectronics innovation and setting its pace. It was a marketing and sales tool used to convince potential customers to buy microchips. When it became associated with a new institution, the National Technology Roadmap, it evolved into a tool of innovation governance. However, Moore's Law was also a competitive instrument employed by Moore and his successors at Intel to weaken and displace other corporations active in the semiconductor industry.

In this respect, it might be helpful to distinguish Moore's Law from what can be called "Moore's band." Moore's Law was the rule devised and employed by Moore, whereby the number of components per integrated circuit doubled over a period ranging from every year to every two years (Moore's formulation of the law changed several times). In contrast, Moore's band was formed by all the individual trajectories of semiconductor firms in terms of growing chip complexity. Semiconductor corporations designed and produced integrated circuits according to different tempos. Some were slower, others faster in multiplying

1. Ceruzzi, "Moore's Law and Technological Determinism."
2. Thackray, Brock, and Jones, *Moore's Law*; Brock, *Understanding Moore's Law*.
3. Mody, *The Long Arm of Moore's Law*.
4. Schaller, "Moore's Law."
5. Flamm, "Moore's Law and the Economics of Semiconductor Price Trends."

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the number of transistors per integrated circuit. The sum total of these trajectories was Moore's band. It had a general direction, toward ever greater integration. It also had a slope that changed over time. Moore conceived Moore's Law, in part, as a tool that would allow Fairchild and then Intel to stay on top of Moore's band and reap the economic benefits derived from this position over the long term.

This article examines the ways in which Moore crafted his law in the early and mid-1960s and revised and utilized it in the following decades. It investigates how and when Moore's Law was adopted by other firms, both nationally and internationally. Another topic addressed in this article is the law's impact on Moore's band and Intel's position within it. To explore these issues, the article relies on an examination of the personal papers of Gordon Moore. It also relies on interviews with Moore's colleagues at Fairchild and Intel and executives heading competing firms and organizations, notably in Japan. It contends that Moore's Law was deeply tied to the careers of its creator, Gordon Moore, and other Intel executives such as Robert Noyce, Andrew Grove, Craig Barrett, Leslie Vadasz, David House, and Paolo Gargini. These men transformed and refined Moore's Law over several decades. They acted as its main champions. They also coupled it with another managerial tool-cum-institution—the technology roadmap—to govern semiconductor innovation at the national and, later, international scale.

Before Moore's law acquired its current name, it was known as "Moore's plot." In the mid-1960s, Gordon Moore, who directed research at Fairchild Semiconductor, devised his plot as a tool guiding process and product development and as a marketing tool aimed at convincing potential customers of the technological and economic potential of integrated circuits. Moore also used his plot to keep Fairchild on top of Moore's band. In 1968, Moore cofounded Intel Corporation. At Intel, Moore and his associates heavily promoted Moore's plot in the electronics community. This promotional campaign convinced many in the industry that rapid growth in chip complexity was a long-term trend. As a result, Moore's plot became increasingly referred to as "Moore's Law" in the late 1970s and early 1980s, but rare were the firms, aside from Intel, that used it as a technology planning tool at the time.

The semiconductor wars of the 1980s transformed Moore's Law and Moore's use of it. Employing another metric, the quadrupling of memory capacity every three years, Japanese semiconductor manufacturers established themselves as major players in worldwide markets for integrated circuits. Moving to the top of Moore's band, they outcompeted Intel and other U.S. manufacturers. In order to regain Intel's former leadership, Moore accelerated the speed at which his firm increased chip complexity. Moore and his Intel colleagues also implemented Moore's Law in a much more regimented fashion. In collaboration with

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the executives of other major microelectronics firms, they established cooperative research organizations, such as Sematech, that employed Moore's Law and technology roadmaps as their primary planning tools.

In 1992, Moore further institutionalized Moore's Law by putting it at the very center of the National Technology Roadmap for Semiconductors, a structure of innovation governance for the entire American microelectronics industry. Moore and his successors at Intel used the national roadmap to orient federal investments in semiconductor technology and guide the research and development activities of universities, national laboratories, and materials and equipment suppliers. In 1998, they expanded the roadmap's membership to foreign corporations to access their technological and financial resources. As a result, Moore's Law became the main technology planning tool across the global semiconductor industry for much of the following decade.

Crafting Moore's Plot

Gordon Moore was relatively new to semiconductor technology when he devised Moore's plot over several years in the early to mid-1960s. After earning a PhD in chemistry at the California Institute of Technology (Caltech), he joined Shockley Semiconductor Laboratory, Silicon Valley's first semiconductor start-up, in 1956. Rebelling against William Shockley, Shockley Semiconductor's founder, he established Fairchild Semiconductor with Robert Noyce and six other scientists and engineers the following year. At Fairchild, Moore quickly established himself as the firm's technical leader, becoming the head of its research laboratory. Under his leadership, the laboratory originated fundamental innovations such as the planar process and the planar integrated circuit.[6]

In 1963, Moore wrote a seminal chapter on integrated circuit technology and the economics of semiconductor manufacturing for a volume on microelectronics edited by Edward Keonjian. This book reviewed different approaches to electronics miniaturization, including hybrid circuits, thin-film circuits, and functional devices. In his contribution to the volume, Moore aimed at convincing others in the industry that integrated circuits offered the cheapest avenue to make electronic devices and systems smaller. This was a novel argument at the time, as the general consensus among engineers was that miniaturization added to the cost of electronics. To make the case that microcircuits would make electronics inexpensive, Moore contended that the

6. On the history of Fairchild, see Berlin, *The Man behind the Microchip*; Lécuyer, *Making Silicon Valley*; Lécuyer and Brock, *Makers of the Microchip*; Thackray, Brock, and Jones, *Moore's Law*.

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cost per electronic function would decrease as integrated circuit complexity increased. Because of this dynamic relationship, Moore predicted that "the amount of circuit function to be put economically in a single functional block will increase rapidly. This in turn will further contribute to cost and reliability improvements in systems."[7]

To support this argument, Moore made a detailed analysis of the economics of semiconductor production. He noted that the fabrication cost of an integrated circuit was highly dependent on yield, the percentage of salable microchips coming out of the manufacturing line. In turn, Moore argued, yield depended on the size of the die, the piece of silicon crystal on which one patterned a single integrated circuit. The smaller the die, the likelier it was that it would not be impaired by "bad spots" such as minute defects in the dioxide layer protecting the silicon crystal. By decreasing the size of the die through process improvements, one could reduce the incidence of these "bad spots" and, therefore, increase yield and lower cost. "As the complexity is increased," Moore argued,

> microcircuits are favored more and more strongly, until one reaches the point where the yield, because of the complexity, falls below a production-worthy value. The point at which this occurs will push increasingly in the direction of increased complexity. As the technology advances, the size of circuit function that is practical to integrate will increase rapidly. The problems associated with yield and area will be better understood and the yield improvements which will result will allow the use of larger areas. More circuitry will be possible in a given area through the use of finer scale structures.[8]

In short, integrated circuits were poised to become dramatically cheaper than equivalent circuits made of discrete components, and the reduction in their cost would be dictated by evolving processing capabilities.

Making the most of this insight, starting in 1963, Moore reoriented his laboratory toward integrated circuit technology. He requested that scientists and engineers working in his laboratory design and fabricate increasingly complex integrated circuits. He also funded this activity very heavily. Harry Sello, the head of the laboratory's process and materials section, later remembered that Moore would regularly ask him and other researchers to develop integrated circuits with more and more transistors. As Sello put it, Moore "pushed us to go back to the lab, reduce the imperfections in silicon crystals, and improve the manufacturing process. This drove us into better production capability."[9] As a result,

7. Moore, "Semiconductor Integrated Circuits"; Thackray, Brock, and Jones, *Moore's Law*.

8. Moore, "Semiconductor Integrated Circuits."

9. Sello, interview.

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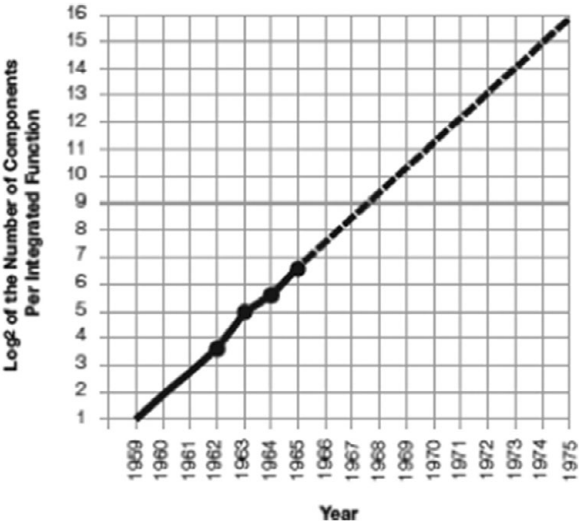

Figure 1 Moore's plot, 1965.

Source: Gordon Moore, "Cramming More Components onto Integrated Circuits," *Electronics*, April 19, 1965, 116. @2006 IEEE, reprinted with permission.

Fairchild introduced increasingly complex integrated circuits to the market. By 1965, its most advanced chip had fifty transistors.[10]

However, the firm's integrated circuits did not sell well. Electronics engineers were hesitant to employ microchips in their devices and systems. To persuade engineers to adopt the new technology, Moore gave several talks on the future of integrated circuits at professional meetings in 1964. The following year, he published an article on microchips, titled "Cramming More Components onto Integrated Circuits," in *Electronics*, a trade magazine. In this piece, he outlined the argument about the economics of microchip manufacturing he had presented in Keonjian's volume two years earlier. However, in a departure from his earlier piece, he quantified the complexity increase he had envisioned in 1963. He produced a plot, later known as "Moore's plot," showing the number of components per microchip as a function of time (figure 1). To create this plot, Moore used the component counts of the most complex chips Fairchild had introduced to the market over the previous three years. As he created the plot, Moore realized, for the first time, that since the initiation of integrated circuit technology, the number of components in Fairchild's chips had doubled every year.[11]

10. Sello, interview.

11. Moore, "Cramming More Components." On the context of Moore's 1965 article, see Gibbs, "Gordon E. Moore"; Brock, *Understanding Moore's Law*; Thackray, Brock, and Jones, *Moore's Law*; and Lécuyer, *Making Silicon Valley*.

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With this plot, Moore went further than quantifying his success as a research manager. He made an important addition to the graph by inserting a dotted line showing that the annual doubling of components per chip would continue for another ten years. This was a bold prediction. It was also a masterstroke of marketing. To persuade electronics engineers to employ microchips in their designs, Moore argued that circuit complexity would increase exponentially and that the most advanced integrated circuits would have 65,000 transistors in 1975. This exponential increase, Moore contended, would revolutionize electronics. It would dramatically reduce the cost of electronic functions. It would also make new types of electronic devices such as "home computers" possible. Furthermore, Moore asserted that there were no fundamental physical limitations to the trend toward greater complexity. Only good engineering was needed. "The future of integrated electronics," Moore asserted, "is the future of electronics itself. The advantage of integration will bring about a proliferation of electronics, pushing this science into many new areas."[12]

Moore's article was widely read. It soon became part of a debate on the future of miniaturization. On the one hand, research managers at Bell Labs openly doubted that microchips would significantly lower the cost of electronic systems. The more complex the integrated circuit, they argued, the more likely it was that one or more of its elements would be nonfunctional. As a result, the yield of the integrated circuit as a whole would drop to zero, making the technology uneconomical. Similarly, many IBM managers and engineers were skeptical about Moore's contention that improvements in processing capabilities would drive microchip costs down. They favored another approach to miniaturization—hybrid circuits—for their new line of computers, System/360. Other engineers in the electronics industry argued that Moore's prediction was based only on a few data points and that, as a result, its predictive power was nil. They also contended that the plot was an artifact of the observer, as it was based exclusively on Fairchild's microchips.[13]

But Moore's plot and his attendant prediction on the future of integrated circuits also had their supporters, including within Bell Labs and the research laboratory of IBM. None were more vocal than Patrick Haggerty and other Texas Instruments (TI) executives. Like Moore, they contended that microchips would make "impressive contributions" to electronic systems by "removing limitations of reliability, cost, and complexity."[14] For example, in an article published in 1966, Richard Petritz, the director of TI's semiconductor research and development laboratory, predicted the advent of large-scale integrated (LSI) circuits,

12. Moore, "Cramming More Components."

13. Morton, *Organizing for Innovation*; Ross and Reed, "Functional Devices"; Ross, interview; Sello, interview.

14. Patrick Haggerty cited in Richard Petritz, "Technical Foundations."

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chips with thousands of transistors, and he forecasted that within ten years, integrated circuit density would reach a million transistors per square inch. He also presented his own version of Moore's plot, which exhibited a slower rate of complexity increase than Moore's. Like Haggerty and Petritz, executives at Motorola pushed for constant increases in chip complexity in the second half of the 1960s.[15]

It was at Fairchild that Moore's article had the greatest impact. Starting in 1965, Moore used his plot as a planning tool to guide process and product development and allocate financial and engineering resources within his laboratory. He instructed researchers to increase chip complexity by a factor of two every year. By doing so, Moore surmised, Fairchild would stay ahead of its competitors and remain on top of Moore's band. This was important for economic reasons. The more complex the microchip, the more profitable it became. With the profits made on high performance chips, Fairchild could reinvest in the development of advanced products and processes. In contrast, competing firms such as Sylvania and General Electric that were positioned significantly lower in Moore's band were in a precarious financial situation, so much so that many left the business in the late 1960s and early 1970s. The plot was not only a marketing and technology planning tool. It was also a competitive weapon that would allow Fairchild to commercialize the highest performance chips at the lowest possible cost and stay in the business over the long run.[16]

Promoting Moore's Plot

In the mid-1960s, Moore made another inventive use of his plot. He employed it to spot new technological and entrepreneurial opportunities. In 1966, Moore and his Fairchild colleague, Robert Noyce, noticed that engineers would soon be able to put enough transistors on a die to fabricate a new type of integrated circuit, semiconductor memories. This realization and internal conflicts at Fairchild Camera, Fairchild Semiconductor's parent company, led Noyce and Moore to leave Fairchild and form Intel in 1968. The primary focus of the new firm was to design, produce, and market memory circuits that would replace magnetic cores in computer terminals, minicomputers, and mainframes. Noyce and Moore aimed to commercialize the highest performance chips and sell them at a high price. As soon as these circuits were

15. Petritz, "Technical Foundations"; Sello, interview; Yu, *Creating the Digital Future.*

16. Sello, interview.

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copied by other corporations, they would cease producing them and introduce more advanced products to the market.[17]

This commercial strategy was predicated on adhering to Moore's plot. Intel had to double transistor counts every year in order to stay ahead of its competitors. This objective soon became a fundamental expectation at the firm. To drive the growth in chip complexity, Moore and Noyce put great emphasis on the development and continuous improvement of advanced manufacturing processes. For example, in the late 1960s, they bet their corporation on the development of the silicon gate process. This process relied on polysilicon to form the gates of MOS transistors. It reduced the space between components, thereby enabling the cramming of more transistors onto the same die. Intel's engineers were among the first to adopt projection lithography, a technique that helped produce smaller patterns onto silicon dies. With these processes, Intel's factories produced the most complex microchips, those with the most transistors, in the first half of the 1970s.[18]

Moore's plot also oriented product design. It enabled Intel's managers to determine the complexity they had to achieve with their microchips at any given time. Leslie Vadasz, the head of memory engineering in the late 1960s and early 1970s, later reminisced that Moore's plot "was a sanity check for the product we were designing. As you went along with the design, you had a transistor budget. You looked at it. If you were way off for whatever reason, you took a second look."[19] Another important usage of the plot was its employ in purchasing decisions regarding materials and manufacturing tools. "When you worked with equipment companies and looked at the capability of their equipment," Vadasz added, "you took Moore's [plot] into account. Moore's [plot] was the guide."[20]

The plot was a living instrument, repeatedly tweaked by Moore and his associates at Intel. In the late 1960s and 1970s, Moore regularly updated the graph, adding Intel's chips as the new data points on the curve. He also integrated the development of novel device structures and circuit types into his plot. More importantly, in 1975 Moore revised his plot. In a talk presented at a meeting of the Institute of Electrical and Electronics Engineers (IEEE), he argued that the trend he had identified ten years earlier would soon slow down. He predicted that starting in 1980, the number of transistors per microchip would double every two

17. "Turning Science into Industry"; Vadasz, interview; Lécuyer, *Making Silicon Valley*. On the early history of Intel, see Aspray, "The Intel 4004 Microprocessor"; Bassett, *To the Digital Age*; Berlin, *The Man behind the Microchip*; and Thackray, Brock, and Jones, *Moore's Law*.

18. Vadasz, interview; Brock and Lécuyer, "Digital Foundations."

19. Vadasz, interview.

20. Vadasz, interview; House, interview.

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years, instead of every year. This was a point he reiterated in talks he presented on the future of integrated circuit technology at professional and industry meetings over the next four years. Moore made this forecast on the basis of the growing difficulties Intel's engineers encountered in producing more and more complex integrated circuits. The smaller the silicon structures, the more prominent the contamination problems became. With the silicon gate process and its subsequent incarnations, Intel's engineers had also reduced the space between transistors to the point where there was no space left. According to Moore, only two avenues remained for increasing the number of transistors on the same chip: making the die bigger and reducing the size of the transistors.[21]

In the 1970s, Moore and his Intel colleagues heavily promoted Moore's plot. The plot appeared prominently in talks by Moore, Noyce, Andrew Grove, and other Intel managers. For example, in the mid- and late 1970s, David House, the firm's marketing manager for microprocessors and, later, the general manager of its microprocessor division, started every presentation to customers with a discussion of Moore's plot. In these promotional efforts, Intel's leadership was greatly helped by Carver Mead, a faculty member at Caltech and a friend and business associate of Moore. In the late 1960s and early 1970s, Mead gave a series of talks at universities and corporate research laboratories where he, in his own words, "crusaded" for Moore's plot. He argued that it was possible to scale down transistors to much smaller dimensions and that, as these transistors scaled, all their characteristics would significantly improve. In 1972, Mead and his doctoral student Bruce Hoeinesen published two articles in *Solid-State Electronics* in which they explored the physics of growing chip complexity. This analysis led them to claim that the industry had ten more years of exponential complexity increase in front of it and that by 1980 integrated circuits would have ten million transistors per square centimeter.[22]

21. Moore, "Progress in Digital Electronics"; Moore, paper presented at the Fourteenth Symposium on Electron, Ion and Photon Beam Technology, May 1977, in box 6, folder 11; Moore, "Future Directions in Silicon Device Technology," September 1977, in box 6, folder 14; Moore, presentation at the General Electric Microprocessor Symposium, 11 October 1977, in box 7, folder 2; Moore, "Are We Ready for VLSI2?" talk presented at the Caltech Very Large Scale Integration Symposium, January 1979, in box 8, folder 1— all in Gordon Moore Papers; Hoeinesen and Mead, "Fundamental Limitations in Microelectronics –I. MOS Technology"; Sello, interview; House, interview.

22. Hoeinesen and Mead, "Fundamental Limitations in Microelectronics–I. MOS Technology" and "Fundamental Limitations in Microelectronics–II. Bipolar Technology"; House, interview; Mead, interview conducted by Fairbairn; Mead, interview conducted by Cohen.

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Intel's managers and their academic allies publicized Moore's plot very heavily, because many in the industry thought that the trend toward greater integration was about to end (predictions on the imminent demise of exponential complexity growth have been a continuous feature of Moore's Law's history). The plot's greatest critic in the late 1960s and the first half of the 1970s was Robert Keyes, a physicist working at IBM's research laboratory. Keyes published several articles in *IEEE Spectrum* and the *Proceedings of the IEEE* in which he contended that the evolution toward smaller and smaller dimensions would soon encounter physical limitations. Keyes argued that the smaller the transistors would become, the higher the dissipated power would be, and the more likely it was that the die would melt. Other limits to miniaturization, Keyes asserted, were electrical resistance, dielectric breakdown, and electromigration, the phenomenon whereby electrical currents carried aluminum atoms with them, thereby breaking the aluminum lines interconnecting transistors. These articles were influential. They garnered its author the W. R. G. Baker prize of the IEEE and a membership in the National Academy of Engineering in 1976. It was essential for Moore and his colleagues to counter the arguments of Keyes and other experts regarding the end of exponential growth in chip complexity. They had to convince the semiconductor community that the plot was valid, because their ability to follow Moore's plot depended upon the work of engineers developing new materials, processes, and manufacturing equipment outside of Intel.[23]

But Intel's managers had other reasons for promoting Moore's plot. They relied on the plot to sell their own products. They were aware that Intel's microprocessors were often subpar in comparison with those of competitors such as Zilog and Motorola. "Usually, we did not have the best processor," House later admitted, "so I was selling futures and Moore's [plot] was a great way to talk about the future."[24] In essence, House told potential buyers that purchasing Intel microprocessors, however imperfect they may be, was buying into an architecture that would become more and more powerful over time as chip complexity increased. This sales pitch, which had no equivalent at Zilog, resonated well with computer, automotive, and telecommunications customers, who were interested in continuously upgrading their products with more powerful microchips and, at the same time, sought to preserve their software investments. House was not alone in using Moore's plot to sell Intel's chips. Moore, Noyce, and Grove also employed it in their

23. Keyes, "Physical Problems and Limits"; Keyes, "Physical Problems of Small Structures"; Keyes, "Physical Limits in Electronics"; Marshall, "Robert Keyes"; Mody, *The Long Arm of Moore's Law*.

24. House, interview.

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presentations to customers. The plot remained a major sales tool at Intel well into the 2000s. Talking about Moore's plot at professional meetings was also a way for Moore and his managers to stimulate the thinking of the user community regarding potential uses for increasingly complex microchips, get a sense of what the users might need, and therefore identify the types of circuits Intel's engineers should design.[25]

As a result of these promotional efforts, Moore's plot became increasingly accepted in the American semiconductor community in the late 1970s. Reinforcing its credibility was the fact that it was based, by then, on a greater number of data points. Intel's commercial success and the growing prominence of its creator also contributed to the plot's growing acceptance. For much of the 1970s, Intel stood out as the fastest-growing and most-profitable corporation in the entire U.S. microelectronics industry. Moore was increasingly visible as well. Replacing Noyce, he became Intel's chief executive officer in 1975.[26] It was within this context that Moore's plot, in its 1975 version, became referred to as "Moore's Law."[27] The term appeared for the first time in print in an article on the past and future of integrated circuits published by Lester Hogan, Fairchild's associate chairman, in March 1977. A few months later, the expression was used by Noyce in an article on microelectronics in *Scientific American*. In the following years, Moore's Law increasingly showed up in the trade press, in journals of the IEEE, and at technology conferences such as the International Solid-State Circuits Conference (ISSCC). With this semantic shift, the perceived nature of the plot changed. It gained all the authority of a "law." For many American engineers, Moore's graph became a near-physical law governing the development of semiconductor technology.[28]

But the universal acceptance of Moore's Law does not mean that it was adopted as a technology-planning tool by all American microelectronics firms in the late 1970s and early 1980s. In fact, relatively few were the corporations that considered it to be an essential component of their competitiveness and utilized it to guide the development of new technologies. Besides Intel and Fairchild, they consisted mostly of TI, AMD, Motorola, and AT&T (the firm had finally converted to Moore's

25. Moore, talk at Xerox briefing, February 1980, in box 9, folder 3, Gordon Moore Papers; Grove, AT&T presentation, 14 March 1989, in box 17, folder 31, Andrew Grove Speeches; House, interview; Everhart, interview; Bernard Peuto, communication to the author, 6 July 2012.

26. Everhart, interview; Monticelli, "The Wild, Wild West."

27. The origins of the term are unclear. According to Sello, it was the way Moore's direct reports at Fairchild referred to his mandate of doubling chip complexity every year in the mid-1960s. Sello, interview.

28. Hogan, "Reflections"; Noyce, "Microelectronics"; Friedrich et al., "Foreword."

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Law). At other corporations, Moore's Law was viewed as a reassurance that the trend toward greater complexity would continue in the foreseeable future. Signetics, a large Silicon Valley–based manufacturer of logic and linear circuits, is a case in point. In the late 1970s and early 1980s, Signetics conducted several planning exercises that argued that Moore's Law was a long-term trend and there were no immediate physical limitations to the fabrication of finer and finer structures. However, this discussion did not lead the authors of the reports to define a series of technological objectives on the basis of Moore's curve. They focused exclusively on the next generation of process technology and took competitive pressures, rather than the law's cadence, as their main goal setter. This utilization of Moore's Law seems to have been common in most U.S. semiconductor firms at the time.[29]

Revising Moore's Law and Transforming the Modalities of Its Use

In the early and mid-1980s, Moore and his associates at Intel modified the cadence of Moore's Law. They also changed the ways in which they employed it for technology planning. These transformations were made in response to fierce competition coming from Japan. Starting in the mid-1970s, Japanese chipmakers emerged as major players in the semiconductor business. They controlled a growing share of the world market for semiconductors. They also became increasingly competent technically and moved up very quickly within Moore's band. They introduced increasingly complex memories to the market. By 1983 and 1984, they were on par with or ahead of Intel and other U.S. firms for key metrics such as transistor count, transistor size, and the width of metal lines.[30]

The Japanese surge was not predicated on Moore's Law but on the use of another planning tool, the rule whereby the capacity of memory chips increased by a factor of four every three years. Technical leaders in Japan, such as Yasuo Tarui of MITI's VLSI program and engineering managers at NEC, Hitachi, Toshiba, and Fujitsu, were well aware of

29. Zilog, an Intel spin-off, did not use Moore's plot either. Peuto, communication to the author. For planning at Signetics, see "Planning Assumptions: 1979 Technology Forecast," 12 November 1979, box 24, folder: planning assumptions: technology forecast, 1979-11-12, Donald Liddie Papers; "Signetics Business Plan 1979–1982," 14 November 1978, folder: Business Plan, 1979–1982, and "Signetics Corporate Strategic Plan, 1985–1988," 25 June 1984, folder: Signetics Strategic Plan—both in box 18, Donald Liddie Papers.

30. Moore, "The Crisis in Microelectronics," UC Berkeley, 5 February 1983, in box 11, folder 8, Gordon Moore Papers; Tarui, interview; Flamm, *Mismanaged Trade*; Fransman, *The Market and Beyond*; Langlois and Steinmueller, "The Evolution of Competitive Advantage"; Nishi, "The Japanese Semiconductor Industry."

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Moore's Law. However, like their counterparts at most American firms, they viewed it as a reassurance that the complexity and density of integrated circuits would continue to increase. For product and process planning, they preferred another tool, the rule whereby the capacity of semiconductor memories quadrupled every three years. Unlike Moore's Law, which emphasized transistor counts, the Japanese metric was based on product performance. It also had a different tempo—three years, instead of the two years of Moore's Law in its 1975 version.[31]

Japanese executives employed their rule in ways that were different from Moore's own utilization of Moore's Law. They were much stricter in applying it to the development of new products and manufacturing processes. Their engineering groups followed the capacity rule in a highly disciplined and regimented fashion. The focus was on quadrupling product capacity precisely every three years. In contrast, Moore and executives at Motorola and Texas Instruments applied Moore's Law much more loosely. To outdo Japanese corporations, they emphasized radical process innovation, rather than incremental improvements and strict observance of Moore's Law. These efforts to leapfrog the Japanese ended in failure and, starting in the early 1980s, Intel and most other American firms commercialized memories with similar capacities significantly later than their Japanese rivals.[32]

The Japanese surge in integrated circuit complexity forced Moore to increase the cadence of his law. Starting in 1983, he instructed Intel's engineers to "accelerate [the] rate of technical change."[33] Translating the Japanese capacity metric into component counts, he asked them to increase device complexity at the "rate of four times every three years."[34] (figure 2) This became the new formulation of Moore's Law at Intel. To double the number of transistors per chip every eighteen months, Moore and his managers made very significant investments in process engineering. Substantial resources were devoted to the development of one micron and submicron processes (each process being named after the size of the transistor gate).[35]

31. Tarui, interview; Oya, interview; Niwa, interview; Fukuma, interview.

32. Tarui, interview; Vadasz, interview; Pollack, "Japan's Big Lead in Memory Chips"; Wilson, "Intel Wakes Up to a Whole New Market Place."

33. Moore, presentation given to the electronics industry group of the New York Society of Security Analysts, 23 February 1983, in box 11, folder 6, Gordon Moore Papers.

34. Moore, "The VLSI Complexity Crisis," talk given at Dataquest Semiconductor Industry Conference, October 1983, in box 11, folder 14, Gordon Moore Papers.

35. Moore, "Winners by Design," 24 February 1982, in box 10, folder 12, Gordon Moore Papers; Richard Pashley, presentation at the Regis McKenna, Inc. Semiconductor Memory Forum, February 1984, in box 12, folder 2, Gordon Moore Papers; Gerhard Parker, presentation on components technology development, January 1985 in box 13, folder 4, Gordon Moore Papers.

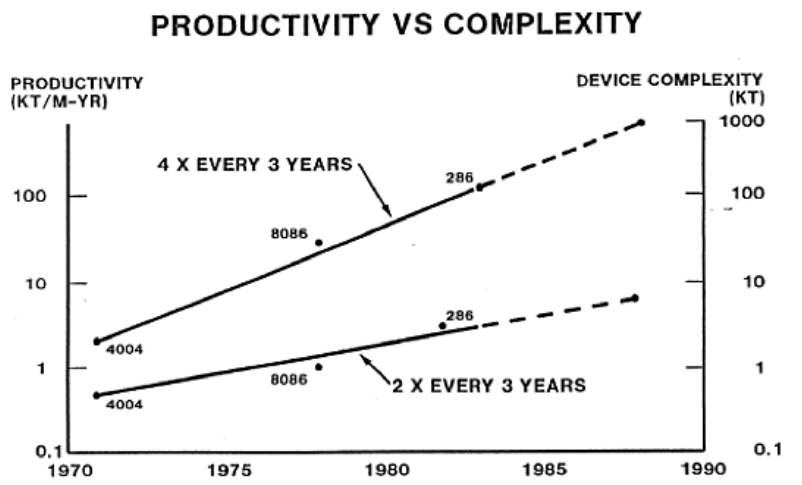

Figure 2 Moore's Law, 1983. Moore defined Moore's Law publicly for the first time as the quadrupling of the number of transistors every three years at the Dataquest Semiconductor Industry Conference in 1983. He also noted that chip design productivity doubled every three years. Source: Gordon Moore, "The VLSI Complexity Crisis," October 1983. Courtesy of Department of Special Collections, Stanford University Libraries.[36]

Following the Japanese model of disciplined implementation, Moore applied Moore's Law much more strictly to the engineering of Intel's products and processes. To stay as close as possible to the new version of the curve, Moore, Vadasz, and other Intel managers coupled Moore's Law with other planning tools. In the early 1980s, they developed plans for "strategic capability segments" that set technology directions and identified long-range requirements. They later adopted a new managerial instrument that had been pioneered at Motorola in the mid- to late 1970s: the technology roadmap. The technology roadmap defined detailed technical milestones over the next five to ten years. It rested on the expertise of the firm's engineers and, as a result, obtained their buy-in. It also served as a communication tool across the corporation and with outside suppliers. In 1985, Moore convened a workshop to create such a roadmap at Intel. His marching orders were clear: define "the key research and development activities which we should be involved in to ensure leadership in the areas where we participate" and develop "the technical strategy Intel should pursue."[37] He expected "the resulting 'technology roadmap'" to "form the basis for implementation of basic research activities" up until 1995. In the

36. Box 11, folder 14, Gordon Moore Papers.

37. Moore to Parker, "The World of the 1990s," 26 February 1985, in box 14, folder 1, Gordon Moore Papers.

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following years, Intel's staff regularly updated the roadmap to take new technical and competitive developments into account.[38]

But following Moore's Law much more strictly also meant developing technologies characterized by different degrees of resolution in parallel and introducing the resulting products sequentially to the market. Intel's managers called this strategy "pipelining." "It took on average three years and nine months to design a new processor," House later reminisced. "If I start development every two years and stagger it, I can stepwise approximate Moore's Law. But if I wait, if I do only one generation [at a time], I get a four-year step before I get back to Moore's Law and I am always below it."[39] To stay on Moore's Law, Intel's engineers introduced a new microprocessor in production every two years, "shrunk" this design (that is, reduced its dimensions through process improvements) each intervening year, and repeated this sequence for the next microprocessor over the following two years. The pipelining of process development and microprocessor design, along with the building of detailed roadmaps, enabled Intel to follow Moore's curve, in its 1983 version, much more precisely. It also allowed the firm to progressively regain its former position at the top of Moore's band in the late 1980s and early 1990s. Along with the sole sourcing of its chips and the revival of its manufacturing operations, the relentless pursuit of Moore's Law enabled Intel to create a near-monopoly for its microprocessors in the fast-growing personal computer market. By 1992, Intel had become the largest semiconductor firm in the world.[40]

To respond to the Japanese challenge, Moore and Noyce also built collaborative research organizations with their counterparts at other large chip-making corporations: IBM, Motorola, National Semiconductor, and Texas Instruments. In 1987 they established Sematech, a research consortium aimed at closing the gap in manufacturing with Japanese chipmakers. Because all the corporations dominating Sematech had by then incorporated road mapping into their technology-planning exercises, the drafting and implementation of technology roadmaps became a central activity of the new organization. Indeed, Sematech was launched through the convening of workshops that

38. For road mapping at Motorola and other U.S. firms, see Willyard and McClees, "Motorola's Technology Roadmap Process," and Robert Schaller, "Technological Innovation in the Semiconductor Industry." For planning at Intel, see Vadasz, presentation prepared for the Bell Telephone Laboratories' visit to Intel, 1 November 1979 in box 8, folder 13, Gordon Moore Papers; Moore to Parker, 26 February 1985 and Eugene Meieran to Alan Baldwin, "Technology Strategy Workshop," 6 March 1985— both in box 14, folder 1, Gordon Moore Papers; Vadasz, interview; House, interview.

39. House, interview.

40. House, interview; Hasell, "The Intelligence of Intel"; Thackray, Brock, and Jones, *Moore's Law*; Lécuyer, "Confronting the Japanese Challenge."

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defined roadmaps for key manufacturing processes such as epitaxy, photolithography, and ion implantation. These roadmaps then provided the basis for the organization's five-year plan and oriented its research and development activities. Through their involvement with Sematech and a related organization, the Semiconductor Research Corporation (SRC) that financed semiconductor research at universities, Intel's engineers and managers gained significant experience with collective technology road mapping. They also learned how to articulate Intel's internal roadmap with the collective roadmaps of Sematech and the SRC.[41]

Institutionalizing Moore's Law

Moore further institutionalized Moore's Law by establishing the National Technology Roadmap for Semiconductors (NTRS) in 1992. The new organization emerged at the convergence point of several developments. The Semiconductor Industry Association (SIA) that represented American microelectronics corporations was interested in reinforcing the technological base and competitiveness of U.S. semiconductor firms. To do so, in early 1991 the SIA formed a new committee—the technology committee—the objective of which was to shape the nation's semiconductor technology policy, and it gave its headship to Moore. By then, Moore was Intel's chairman of the board and the most respected figure in the U.S. semiconductor industry. This new policy interest on the part of Moore and the SIA coincided with a retreat of the federal government from technology policy, a trend that emerged at the end of the George H. W. Bush administration and was amplified under Bill Clinton.[42]

Another factor in the formation of the NTRS was the upcoming dissolution of the National Advisory Committee for Semiconductors (NACS). This committee, directed by Ian Ross of AT&T, had been established by Congress in 1988 to develop a national strategy in microelectronics. In April 1991, the NACS sponsored the development of a technology roadmap, MicroTech 2000. This roadmap, elaborated by ninety experts coming from academia, government, and industry, laid out the steps that the semiconductor industry would need to take in order to be one process generation ahead of the Japanese by 2000. This

41. Schaller, "Technological Innovation in the Semiconductor Industry"; Spencer and Seidel, "International Technology Roadmaps."

42. Moore to SIA Board of Directors, 10 September 1991, in box 33, folder 19, Gordon Moore Papers; Moore, "The Cowboys Who Became Settlers: The Semiconductor Industry Surviving by Becoming Involved," 10 March 1992, in box 25, folder 1, Gordon Moore Papers.

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was a very ambitious goal that would require a large increase in the resources allocated to semiconductor innovation and much tighter collaboration among American microelectronics corporations. As the NACS was about to submit its final report to Congress, Ross approached the SIA and asked it to take over the MicroTech roadmap and transform it into a living document that would be regularly updated and managed by a permanent organization.[43]

Moore seized this offer. He saw it as a way of sustaining exponential growth in chip complexity at a time when engineers encountered more and more problems in following Moore's Law. It was also, for him, an opportunity to reinforce Intel's and the U.S. semiconductor industry's competitive position and market share on the global scale, at the expense of the Japanese. However, judging the tempo of the NACS roadmap and the closeness of the collaborations it required to be impractical, Moore set out to reshape it. He was interested in creating a national roadmap that would take over the roadmap of the NACS and those of Sematech and the Semiconductor Research Corporation, two organizations controlled by the SIA. Using Moore's Law as its primary guidance, the new roadmap would provide long-range technology planning to the industry as a whole. In particular, it would identify "holes" requiring additional research efforts and focus the activities of SRC and Sematech and the investments of the federal government on filling these holes. On the model of Intel's internal roadmaps, the national roadmap would also deliver "actionable" planning. It would be realistic enough for corporations and governmental organizations to focus on reaching its main milestones.[44]

In the fall of 1991, Moore convinced the CEOs of other large microelectronics corporations to back this project. There was much in it that they liked. Taking advantage of the relaxation of antitrust laws since the mid-1980s, Moore proposed to them, in essence, that they form an innovation cartel. This cartel would set the direction and pace of innovation for the industry as a whole. It would be dominated by large corporations through their representation in key committees. With its focus on sustaining exponential complexity growth, it would also set rules for competition that favored the most established corporations because of their greater engineering and financial resources. In addition, Moore gained support for the national roadmap from members of the NACS and several branches of the federal government, including

43. Moore to Wilfred Corrigan, 1 June 1991, in box 33, folder 17, Gordon Moore Papers; Moore to Bill Howard, 30 December 1991, in box 25, folder 11, Gordon Moore Papers; Spencer and Seidel, "International Technology Roadmaps"; Ross, interview.

44. Moore to Howard, 30 December 1991; Moore, "Trip Report," 18 December 1991, in box 33, folder 20, Gordon Moore Papers; House, interview.

the Department of Defense and the Office of Science and Technology Policy.[45]

At Moore's request, William Howard, a former Motorola executive, and Robert Burger, the head of the SRC, organized the workshop that defined the SIA's national roadmap in November 1992. Howard, Burger, and executives from Intel, IBM, AT&T, Motorola, Hewlett-Packard, and Texas Instruments, specified the roadmap's complexity metrics, the milestones in terms of gate counts, bit tallies, and clock frequencies, for five process generations over the next fifteen years. Howard and Burger also invited 170 experts from a wide variety of firms and, to a lesser degree, from academia and governmental organizations, to populate the working groups that translated these metrics into detailed lists of development needs for lithography, interconnects, packaging, and other technologies.[46]

Indicative of the general thrust of the workshop, the removal of obstacles to exponential complexity growth, was Moore's introductory keynote speech (figure 3). After stressing the critical importance of the roadmap for national competitiveness, Moore asked attendees to share their "BEST knowledge and thinking" on "what will happen if we CONTINUE [the exponential trend in chip complexity], where that will put us competitively, and what LONGER RANGE activities should be undertaken either to lay a foundation [for technologies needed to stay on Moore's Law], or to assure that a possible alternative is not precluded. … Our task is to remove roadblocks to continue the trends [toward greater integration] as long as we can and anticipate where we hit the stops."[47]

The roadmap that ensued was published by the SIA in early 1993. It was highly influential. So was the update report that followed in 1994. These documents were employed throughout industry and government to prioritize investments regarding the development of microelectronics technologies. At Moore's urging, Sematech and the SRC realigned their programs to address the issues highlighted by the roadmap. For example,

45. Moore, "Mr. Moore Goes to Washington," 13 March 1992, in box 33, folder 21, Gordon Moore Papers.

46. For the planning of the workshop, see Moore to Bill Howard, 30 December 1991; Bob Burger, "Proposal: SIA Semiconductor R&D Strategy Roadmap Workshop," 19 May 1992; Larry Sumney to Moore, 28 May 1992; Bill Siegle to Warren David, 6 June 1992; "SIA Semiconductor Technology Workshop Steering Committee Meeting Summary," 2 September 1992; Minutes of the SIA Semiconductor Technology Workshop Steering Committee Meeting, 1 October and 22 October 1992—all in box 25, folder 11, Gordon Moore Papers. Robert Burger, "Proposal–SIA Semiconductor R&D Roadmap Workshop," 19 May 1992 and Larry Sumney to Moore, 29 May 1992, both in box 60, folder 8, Gordon Moore Papers. Robertson, "Moore: Unify Tech Strategy"; Spencer and Seidel, "International Technology Roadmaps."

47. Moore, notes for the SIA Technology Roadmap meeting, 17 November 1992, in box 25, folder 11, Gordon Moore Papers.

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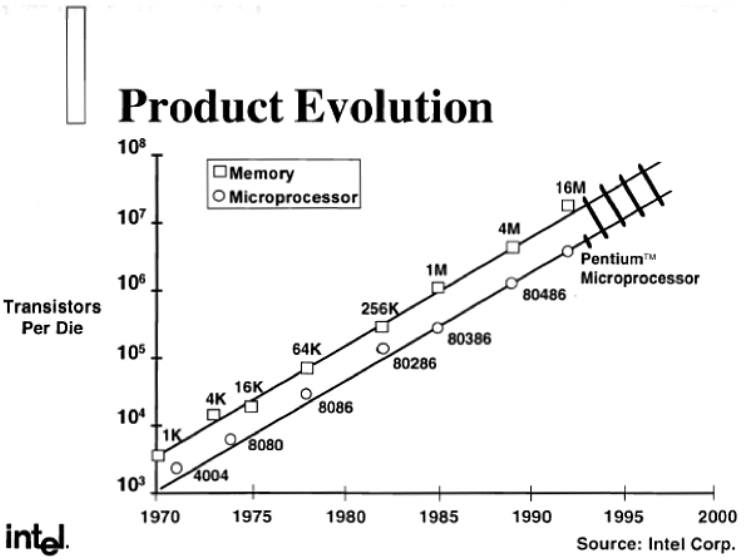

Figure 3 Setting the objective for the NTRS, 1992. In his keynote speech at the SIA road-mapping workshop, Moore focused attendees' attention on exponential complexity growth over the next fifteen years, the crossed-out area in the graph. Source: Gordon Moore, "Moving to a Single Roadmap," November 17, 1992. Courtesy of Department of Special Collections, Stanford University Libraries.[48]

the SRC required that all research proposals it received from academic investigators emphasize their relevance to the roadmap. As Moore had hoped, the NTRS also influenced governmental action. The Defense Advanced Research Projects Agency, the National Science Foundation, and other federal agencies awarded hundreds of millions of dollars in grants for semiconductor research to universities in strict accordance with the roadmap. Faculty members requesting support for semiconductor projects laying outside of the roadmap had very little chance of getting funded. Responding to significant pressure coming from the Clinton administration, the national laboratories expanded their research programs on semiconductors. They collaborated closely with Intel and other corporations, especially in the area of EUV lithography, which promised to pattern nanoscale microchips.[49]

Microchip makers also employed the technology roadmaps internally to allocate resources and coordinate R&D efforts with other firms, but the greatest users of the NTRS reports were the suppliers of specialized

48. Box 25, folder 11, Gordon Moore Papers.

49. Moore to Bill Clinton, 22 December 1992, in box 33, folder 23, Gordon Moore Papers; SIA, *National Technology Roadmap for Semiconductors*, 1994; Wollesen, "Roadmap Implementation"; Schaller, "Technological Innovation in the Semiconductor Industry."

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materials and manufacturing tools. Indeed, one of the primary functions of the roadmap was to communicate the specific needs of integrated circuit manufacturers to the producers of electronic chemicals and production equipment. These suppliers devised their own product offerings to meet the roadmap's requirements. In short, the NTRS became nearly sacrosanct across the U.S. microelectronics community. Moore was one of the very few individuals who could publicly find fault with the roadmap and its tempo. In the early andmid-1990s, he did so repeatedly to prevent blind observance of the roadmap and to attract the attention of the semiconductor community on the economic and technological obstacles facing the industry in its effort to follow Moore's Law. As a result of Moore's public pronouncements, the 1994 roadmap gave greater attention to economic constraints than its prior version."[50]

The near universal embrace of the roadmap had major repercussions. Microelectronics corporations that had, until then, focused on the next generation of process technology started to engage in long-range planning. They all adopted Moore's Law as their primary technology planning tool. Moore's Law became *the* norm. The NTRS also drove technological convergence. It led to the standardization of materials, equipment, and manufacturing processes across the whole industry. "The roadmap steers competitors toward nearly identical memory and microprocessor technologies," a Hewlett-Packard manager closely involved with the roadmap remarked in 1995. "This convergence is critical. It enables equipment suppliers to develop tools with cost effective performances since all customers must basically use them in the same way."[51]

The pace of technology development also increased significantly. In 1995, Intel, Texas Instruments, and other leading firms publicly announced that process technologies progressed more rapidly than the objectives set by the roadmap. This acceleration was made possible by the greater focus, efficiency, and urgency, and the increased resources the NTRS brought to semiconductor research, but it can also be explained by a simple social phenomenon. Because all corporations knew what the targets were, they went faster than the pace set by the roadmap in order to gain an advantage over their competitors. By establishing Moore's Law at the very center of the industry, Moore had changed the very slope of Moore's band, tilting it upward.[52]

50. Spencer and Seidel, "International Technology Roadmaps"; Agres, "IC Density Growth Rate"; "Repealing Moore's Law;" Bartelink, "The Roadmap Can Help Collaborations."

51. Bartelink, "The Roadmap Can Help Collaborations."

52. Agres, "IC Density Growth Rate"; Robertson, "Speeding in Fast Lane"; Peercy, "The Drive to Miniaturization"; Vadasz, interview; House, interview.

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Competing with Moore's Law and the Roadmaps

To stay at the leading edge, Moore and his closest associates, Grove and Barrett, positioned Intel's internal technology roadmap ahead of the NTRS in the early and mid-1990s. Intel's roadmap was at least a year ahead of the national roadmap. It also differentiated itself from it, by selectively emphasizing areas in which Intel could gain a technological advantage. Also critical for Intel maintaining its leading position in Moore's band were the close relations it forged with equipment suppliers. The chipmaker invested heavily in U.S. equipment manufacturers, such as Silicon Valley Group Lithography that fabricated advanced production tools. It also put significant engineering time in the development, improvement, and testing of their equipment, but these investment of time and money came with the condition that Intel would be the first to purchase the tools and employ them on its own manufacturing lines. Along with the timing of the internal roadmap, close relations with suppliers enabled Intel to produce the most complex microchips. Its grip over the semiconductor market increased.[53]

Later in the decade, Intel's management took control of the NTRS to reinforce their firm's technological and competitive position over the long term. Critical for this takeover was Paolo Gargini, an engineering manager close to Barrett. Like Moore, Barrett was increasingly concerned that the NTRS was not detailed and quantitative enough. In his view, it also did not concentrate sufficiently on the long range, especially the significant obstacles Intel and other firms would need to overcome in order to produce microchips with nanoscale features. For instance, no one knew how to pattern microchips at the 100-nanometer process node and those that would follow. Materials that had been critical for the fabrication of integrated circuits since the 1960s would cease to function properly. Layers of polysilicon and silicon oxide would become so thin that electrons would move through them. Entirely new materials would have to be developed for nanoscale integrated circuits.[54]

Exploiting inconsistencies in the 1994 roadmap and benefitting from the considerable heft of his employer, Gargini took control of the NTRS, thereby transforming the innovation cartel into a quasi extension of Intel. He became vice-chair of the 1997 roadmap and the head of its most important committee, the one setting the roadmap's principal targets. Gargini chaired the next iteration of the roadmap and those that followed over the next fifteen years. This position of power enabled

53. Vadasz, interview; Meieran, interview; Gargini interview.

54. Gargini, interview; SIA, *National Technology Roadmap for Semiconductors*, 1997; Buurma, "Heartfelt Words for a Troubled IC Industry"; Grayson, "Chips and a Lifelong Passion"; Brown and Linden, *Chips and Change.*

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him and Barrett to set the pace for technology development for the entire American and, later, global microelectronics industries. Taking stock of the acceleration in the development of manufacturing processes since 1994, Gargini stipulated in the 1997 roadmap that the industry would introduce new process generations every two years, instead of every three years, for the next six years. He knew well that this choice would further accelerate complexity growth, as the largest and most technically proficient firms would go faster than the roadmap and introduce new manufacturing processes in less than two years. In contrast, the smaller corporations or those that were already behind in Moore's band would struggle to keep pace. They would also have to buy increasingly expensive manufacturing equipment at a time when their returns on investment, because of their lateness, would most likely decrease. Gargini and Barrett surmised that many would abandon the complexity race over the medium term.[55]

To focus the attention of the U.S. semiconductor community on the long-range problems facing Moore's Law, Gargini transformed the format of the NTRS. Under his leadership, the roadmap's main targets were stipulated in much greater detail, including not only transistor counts, but also chip size, performance, defect density, power dissipation, and manufacturing cost. The main change, however, was in the tables produced by the working groups. These tables converted the overall roadmap targets into a set of objectives for the many technologies involved in the design and processing of microchips. They became much more detailed. They were also color coded: yellow indicating the targets for which new technologies were then in development and red for those no expert knew how to reach. This color scheme concentrated the attention of researchers at firms, universities, and national laboratories on the "red" problems, the pressing questions confronting Intel and the industry as a whole.[56]

One of the most significant issues was the development of high K materials that would replace polysilicon in transistor gates. "I had the idea," Gargini later reminisced, "that by the middle of the next decade, 2004/5/6, we had to introduce high K metal gates. At the end of the [1997 roadmap] meeting, the university people were terrorized [by this prospect]. It was a terror for all of them [that] all of a sudden something that was a very low-key project was becoming very important.… This created a panic."[57] Artfully prompted and maintained by Gargini, this concern led research groups at American universities to work on new insulating materials for transistor gates. Many other projects were also launched to

55. Gargini, interview.

56. SIA, *National Technology Roadmap for Semiconductors*, 1997; Gargini, interview.

57. Gargini, interview.

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develop low K materials that would not have the limitations of silicon oxide. Federal agencies financed these research programs.[58]

However, it rapidly became clear to Barrett and Gargini that the entire financial and engineering resources devoted to semiconductor research and development in the United States would not be sufficient to solve the many problems of nanoscale microchip manufacturing. In order to find cost-effective solutions for Intel, they would need to mobilize the resources of foreign corporations and research establishments as well. This assessment persuaded Gargini to internationalize the roadmap by opening it to the Japanese, Korean, Taiwanese, and European microelectronics industries in 1998. Another reason for creating the International Technology Roadmap for Semiconductors (ITRS) was the efforts in Japan to form a national roadmap that would compete with the NTRS. Japanese corporations had, by then, lost their dominant market share to American chipmakers. They were interested in creating their own roadmap in order to shore up their declining competitiveness. The formation of a Japanese roadmap represented a sizeable threat for Intel. It would convince equipment makers to divert part of their resources toward the development of tools meeting the stipulations of the Japanese roadmap instead of those of the NTRS. Gargini stifled this project by threatening a rekindling of the semiconductor wars of the 1980s. He persuaded the Japanese to join the upcoming ITRS. The European, Korean, and Taiwanese semiconductor industries followed.[59]

The international roadmap was closely patterned after the national roadmap. It was also dominated by Gargini and Intel. The ITRS further expanded the use of Moore's Law as a technology planning tool. As they joined the ITRS, the Japanese embraced Moore's Law. The international roadmap also led to process convergence at the global scale. Under Intel's guidance, it piloted the development of new semiconductor technologies in the United States, Japan, Europe, and, to a lesser extent, Taiwan and South Korea for much of the 2000s. The European Union and Japanese and European governments partially financed these research programs. Heavy R&D investments on the global scale and the inner workings of the international roadmap enabled Intel to identify the best solutions to the challenges posed by the shift to the nanometer scale and integrate them into its own manufacturing processes. Intel, for instance, introduced microprocessors with high K metal gates to the market in 2007. It was the first corporation to do so.[60]

58. Gargini, interview.

59. Meieran, interview; Gargini, interview; Fukuma, interview; Niwa, interview.

60. Gargini, interview; Niwa, interview; Toriumi, interview; Hiramoto, interview.

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The ITRS weakened American, Japanese, and European corporations. They were put on Intel's "treadmill," struggling to sustain the pace imposed by the chipmaker and solve the considerable problems of producing chips with nanoscale features. Because of their active involvement in the roadmap, Japanese firms lost some of their strategic capability. Intel further undermined their competitive position by setting the ITRS targets significantly behind those of its own internal roadmap. For example, Intel announced its use of low K materials a year and a half ahead of the ITRS official target. As a result of the pace imposed by Intel and the growing cost of manufacturing equipment, more and more microelectronics corporations in Japan, America, and Europe dropped out from exponential scaling in the mid- to late 2000s. This left only a handful of firms actively pursuing Moore's Law, the most prominent of which were Intel, TSMC, and Samsung.[61]

Conclusion

In the early and mid-1960s, Gordon Moore shaped Moore's law into a tool to drive semiconductor innovation, sell integrated circuits, and compete with other chipmakers. He later adapted it to changing economic and technological conditions. He modified its cadence several times. He also associated it with the technology roadmap, another planning instrument that, at his instigation, later became a structure of innovation governance. During his tenure at Fairchild, Moore employed Moore's Law to set objectives and allocate resources in his research laboratory. In the 1970s and early 1980s, he transformed it into a critical tool of innovation management at Intel. In contrast, relatively rare were the American chipmakers that utilized the law to plan new products and processes during the same period. It was only in the early 1990s, with the formation of the NTRS, that they universally adopted Moore's Law to manage semiconductor innovation. It took another ten years for Japanese chipmakers to integrate the law fully into their own technology planning processes.

The gradual adoption of Moore's Law transformed Moore's band. At first, it affected the positions of individual firms within the band. Corporations that embraced Moore's Law as a planning tool and made the necessary investments moved to the top of the band. The institutionalization of Moore's Law, with the formation of the NTRS, changed the band's slope. Because the largest firms sought to beat the roadmap's targets, they accelerated the growth in integrated circuit complexity

61. Niwa, interview; Fukuma, interview; Toriumi, interview; Hiramoto, interview.

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and slanted the band upward. However, as they rapidly increased the number of transistors per microchip, they faced technological problems that were increasingly difficult to solve. The cost of following Moore's Law became so prohibitive that many corporations dropped out of the race in the second half of the 2000s. As a result, Moore's band narrowed significantly, leaving only a handful of chipmakers actively pursuing Moore's Law at the end of the decade.

A number of lessons can be derived from this account of Moore's Law. First, there was nothing inevitable about the law and its evolution. Moore's Law owed much to *one* man, Gordon Moore, his constancy of purpose, and his focus on the long range. The law's growing influence can be partially attributed to Moore's staying power and talent for social engineering, but Moore's Law was also shaped by large historical processes, notably the rivalry between American and Japanese chipmakers. It was in response to the Japanese challenge that Moore and his associates at Intel modified the ways in which they used the law. They coupled it with "pipelining" and road mapping. Later, Moore created the national roadmap to drive chip complexity faster than Japanese corporations. The ITRS was partially conceived as a way of weakening Japanese firms even further by cooperating with them.

Second, innovation in semiconductors was, and still remains, a top-down process. The drive to integrate more and more electronic functions onto microchips came from the very top. At Fairchild and Intel, Moore, Noyce, Grove, and Barrett relentlessly pushed for the design and manufacture of increasingly complex integrated circuits. They instructed their staff to realize this objective and gave them the laboratories and financial resources to do so. With the formation of the NTRS and even more so the ITRS, Intel's leaders expanded their sphere of influence. They set the direction and pace of innovation not only for Intel but for all organizations active in microelectronics, worldwide. Through the road mapping process, the most prominent researchers in the field participated in setting detailed technical objectives, but the main orientations were decided elsewhere, mostly at Intel.

Third, Moore's Law was a formidable tool to weaken and displace competitors over the long term. In 1984, Regis McKenna, the business guru and long-time consultant to Intel, described Moore's Law in the following way: "The longer you wait, the fewer the fish."[62] In other words, the more the microelectronics industry advanced on the path of growing chip complexity in accordance with Moore's Law, the fewer the firms that had the financial and engineering wherewithal

62. Regis McKenna at the Regis McKenna, Inc. Semiconductor Memory Forum, February 1984, in box 12, folder 2, Gordon Moore Papers.

to tackle the problems associated with still greater integration. The other corporations, those unable to sustain the pace, focused on less complex chips for smaller markets or left the industry altogether. This phenomenon was at work throughout the history of Moore's Law: from the late 1960s and early 1970s, when exponential growth in chip complexity led to Sylvania's and General Electric's exit from the industry, to the 2000s and early 2010s, when corporations that had long followed Moore's Law, such as Texas Instruments, abandoned the leading edge to Intel and the largest Korean and Taiwanese firms.

But Intel's triumph did not last long. In the 2010s, the corporation that had been the main advocate of Moore's Law throughout its history and had succeeded in staying at the very top of Moore's band for several decades, gradually lost its process leadership to TSMC and Samsung. The Koreans and Taiwanese, who had been very aggressive at increasing the complexity of their microchips since the mid- to late 1990s, progressively manufactured integrated circuits that were on par, complexity-wise, with those of Intel. At the ITRS, they pushed to accelerate the pace of innovation, whereas Intel sought to slow it down. These disagreements led to the folding of the international roadmap in 2016. Making conservative process choices and facing serious technical difficulties that prompted many observers to predict the end of exponential complexity growth, Intel missed deadline after deadline. It was four years behind schedule in bringing its 10-nanometer process to production. It also encountered yield problems and was unable to meet customer demand for its chips. In contrast, TSMC and Samsung introduced new process generations earlier than their American competitor. They also grew much faster. In 2017, Samsung became the world's largest chipmaker. Intel's recent travails exemplify the central paradox of Moore's Law. In order to drive exponential complexity growth according to Moore's Law, Intel's executives had to convince other corporations to adopt their own tool and strategy. However, as they did so, they left themselves exposed to competitors that could execute exponential integration faster than they did. Managerial tools are double-edged indeed.[63]

63. Hiramoto, interview; Fukuma, interview; Merritt, "Chip Roadmap Reboots"; Merritt, "Intel May Sit Out Race to EUV"; Lee, "Intel Needs New Strategy"; McGrath, "Intel Claims Progress at 10nm Yields"; Clark, "Intel's Culture Needed Fixing." At the time of this writing, exponential complexity growth is alive and well. It is continuing at a brisk pace in memories. In the case of microprocessors and other logic chips, leading firms are currently developing 2-, 3-, and 5-nanometer processes. They are also using larger dies and stacking them one over the other in order to pack more transistors in their devices.

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Bibliography of Works Cited

Books

Bassett, Ross. *To the Digital Age: Research Labs, Start-Up Companies and the Rise of MOS Technology*. Baltimore: Johns Hopkins University Press, 2002.

Berlin, Leslie. *The Man behind the Microchip: Robert Noyce and the Making of Silicon Valley*. New York: Oxford University Press, 2005.

Brock, David, ed. *Understanding Moore's Law: Four Decades of Innovation*. Philadelphia: Chemical Heritage Press, 2006.

Brown, Clair, and Greg Linden. *Chips and Change: How Crisis Reshapes the Semiconductor Industry*. Cambridge, MA: MIT Press, 2009.

Flamm, Kenneth. *Mismanaged Trade? Strategic Policy and the Semiconductor Industry*. Washington: Brookings Institution Press, 1996.

Fransman, Martin. *The Market and Beyond: Cooperation and Competition in Information Technology in the Japanese System*. New York: Cambridge University Press, 1993.

Lécuyer, Christophe. *Making Silicon Valley: Innovation and the Growth of High Tech, 1930–1970*. Cambridge, MA: MIT Press, 2006.

Lécuyer, Christophe, and David C. Brock. *Makers of the Microchip: A Documentary History of Fairchild Semiconductor*. Cambridge, MA: MIT Press, 2010.

Mody, Cyrus. *The Long Arm of Moore's Law: Microelectronics and American Science*. Cambridge, MA: MIT Press, 2016.

Morton, Jack. *Organizing for Innovation: A Systems Approach to Technical Management*. New York: McGraw-Hill, 1971.

Thackray, Arnold, David C. Brock, and Rachel Jones. *Moore's Law: The Life of Gordon Moore, Silicon Valley's Quiet Revolutionary*. New York: Basic Books, 2015.

Yu, Albert. *Creating the Digital Future: The Secrets of Consistent Innovation at Intel*. New York: The Free Press, 1998.

Articles and Chapters in Books

Aspray, William. "The Intel 4004 Microprocessor: What Constituted Invention?" *Annals of the History of Computing* 19, no. 3 (1997): 4–15.

Brock, David C., and Christophe Lécuyer. "Digital Foundations: The Making of Silicon-Gate Manufacturing Technology." *Technology and Culture* 53, no. 3 (2012): 561–597.

Ceruzzi, Paul. "Moore's Law and Technological Determinism: Reflections on the History of Technology." *Technology & Culture* 46, no. 3 (2005): 584–593.

Flamm, Kenneth. "Moore's Law and the Economics of Semiconductor Price Trends." *International Journal of Technology, Policy and Management* 3, no. 2 (2003): 127–141.

Friedrich, Hans, Walter Kosanocky, and Takuo Sugano. "Foreword." *IEEE Transactions on Electron Devices* ED-26 (April 1979): 257.

https://doi.org/10.1017/eso.2020.38 Published online by Cambridge University Press

Hoeinesen, Bruce, and Carver Mead. "Fundamental Limitations in Microelectronics–I. MOS Technology." *Solid-State Electronics* 15, no. 7 (1972): 819–829.

———. "Fundamental Limitations in Microelectronics–II. Bipolar Technology." *Solid-State Electronics* 15, no. 8 (1972): 891–897.

Hogan, Lester. "Reflections on the Past and Thoughts about the Future of Semiconductor Technology." *Interface Age* 2, no. 4 (1977), 24–36.

Keyes, Robert. "Physical Problems and Limits in Computer Logic." *IEEE Spectrum* 6, no. 5 (1969): 36–45.

———. "Physical Problems of Small Structures in Electronics." *Proceedings of the IEEE* 60, no. 9 (1972): 1055–1062.

———. "Physical Limits in Digital Electronics." *Proceedings of the IEEE* 63, no. 5 (1975): 740–767.

Langlois, Richard, and Edward Steinmueller. "The Evolution of Competitive Advantage in the Worldwide Semiconductor Industry, 1947–1996." In *The Sources of Industrial Leadership: Studies of Seven Industries*, edited by David Mowery and Richard Nelson, 19–78. New York: Cambridge University Press, 1999.

Lécuyer, Christophe. "Confronting the Japanese Challenge: The Revival of Manufacturing at Intel." *Business History Review* 93, no. 2 (2019): 349–373.

Marshall, Nathan. "Robert Keyes, 1921–2010." *National Academy of Engineering Memorial Tributes* 16 (2012): 132–136.

Moore, Gordon. "Progress in Digital Electronics." Technical Digest, IEEE International Electron Devices Meeting 21 (1975): 11–13.

———. "Semiconductor Integrated Circuits." In *Microelectronics: Theory, Design, and Fabrication*, edited by Edward Keonjian, 262–359. New York: McGraw-Hill, 1963.

Nishi, Yoshio. "The Japanese Semiconductor Industry." In *Developing the Electronics Industry*, edited by Björn Wellenius, Arnold Miller, and Carl Dahlman, 123–130. Washington: The World Bank, 1993.

Petritz, Richard. "Technical Foundations and Future Directions of Large Scale Integrated Electronics." In *Proceedings of the November 7–10, 1966, Fall Joint Computer Conference*, 65–87. New York: Association for Computing Machinery, 1966.

Ross, Ian, and Eugene Reed. "Functional Devices." In *Microelectronics: Theory, Design, and Fabrication*, edited by Edward Keonjian, 360–375. New York: McGraw-Hill, 1963.

Schaller, Robert R. "Moore's Law: Past, Present, and Future." *IEEE Spectrum*, June 1997, 53–59.

Spencer, William, and Thomas Seidel. "International Technology Roadmaps: The US Semiconductor Experience." In *Productivity and Cyclicality in Semiconductors: Trends, Implications, and Questions*, edited by Dale W. Jorgenson and Charles W. Wessner, 135–150. Washington: National Academies Press, 2004.

Willyard, Charles, and Cheryl McClees. "Motorola's Technology Roadmap Process." *Research Management* 30, no. 5 (1987): 13–19.

Newspaper and Magazine Articles

Anonymous, "Turning Science into Industry." *IEEE Spectrum*, January 1966.

Anonymous, "Repealing Moore's Law." *OEM Magazine*, 1 December 1996.

Agres, Ted. "IC density growth rate is key issue for industry." *R&D*, 1 June 1996.

Bartelink, Dirk. "The Roadmap Can Help Collaborations, but Should not Stamp out Competition." *Solid State Technology*, 1 February 1995.

Buurma, Jack. "Heartfelt Words for a Troubled IC Industry." *Electronics Engineering Times*, 20 January 1997.

Clark, Don. "Intel's Culture Needed Fixing. Its CEO is Shaking Things up." *New York Times*, 1 March 2020.

Gibbs, W. Wayt. "Gordon E. Moore, Part 1." *Scientific American*, 22 September 1997.

Keyes, Robert. "Physical Problems and Limits in Computer Logic." *IEEE Spectrum*, May 1969, 36–45.

Grayson, Ian. "Chips and a Lifelong Passion." *The Independent*, 8 April 1997.

Hasell, Nick. "The Intelligence of Intel." *Management Today*, 12 November 1992.

Lee, Sang-Yun. "Intel Needs New Strategy, ASAP." *Electronic Engineering Times*, 7 March 2018.

McGrath, Dylan. "Intel Claims Progress at 10nm Yields." *Electronic Engineering Times*, 27 July 2018.

Merritt, Rick. "Chip Roadmap Reboots." *Electronic Engineering Times*, 4 May 2016.

Merritt, Rick. "Intel May Sit Out Race to EUV." *Electronic Engineering Times*, 10 October 2017.

Monticelli, Dennis. "The Wild, Wild West." *Electronic Business*, 1 November 2005.

Moore, Gordon. "Cramming more Components onto Integrated Circuits." *Electronics*, 19 April 1965.

Peercy, Paul. "The Drive to Miniaturization." *Nature*, 406, 31 August 2000, 1023–1026.

Pollack, Andrew. "Japan's Big Lead in Memory Chips." *New York Times*, 28 February 1982.

Noyce, Robert. "Microelectronics." *Scientific American*, 237, No. 3, September 1977, 62–69.

Robertson, Jack. "Moore: Unify Tech Strategy." *Electronic News*, 27 July 1991.

Robertson, Jack. "Speeding in Fast Lane." *Electronic Buyers' News*, 29 July 1996.

Wilson, John. "Intel Wakes up to a Whole New Market Place in Chips." *Business Week*, 2 September 1985.

Wollesen, Dan. "Roadmap Implementation." *Solid State Technology*, 1 February 1995.

Reports and dissertation

Schaller, Robert. "Technological Innovation in the Semiconductor Industry: A Case Study of the International Roadmap for Semiconductors (ITRS)." PhD diss., George Mason University, 2004.

Semiconductor Industry Association. *National Technology Roadmap for Semiconductors*. Santa Clara, CA: 1994.
Semiconductor Industry Association. *National Technology Roadmap for Semiconductors*. Santa Clara, CA: 1997.

Interviews and Oral Histories

Everhart, Thomas. *Oral history interview conducted by David C. Brock*. March 28, 2007. Science History Institute, Philadelphia, PA.
Fukuma, Masao. Interview with author. June 14, 2016, and September 11, 2016.
Gargini, Paolo. *Oral history interview conducted by Harry Sello and Daryl Hatano*. July 27, 2011. Computer History Museum, Mountain View, CA.
Hiramoto, Toshiro. Interview with author. June 29, 2018.
House, David. Interview with author. August 15, 2014.
Mead, Carver. *Oral history interview conducted by Shirley Cohen*. July 17, 1996. Archives, California Institute of Technology, Pasadena, CA.
———. *Oral history interview conducted by Doug Fairbairn*. May 27, 2009. *Computer History Museum*, Mountain View, CA.
Meieran, Eugene. Interview with author. June 23, 2010.
Niwa, Masaaki. Interview with author. June 7, 2016.
Oya, Yuichiro. Interview with author and Yashushi Sato. June 4, 2016.
Ross, Ian. *Oral history interview conducted by Lewis Terman*. August 19, 2009. Computer History Museum, Mountain View, CA.
Sello, Harry. Interview with author. June 6, 2012, and May 30, 2013.
Tarui, Yasuo. Interview with author and Yashushi Sato. May 31, 2016.
Toriumi, Akira. Interview with author. June 14, 2018.
Vadasz, Leslie. Interview with author. August 13, 2013.

Archival Sources

Andrew Grove Speeches, M1630, Stanford University Archives and Special Collections, Palo Alto, CA.
Donald Liddie Papers, X4609. 2008, Computer History Museum, Mountain View, CA.
Gordon Moore Papers, M1965, Stanford University Archives and Special Collections, Palo Alto, CA.

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