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A low-noise and flexible FPGA-based binary signal measurement generator

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Research Paper

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Abstract

In the area of electromagnetic metrology, binary coded excitation signals become more and more important and various binary coded sequences are available. The measurement approach is to assess the impulse response function of a device under test by correlating the response signal with the excitation signal. In order to achieve a high measurement reproducibility as well as a high dynamic range, the generated binary coded signals have to provide low-noise. In this contribution, a low-noise signal generator realized with a field programmable gate array is presented. The performance investigation of different kinds of binary coded excitation signals and different correlation concepts have been practically investigated. With a chip rate of 5 Gchip/s, the generator can be utilized for ultra-wideband applications. In order to allow for a low-noise and long-term stable signal generation, a new clock generator concept is presented and results of phase noise measurements are shown. Furthermore, an algorithm to fast and precisely shifting the time lag between two binary coded signals for correlating excitation and response signals with a hardware correlator is presented. Finally, the realized demonstrator system is tested using two commonly used types of binary coded sequences.

Introduction

For measuring the impulse response function (IRF) of a device under test (DUT), continuous binary coded excitation signals are often used. One reason is the high signal-to-noise ratio (SNR), because of the large signal energy of the continuous signal. Another reason is the relatively simple and cheap signal generation in digital electronics. An approximation of a delta-impulse shaped autocorrelation function (ACF) of the binary coded excitation signal is needed in order to obtain good results for the IRF. For this purpose, a variety of optimized binary sequences with different individual advantages and disadvantages are available. Maximum length sequences (MLS) can easily be generated by using a linear feedback shift register (LFSR) [1,2]. However, since dynamic range is linked to the sequence length for this type of sequence, a long MLS is needed to achieve a high dynamic range. Moreover, nonlinearities inside the measurement system lead to undesired peaks maxima in the IRF [3]. So-called almost perfect autocorrelation sequences (APAS) [4] are more robust against nonlinearities and are therefore a good alternative to MLS. However, APAS are more difficult to generate as compared to MLS. Besides the sequence itself, its correlation procedure is of major concern to obtain good results for the IRF of the DUT. This can be done in different ways. First, the response signal can directly be sampled and the correlation can efficiently be performed in software [5–7]. Nevertheless, even with a subsampling approach, a high speed and highly precise sample and hold stage is needed in this approach. Alternatively, the correlation can be performed completely in hardware [8]. However, the analog electronics has to fulfill high requirements regarding the linearity of a multiplier [9], and a highly precise integrator has to be used [10] to achieve a high dynamic range. We have shown that the integration can easily and precisely be performed in software [10]. Due to the lower hardware requirements resulting from the combination of hardware and software correlation, this is preferred and in the following referred to as hybrid correlation.

In this paper, a flexible binary coded signal generator based on a field programmable gate array (FPGA) is presented. The generator allows to generate arbitrary binary signals and to validate different correlation concepts by means of practical measurements. To achieve a high measurement rate with the hardware and the hybrid correlator, the time lag between the two generated signals has to be set fast and precisely. The algorithm to realize this inside the FPGA is a key component of the signal generator, as will be explained in more detail in the following. Furthermore, a clock synchronization has been implemented in order to reduce the noise of the generated signals. Generally, noise can be distinguished between amplitude noise and phase noise. In digital electronics amplitude noise is negligible and is therefore not considered in this paper. The realized clock generator provides a low phase noise and thus a low jitter, enabling a high dynamic range in systems where jitter is the limiting factor [9].

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Measurement results are presented that validate the performance of the new clock generator. Furthermore, time domain measurements have been performed in order to verify the fast and precise change of the time lag. MLS and APAS have been used for these measurements.

As an extension to our previous work [11], a complete measuring system based on the hybrid correlator achieving a high bandwidth is presented. Previously, the high frequency coded binary signals were sampled using an expensive high-speed digital storage oscilloscope (DSO) and the correlation has been performed in software. Furthermore, the new low-noise clock generator has several advantages over the previously used laboratory signal generators. The developed clock generator achieves a much lower jitter, which leads to a reduction of random errors. Since the dynamic range of the realized measurement system is limited by systematic errors inside the used multiplier, the advantage of the low jitter cannot be shown. Moreover, the developed clock generator achieves a long-term stable clock synchronization and thus enables long-term measurements, which was not possible with the realization presented in [11]. Additionally, the clock generator is much more compact making the measurement system mobile, more cost-effective and consumes less power.

Theoretical background

Binary sequences

Assuming a periodic binary sequence

$$s = s_0 s_1 \ldots\ldots s_{N-1}, \quad s_j \in \pm 1, \tag{1}$$

of length N. An MLS can be generated using an LFSR with a length of m bit, resulting in an odd sequence length

$$N_{\mathrm{MLS}} = 2^m - 1, \quad m \in \mathbb{N}. \tag{2}$$

A time continuous binary coded rectangular MLS signal $x(t)$ is shown in Fig. 1 (left). A finite sequence length N results in a code repetition period

$$T_{\mathrm{code}} = N \cdot T_{\mathrm{chip}}, \tag{3}$$

with the chip period T_{chip}.

The ACF

$$r_{xx}(\tau) = \int_{t_0}^{t_0 + M \cdot T_{\mathrm{code}}} x(t) \cdot x(t-\tau)\,\mathrm{d}t, \quad M \in \mathbb{N}, \tag{4}$$

of the binary coded signal $x(t)$ is a train of triangular pulsed signals with a full width at half maximum (FWHM) of approximately T_{chip}. Significant side maxima of the ACF $r_{xx}(\tau)$ are given, what limits the achievable dynamic range to

$$D_{\mathrm{MLS,max}}\big|_{\mathrm{dB}} = 20 \cdot \log_{10}(N_{\mathrm{MLS}}). \tag{5}$$

Since the level of the side maxima is constant, the resulting side maxima level of any IRF can be subtracted to avoid the mentioned limitation of the dynamic range. Because the level to be subtracted depends on the DUT, it must be determined inside a measured

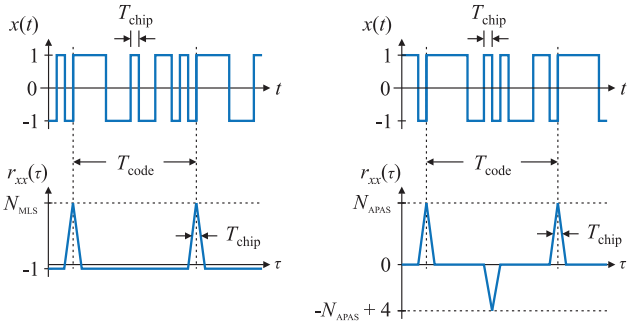

Fig. 1. Modulated periodic sequences $x(t)$ and their ACFs $r_{xx}(\tau)$ over time lag τ using an MLS of length $N_{\mathrm{MLS}} = 15$ (left) and an APAS of length $N_{\mathrm{APAS}} = 16$ (right).

IRF. Alternatively to MLS, APAS offer some advantages. An algorithm to calculate APAS is described in [4]. Each APAS has a length

$$N_{\mathrm{APAS}} = 2(q+1), \quad q = p^k, \tag{6}$$

where p is a prime number, k is a positive integer and q has to be odd. Consequently, N_{APAS} is in any case an integer multiple of four. In Fig. 1 (right), a binary coded APAS signal $x(t)$ and its ACF $r_{xx}(\tau)$ are shown exemplarily. Comparing the ACF of the APAS and the MLS, two differences can be seen: First, an additional inverted pulse at exactly half of the code repetition period T_{code}, which reduces the unambiguous range to $T_{\mathrm{code}}/2$. Accordingly, no side maxima appear at all. Under perfect conditions, the theoretical dynamic range is infinite:

$$D_{\mathrm{APAS,max}}\big|_{\mathrm{dB}} \to \infty. \tag{7}$$

Crosscorrelation principle

To determine the IRF $h(t)$ of the DUT using the binary coded excitation signal, a correlation has to be performed. In Fig. 2, an according measurement setup is shown. The approach behind the correlator can be represented by the crosscorrelation function (CCF)

$$r_{yx}(\tau) = \int_{t_0}^{t_0 + M \cdot T_{\mathrm{code}}} y(t) \cdot x(t-\tau)\,\mathrm{d}t, \quad M \in \mathbb{N}, \tag{8}$$

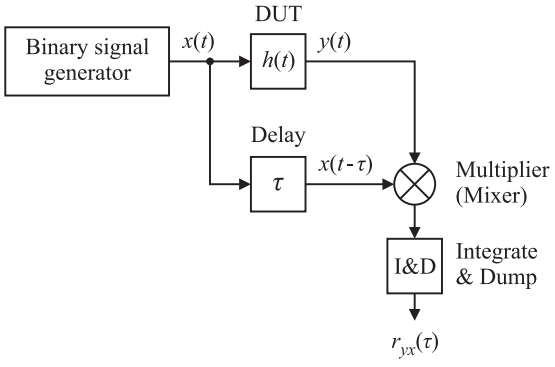

Fig. 2. Measurement system using the correlation principle.

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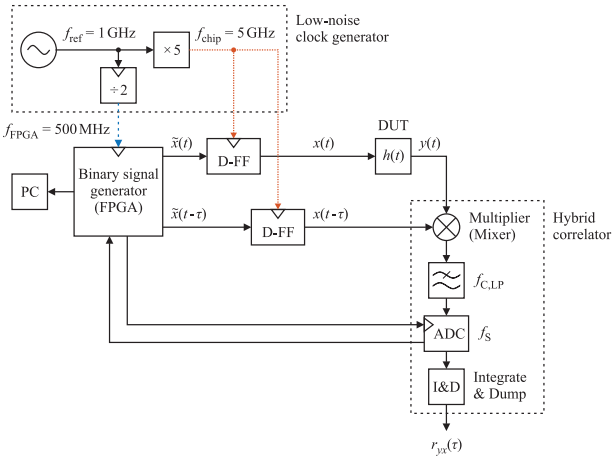

Fig. 3. Block diagram of the developed measurement system with the low-noise binary signal generator and hybrid correlator.

where the response signal $y(t) = h(t) * x(t)$ is correlated with the excitation signal $x(t)$. To achieve this, the excitation signal has to be time delayed by the time lag τ and multiplied with the response signal $y(t)$. Finally, an integration has to be performed for every time lag τ, which is referred to as integrate and dump (I&D) in Fig. 2. The integration time has to be an integer multiple of the repetition period T_{code} in order to achieve a high side maxima suppression. If the ACF of the excitation signal is a good approximation of the Kronecker delta function ($r_{xx}(\tau) \approx \delta(\tau)$), the CCF directly represents the IRF of the DUT [12]:

$$r_{yx}(\tau) = h(\tau) * r_{xx}(\tau) \approx h(\tau) * \delta(\tau) = h(\tau). \quad (9)$$

System overview

A block diagram of the developed measurement system is shown in Fig. 3. The goal of this measurement system is to achieve a high dynamic range and a high bandwidth. Generally, the dynamic range is limited by random errors as well as systematic errors. In the proposed measurement system random errors are given by the jitter of the signals $x(t)$ and $x(t-\tau)$ as well as the additive noise of the analog electronics inside the correlator. The resulting SNR increases by averaging several measurements and by increasing the sequence length N. Both result in a longer measurement time. Increasing the sequence length N is preferably used here, because, especially in case of APAS, it results in an increased robustness against nonlinear distortions inside the measurement system [9]. Additionally, the SNR can be increased by decreasing noise inside the measurement system. Systematic errors inside analog electronics, for example linear and nonlinear distortions, are unavoidable. Where linear errors can easily be corrected by applying a calibration, non-linear errors lead to a degradation of the dynamic range, because, in the case of MLS, discrete peaks appear in the ACF and can be mistakenly interpreted as ghost targets [3] and in case of the APAS, nonlinearities lead to an almost constant increase of the side maxima level [3]. This side maxima level can be decreased by increasing the sequence length N. In the proposed measurement system, nonlinearities are mainly caused by the analog multiplier inside the correlator. Other systematic errors, for example a bit error in the code sequence, would also increase the side maxima level and consequently limit the achievable dynamic range. The focus of this paper is on the generation of the two signals $x(t)$ and $x(t-\tau)$ with a small jitter and a high chip rate, allowing also for a large sequence length. Binary coded signals are generated with a chip rate of 5 Gchip/s using a *Cyclone V GT* (Intel, Santa Clara, USA) FPGA. Achieving a short measurement time, the time lag τ has to be changed fast within one chip period $T_{chip} = 200$ ps [10]. A solution for this challenging task is presented in the section "Low-noise binary signal generator". The step size of the time lags results in an effective high-frequency sampling rate of $1/T_{chip} = 5$ GHz. Thus, due to the Nyquist-Shannon sampling theorem, the bandwidth of the response signal $y(t)$ has to be limited to 2.5 GHz. If this is not guaranteed by the DUT, a low pass filter has to be added. High-speed transceivers inside the used FPGA offer a high chip rate and are typically used for high-speed data transmission. Unfortunately, the jitter of transceiver output signals is relatively high (typically 2 ps). For applications requiring a high dynamic range larger than 90 dB, the jitter has to be smaller than 200 fs when an APAS with a length $N_{APAS} = 64{,}320$ is used [9]. Crosstalk inside the FPGA and the printed circuit board (PCB) further limits the dynamic range. In order to reduce the jitter of the generated signals and to suppress crosstalk, a clock synchronization technique using D flip-flops (D-FF) and a low-noise clock generator has been implemented. Since the D-FF are triggered by the low-noise clock, only the logically state (low or high) of the FPGA output signals $\tilde{x}(t)$ and $\tilde{x}(t-\tau)$ at the data inputs of the two D-FF is important. The resulting jitter of the D-FF output signals $x(t)$ and $x(t-\tau)$ only depends on the jitter of the low-noise clock generator and the additive jitter of the D-FF, which is typically negligible. Additionally, disturbing signals, for example caused by crosstalk, are strongly suppressed. For the stable clock synchronization, the chip rate f_{chip} synthesized inside the FPGA using a phase-locked loop (PLL) has to be exactly the same as the chip rate generated by the low-noise clock generator. This is ensured by using the same reference oscillator.

We have already previously used this concept of clock synchronization [11]. However, the FPGA clock frequency f_{FPGA} as well as the chip clock frequency f_{chip} were generated using two laboratory signal generators *SME06* and *SMR40* (Rohde & Schwarz, Munich, Germany) respectively, sharing the same 10 MHz reference oscillator. Inside the generators, PLL concepts are used to achieve a high output frequency. Due to the relatively low reference frequency, high divider factors inside the PLL have to be used, which increase the noise transfer from the PLL components to the output [13]. Furthermore, the high thermal capacity of the laboratory signal generators leads to a long-term phase drift between the FPGA clock and the clock of the D-FF. Thus, within the long warm-up time of the laboratory signal generators of about 2 hours, the clock synchronization is unstable. Even long-term drifts could be observed, which do not allow for stable measurements over several hours without adjusting the relative phase position.

For a stable clock synchronization, the phase drift between the FPGA clock and the clock of the D-FF has to be below $T_{chip} = 200$ ps. Furthermore, a small jitter of < 200 fs has to be guaranteed to allow for a high dynamic range without averaging. For a temperature-stable clock frequency, a crystal-controlled oscillator (XCO) is a good option as a reference oscillator. An XCO with additional oven-controlled temperature (OCXO) and integrated frequency multiplier with an output frequency of 1 GHz is available for a reasonable price and used here as a

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reference oscillator. To increase the clock frequency to the required $f_{chip} = 5$ GHz, the following two concepts could be used: First, the frequency synthesis by a PLL, secondly, the generation of harmonics by a nonlinear network. The PLL concept uses a temperature-unstable high-frequency oscillator whose phase is related to a temperature-stable low-frequency oscillator. Various concepts for the realization of high-frequency oscillators are available. Yttrium iron garnet-based (YIG) oscillators provide a wide frequency tuning range while maintaining a good quality factor. Since a frequency tuning is not necessary for the measurement system presented here, a dielectric resonator oscillator (DRO) with a very small tuning range and very high-quality factor would be more appropriate. Nevertheless, both types of oscillators require a relatively complex mechanical construction. Alternatively, a voltage controlled oscillators (VCO) realized within an integrated circuit could be used. However, the quality factor is lower and consequently the jitter is higher as compared to the YIG and DRO oscillators. Besides the mentioned oscillators, further electronic circuits (frequency divider, phase detector, loop filter) are required to realize a PLL. For the system realized here, a nonlinear electronic circuit is used to generate harmonics. Subsequently, the desired fifth harmonic is filtered out by using a bandpass filter. A high-quality filter with a large stopband attenuation is required in order to suppress the undesired harmonics. In addition, compared to the above-mentioned laboratory signal generators, the jitter is lower, it is more compact, cost-effective and consumes less power.

The FPGA reference clock at $f_{FPGA} = 500$ MHz could be derived from the chip clock with $f_{chip} = 5$ GHz using a ÷ 10 divider. However, since a reference clock with $f_{ref} = 1$ GHz is available, a ÷ 2 divider is used, see Fig. 3, which also has even lower requirements for its maximum input clock frequency. The concept and realization of the low-noise clock generator is explained in detail in the section "Low-noise clock generator".

In the proposed measurement system, shown in Fig. 3, the correlation is performed partly in hardware (time lag and multiplication) and partly in software (precise integration). Thus, no analog integrator is necessary. In addition, the requirements for the sample and hold stage of the analog-to-digital converter (ADC) are low as the mixing and low pass filtering significantly reduces the bandwidth of the signal to be sampled [10]. For the precise integration over one code repetition period T_{code} or integer multiples thereof, the sampling rate f_s has to be an integer multiple N_{sample} of the code repetition frequency:

$$f_s = \frac{N_{sample}}{T_{code}} = \frac{N_{sample} \cdot f_{chip}}{N}. \quad (10)$$

The ADC has a maximum sampling rate of 5 MHz. In case of an APAS with a length $N = 64{,}320$, for example, $N_{sample} = 64$ is set resulting in a sampling rate $f_s \approx 4.98$ MHz.

Low-noise clock generator

Concept

In Fig. 4, a block diagram of the proposed low-noise clock generator including the FPGA and a 10 MHz clock outputs, is shown. The used components are listed in Table 1. As reference signal, a low-noise 1 GHz high-frequency oven-controlled crystal oscillator (OCXO) with a measured output power of approximately 12 dBm into a 50 Ω load is used. The low clock

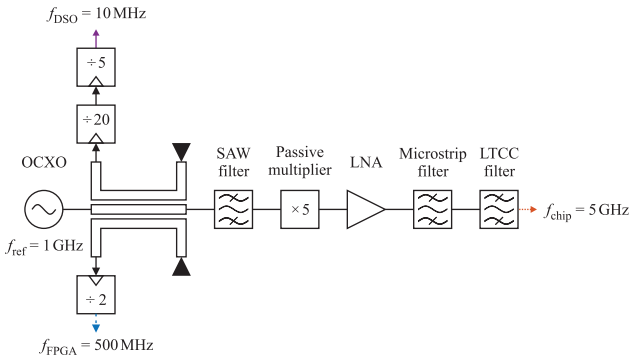

Fig. 4. Block diagram of the developed low-noise chip clock generator with additional divider providing low frequency clocks.

frequencies, $f_{FPGA} = 500$ MHz for the FPGA and $f_{DSO} = 10$ MHz for a DSO, used for additional time domain measurements in the section "Low-noise binary signal generator", are derived from the OCXO using low-noise frequency dividers. This keeps the requirements for the maximum input frequency of the frequency dividers low. The minimum recommended input power of the divider *HMC394* is only − 15 dBm allowing to use a double microstrip coupler with a small coupling factor of approximately − 18 dB and a small insertion loss of approximately only − 0.34 dB. As a consequence, a sufficiently large signal level for the frequency multiplier is available. The spectrum of the OCXO output shows significant spurious at every integer multiple of 100 MHz. To suppress the spurious, a surface acoustic wave (SAW) band pass filter with a small − 3 dB bandwidth of 48 MHz is used. After passing the SAW filter, the required input level range of the passive × 5 multiplier is directly available with no need for further attenuation or amplification. Because the multiplier is a passive device, the conversion loss is larger than 25 dB. Spectral components at odd integer multiples of 1 GHz have similar power levels. A designed 4th-order microstrip band pass filter with a center frequency of approximately 5 GHz and a − 3 dB bandwidth of approximately 300 MHz in combination with a low temperature cofired ceramic (LTCC) band pass filter is used to suppress the unwanted spectral components. Due to the high conversion loss of the multiplier and the attenuation of the band pass filters, a low-noise amplifier (LNA) is used to increase the signal level. The LNA is placed right after the passive

Table 1. Components used for the proposed low-noise clock generator.

Component	Part number	Manufacturer
OCXO	*O-CEGM*	NEL Frequency Controls, INC. Burlington, USA
SAW filter	*TA0820A*	Golledge Electronics Ltd. Ilminster, UK
× 5 multiplier	*RMK-5-83+*	Mini-Circuits Brooklyn, USA
LNA	*PMA3-83LN+*	Mini-Circuits Brooklyn, USA
LTCC filter	*BFCN-4800+*	Mini-Circuits Brooklyn, USA
÷ 2 divider	*HMC394*	Analog Devices Norwood, USA
÷ 20 divider	*HMC394*	Analog Devices Norwood, USA
÷ 5 divider	*HMC438*	Analog Devices Norwood, USA

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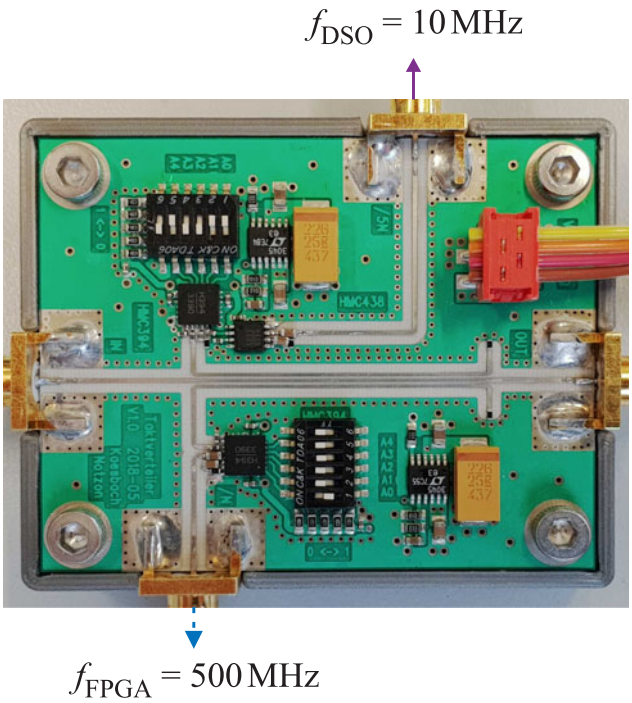

Fig. 5. Photo of the realized coupler and frequency dividers.

multiplier to avoid a degradation of the phase noise due to the noise floor and the attenuation of the filters.

Realization

In Fig. 5, a photo of the realized PCB including the coupler and the frequency divider is shown. A low-loss *RO4003C* (Rogers Corporation, Chandler, USA) substrate material (0.2 mm thickness) has been used and mechanically stabilized by a 3D printed frame. The division factor of the *HMC394* can actually be changed between 2 and 32 by means of onboard switches. In Fig. 6, a photo of the realized × 5 multiplier with filters and amplifier, which has been realized using the same substrate material, is shown. Sub-miniature-A (SMA) connectors are used to flexibly interface the components and the further test equipment.

Measurement results

To verify the functionality of the × 5 multiplier, in a first step, the output spectrum was measured using an *FSWP* (Rohde & Schwarz, Munich, Germany), see Fig. 7. At $f_{chip} = 5$ GHz, a large spectral line with the largest power level of approximately − 6.8 dBm can be seen. This level is large enough to trigger the used D-FF *HMC723LP3E* (Analog Devices, Norwood, USA) even behind a − 6 dB power divider. Spurious lines at integer

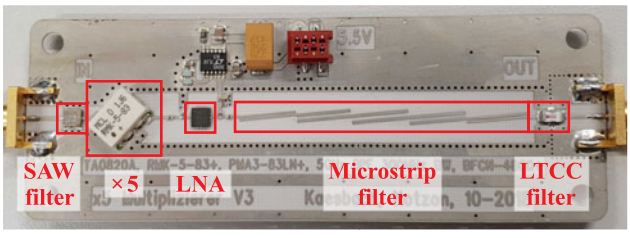

Fig. 6. Photo of the realized × 5 multiplier.

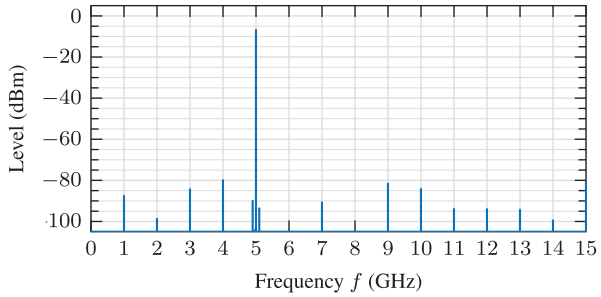

Fig. 7. Measured frequency spectrum of the × 5 multiplier output.

multiples of the reference frequency $f_{ref} = 1$ GHz and the transformed spurious of the OCXO at integer multiples of 100 MHz, on the other hand, are strongly suppressed.

In another step, phase noise measurements using the *FSWP* have been performed, to quantify the jitter. The measured raw data were processed by using a spurious reduction and smoothing algorithm. Fig. 8 shows the single side band phase noise L_{dB} as a function of the offset frequency f_{os}. For a frequency multiplication by a factor of five, a 20 dB log (5) ≈ 14 dB increase of the phase noise is expected [14]. The measured phase noise at the output of the proposed × 5 multiplier output, using the 1 GHz OCXO as the reference, fits well with this theoretical expectation. The band pass filters even decrease the phase noise for offset frequencies down to approximately 10 MHz. In comparison to the laboratory signal generator *SMR40*, with a comparable output power level of − 5 dBm, the phase noise of the proposed × 5 multiplier is much lower except in the range from 1.5 MHz to 27.5 MHz. The standard deviation t_j of the jitter was calculated from the measured phase noise by using the following relationship [15]:

$$t_j = \frac{\sqrt{2\int_{f_l}^{f_u} L(f_{os})\,df_{os}}}{2\pi f_c}, \quad \text{with } L(f_{os}) = 10^{L_{dB}(f_{os})/10}. \tag{11}$$

The lower and upper limits f_l and f_u, respectively, of the relevant frequency range have to be specified for calculating t_j. The lower limit f_l depends on the measurement time and the upper limit f_u depends on the receiver bandwidth. Furthermore, the DUT can further limit the bandwidth and accordingly the integration

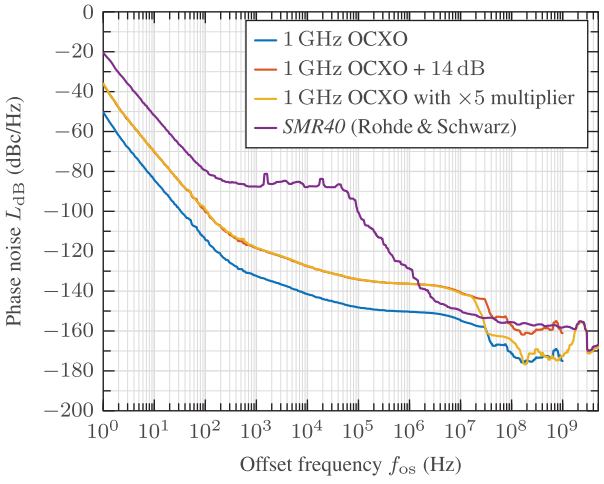

Fig. 8. Measured phase noise.

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interval in (11). Exemplary, for $f_l = 1$ kHz and $f_u = 2$ GHz, a jitter $t_{j,\times 5} \approx 24.3$ fs for the $\times 5$ multiplier and a larger jitter $t_{j,SMR40} \approx 520.2$ fs for the *SMR40* laboratory signal generator are given.

Low-noise binary signal generator

Hardware realization using an FPGA

For the realization of the signal generator, a *Cyclone V GT FPGA Development Board* (Intel, Santa Clara, USA) has been used. This FPGA offers a number of 12 onboard transmitters with a maximum clock rate of 5 Gchip/s. Fig. 9 shows a block diagram of the developed FPGA system. To allow for the high chip frequency $f_{chip} = 5$ GHz, an integrated PLL is used to multiply the FPGA clock frequency f_{FPGA}. Onboard serializers convert a 40 bit parallel data stream into a serial one, what reduces the internal FPGA clock frequency by a factor of 40 to 125 MHz. In the proposed design, actually four of the available transmitters are used. To feed the corresponding serializers, the data are calculated by four different algorithms, see Fig. 9, which are presented below.

The unshifted sequence algorithm continuously repeats the desired excitation sequence, and the shifted sequence algorithm outputs a second sequence with a circular shift relative to the first one. The accordingly realizable time lags are set in steps of the chip period $T_{chip} = 200$ ps in the digital electronics. The shifted and unshifted sequence algorithms are using independent memory blocks inside the FPGA, which increases the flexibility for generating different types of sequences. Although both algorithms were kept as short as possible, the worst-case propagation delay on the FPGA is approximately 11 ns. Since this is too large for the short clock period of 8 ns, the algorithms are working at half the clock frequency. To achieve the required data throughput under this condition, a factor two larger number of 80 bit is processed in each clock period. Despite this concept, the additional increase of overall propagation delay is still sufficiently small. To be able to feed the serializers, a multiplexer (MUX) inside the FPGA is used to finally reduce the bus width to the required 40 bit.

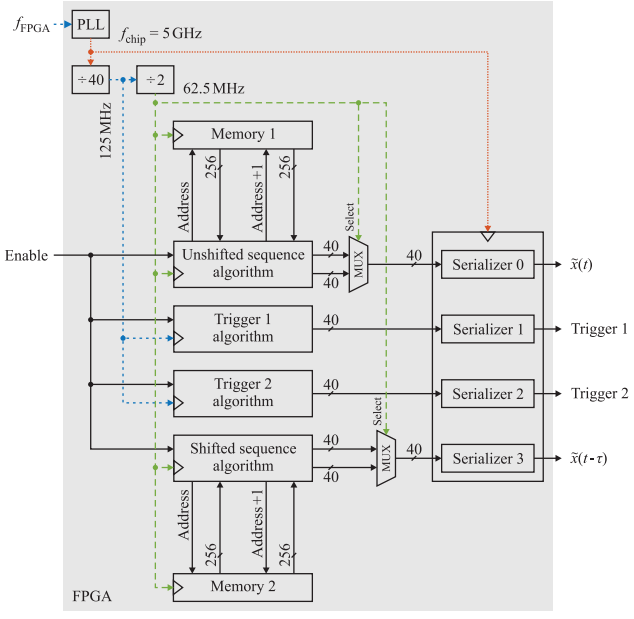

Fig. 9. Block diagram of the developed FPGA system.

Algorithm 1 Shifted sequence with example values.

Initialization:
  $N = 7$, $N_{shifts} = 7$, $W_{mem} = 4$, $W_{cache} = 3$
  $n_{out} = k = r = n_{shift} = p_{shift} = 0$
  $cache(0 \ldots W_{cache} - 1)$
if Rising edge on input clock **then**
  Read data from memory and update *cache*
  $n_{out} \leftarrow n_{out} + 1$
  $k \leftarrow r + n_{out} \cdot W_{cache} - N$
  if $k \geq 0$ **then**
    $r \leftarrow k$
    $n_{shift} \leftarrow n_{shift} + 1$
    if $n_{shift} = N_{shifts}$ **then**
      $n_{shift} \leftarrow 0$
    end if
    $p_{shift} \leftarrow N + r - n_{shift}$
    if $k > 0$ **then**
      Rearrange *cache* as follows:
      $cache(W_{cache} - r$ to $W_{cache} - 1) \leftarrow$
      $cache(W_{cache} - r - 1$ to $W_{cache} - 2)$
    end if
  end if
  Update memory address and cache position
  return *cache*
end if

The shifted sequence algorithm is described in the form of a pseudocode in Algorithm 1. During initialization, the sequence length N, the number of shifts N_{shifts} to be performed, the memory block width W_{mem}, and the *cache* width W_{cache} are predefined. In the realized system, $W_{mem} = 256$ and $W_{cache} = 80$ are given. For a better understanding some iterations of the algorithm, with $N = N_{shift} = 7$, $W_{mem} = 4$, and $W_{cache} = 3$ as an example, are shown in Fig. 10 and are explained below in some more detail. In the left part of Fig. 10, the numerical values of the five variables (n_{out}, k, r, n_{shift}, p_{shift}) at the end of each iteration are given. In the upper part, a periodically stored sequence $s = s_0 \ldots s_6$ with a length $N = 7$ in memory 2 is shown. In the right part of Fig. 10, the black-rimmed *cache* content, with the result of the calculations, is given for each iteration. The beginning of a circularly shifted sequence is marked with a black background and the end is marked with a gray background. In the first two iterations, the

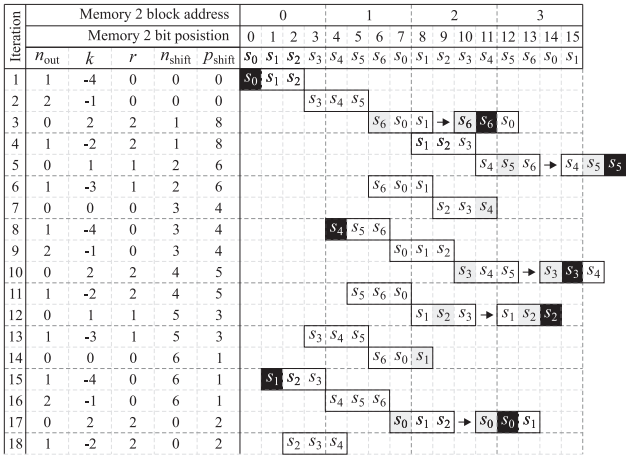

Fig. 10. Numerical example of the shifted sequence algorithm.

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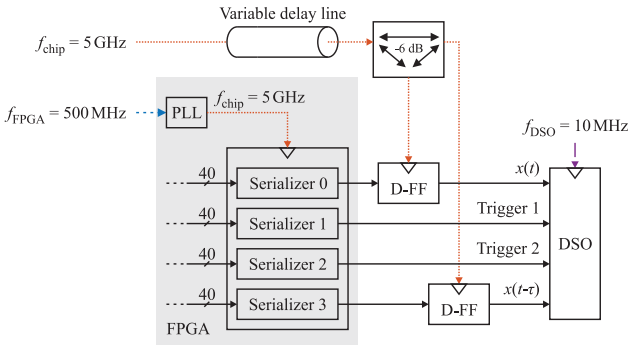

Fig. 11. Block diagram of the measurement setup.

cache is filled stepwise with the content stored in the memory 2. If the end of the sequence is reached ($k \geq 0$), a circular shift operation is performed. The idea behind this algorithm is to rearrange the *cache* content, as is indicated by arrows in Fig. 10. If a shift occurred, the readout of memory 2 continues at bit position p_{shift}. If $k = 0$, which happens for example at iteration 7, no *cache* rearrangement has to be performed. For achieving a high dynamic range, a long sequence length N is required, resulting in a long measurement time. If the IRF of a DUT is significantly shorter than the unambiguous range given by the selected code sequence, the measurement time can be decreased by performing only the necessary number of shifts. In the presented algorithm, in addition, to perform all possible number of shifts ($N_{shifts} = N$), as was done in the example here, the number of shifts N_{shifts} can be reduced to any integer multiple of the *cache* width W_{cache} where no cache rearrangement is performed ($k = 0$), in order to decrease the measurement time.

For the correlator concept proposed in the section "System overview", the low pass filter, see Fig. 3, has to be able to settle after each shift operation [10]. Thus, the sequence is sent twice for each cyclic shift. This is realized by simply repeating the sequence once and by specifying its length twice as long as it actually is. Sometimes, the *cache* requires content from two adjacent memory blocks right after a shift has been performed, see iteration 6 in Fig. 10. The utilized *Cyclone V GT* FPGA allows a parallel memory block readout at two independent addresses. This is used here to be always able to readout two adjacent memory blocks, allowing it to keep the algorithm simple and fast.

The algorithm for the unshifted sequence can easily be derived from the shifted sequence algorithm and is much simpler, because no *cache* rearrangement has to be performed and no shift counter n_{shift} is needed. At the end of the sequence, p_{shift} is set to k.

In addition to the sequence algorithms, two different trigger algorithms were developed. Trigger 1 indicates the start of a measurement ($\tau = 0$) and trigger 2 indicates a shift in time lag τ. In order to synchronize all four algorithms, they get the same enable signal.

Measurement setup

Figure 11 shows a block diagram of the realized measurement setup. The low-noise clock generator described in the section "Low-noise clock generator" is used here to synthesize the low-noise chip clock, the FPGA clock, and the DSO clock. The generated unshifted signal $\tilde{x}(t)$ and the shifted signal $\tilde{x}(t - \tau)$ are clock synchronized to the low-noise chip clock. A − 6 dB power divider is used to distribute the low-noise chip clock signal. The utilized D-FF allow for a chip rate up to 13 Gchip/s, and the single-ended output voltage swing of ± 300 mV results in an output level of approximately 2.6 dBm into a 50 Ω load. In addition, the phase difference between the clock inputs of the two D-FF is adjusted once by using a variable delay line to ensure a stable time shift between clock and data input.

In Fig. 12, a photo of the realized measurement setup is shown. An adapter card *XTS-HSMC* (Terasic, Hsinchu City, Taiwan) is used to connect the transmitters of the FPGA to SMA connectors and cables. Furthermore, the two D-FF have been shielded by using separate metallic boxes to minimize crosstalk.

Measurement results

For sampling the time-domain signals $x(t)$ and $x(t - \tau)$, a high-speed DSO *RTO1044* (Rohde & Schwarz, Munich, Germany) with an input bandwidth of 4 GHz and a sampling rate of 20 GSPS was used. With the realized low-noise and flexible binary

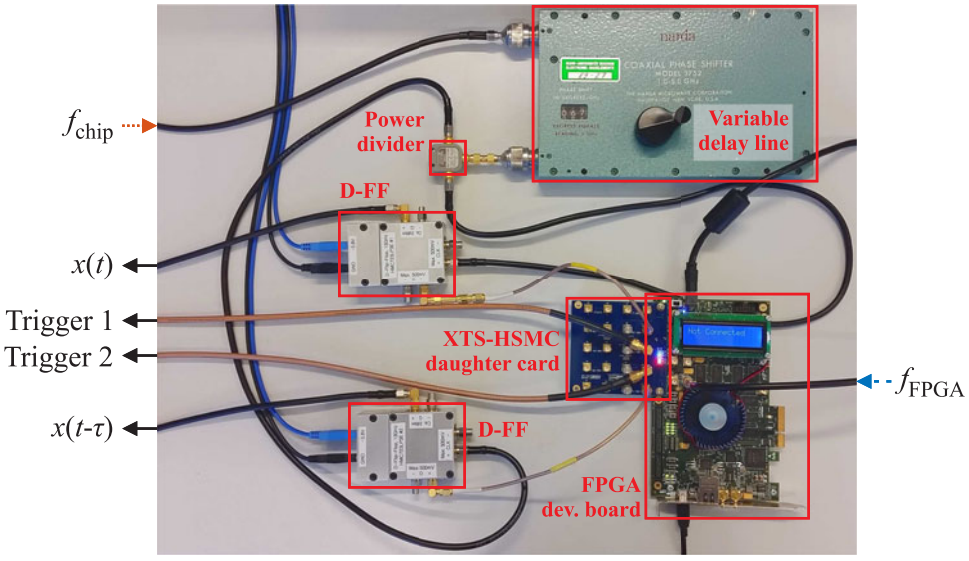

Fig. 12. Photo of the measurement setup.

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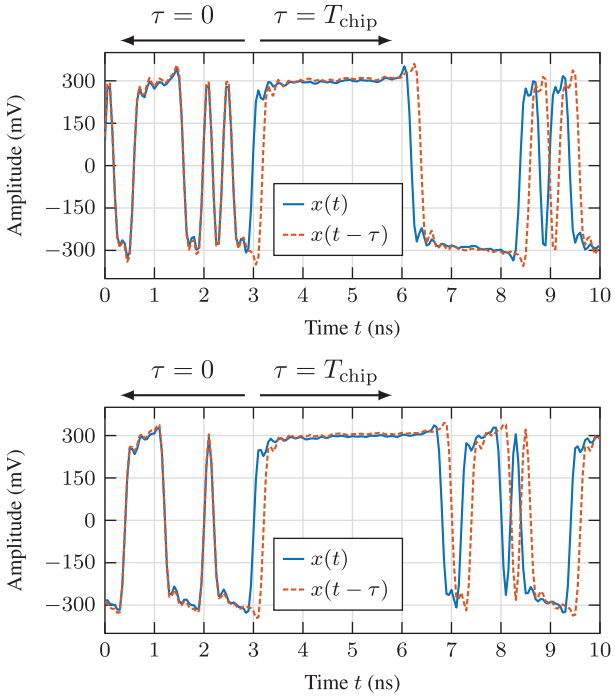

Fig. 13. Sections of the measured signals $x(t)$ and $x(t-\tau)$ using an MLS of length $N_{\mathrm{MLS}} = 65{,}535$ (top) and an APAS of length $N_{\mathrm{APAS}} = 64{,}320$ (bottom).

signal generator different kinds of sequences can easily be synthesized and tested. For demonstration purpose, an MLS with a large length $N_{\mathrm{MLS}} = 65{,}535$ and an APAS with a similar length $N_{\mathrm{APAS}} = 64{,}320$ have been implemented. Sections of both signals with stepwise changed time lags τ from zero to $T_{\mathrm{chip}} = 200$ ps are shown in Fig. 13. In order to decrease the noise of the DSO, 100 measurements were averaged. Both types of sequence, the MLS in Fig. 13 (top) and the APAS (bottom), clearly show the intended and programmed change of the time τ from zero to T_{chip} at the time instance $t = 3$ ns. Because of the limiting bandwidth of the DSO, the actually shown slew rate of the D-FF is smaller than the actually given one.

For another measurement, the proposed hybrid correlator, shown in Fig. 3, instead of the DSO has been used. A through connection has been used as ideal DUT and the bandwidth of the response signal was not limited to 2.5 GHz for the measurement ($y(t) = x(t)$), in order to directly assess the ACF. Sections of the measured ACF obtained with the same two sequences as above are shown in Fig. 14. To compensate the constant side

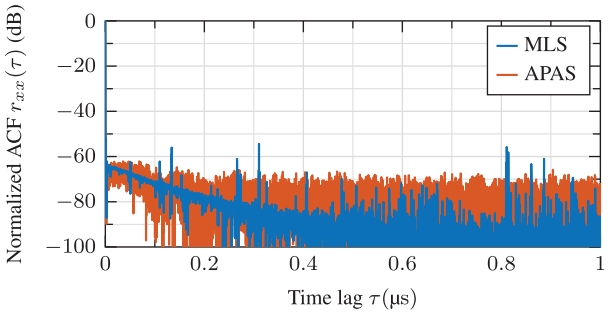

Fig. 14. Sections of the measured ACF $r_{xx}(\tau)$ using an MLS of length $N_{\mathrm{MLS}} = 65{,}535$ and an APAS of length $N_{\mathrm{APAS}} = 64{,}320$.

maxima level of the MLS and the additional DC-level caused by the analog electronics, the mean value of the ACF was calculated in the range $0.6\,\mu\mathrm{s} \leq \tau \leq 1\,\mu\mathrm{s}$ and then subtracted from the ACF in the whole range $\tau \leq 1\,\mu$s. For the MLS, nonlinearities inside the system lead to multiple time-delayed and attenuated MLS, which appear as discrete peaks in the ACF [3] and strongly decrease the achieved dynamic range to approximately 54 dB. In the case of the APAS, nonlinearities also lead to a degradation of the correlation properties. Instead of discrete peaks, the side maxima level is almost evenly increased [3]. Thus, a dynamic range of approximately 65 dB has been achieved.

We have already previously measured the ACF [11]. But instead of the hybrid correlator approach, we have sampled the high-frequency signals $x(t)$ and $x(t-\tau)$ using the relatively expensive DSO *RTO1044* and performed the correlation in software. We have shown that a dynamic range of at least 90 dB can be achieved using the proposed binary coded signal generator.

The limitations by measuring the ACF with the hybrid correlator are due to the nonlinearities inside the mixer *SYM-63LH+* (Mini-Circuits, Brooklyn, USA) used for multiplying the signals in hardware. A compensation of these nonlinearities is challenging, because their impacts on a measured IRF depends on the DUT behavior. Furthermore, a high pass characteristic of the baluns, which are included in the mixer, further limit the dynamic range for $\tau < 0.1\,\mu$s. A further optimization of the proposed correlator regarding the linearity has to be done in order to take advantage of the presented low-noise binary signal generator. This is currently under investigation.

Conclusion

In this contribution, a flexible and low-noise binary coded signal generator based on an FPGA was presented. A clock generator with low-noise was realized and validated by means of phase noise measurements. A small jitter $t_{\mathrm{j},\times 5} \approx 24.3$ fs within an integration range from 1 kHz to 2 GHz could be achieved. This generator allows for a low-noise and long-term stable signal generation. Furthermore, an algorithm for fast and precise shifting of the time lag between two binary coded signals was shown, which allows for correlating excitation and response signals in the proposed hybrid correlator. Finally, the realized demonstrator system has been tested using two commonly used types of binary coded sequences, the maximum length sequence and the almost perfect autocorrelation sequence.

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