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Design and evaluation of 20-GHz power amplifiers in 130-nm CMOS

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The use of 130-nm CMOS for power amplifiers at 20 GHz is explored through a set of power amplifiers as well as transistor level measurements. The power amplifiers explore single versus cascode configuration, smaller versus larger transistor sizes, and the combination of two amplifiers using power splitters/combiners. A maximum output power of 63 mW at 20 GHz was achieved. Transistor-level characterization using load pull measurements on 1-mm gate width transistors yielded 148-mW/mm output power. Transistor modeling and layout for power amplifiers are also discussed. An estimate on the maximum achievable output at 20 GHz from 130-nm CMOS power amplifiers, based on findings in this paper and the literature, is finally presented.

Keywords: CMOS, 130 nm, K-band, MMIC, Power amplifier

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I. INTRODUCTION

Due to the down-scaling and resulting high transit frequencies, CMOS is becoming a realistic alternative to III–V technologies for microwave applications, also at higher frequencies than today's commercial applications in the lower GHz-region. Several successful design examples well up into the V-band have been published, e.g. [1–4]. Surprisingly, little has however been reported regarding CMOS power amplifiers at frequencies above 10 GHz. The results by Ferndahl *et al.* [5] represent highest power, with 18.3-dBm output at 20 GHz, whereas LaRocca and Chang [6] with 12.2 dBm at 60 GHz represent highest power combined with high frequency. Investigations on device level have also been carried out by Scholvin *et al.* [7] and Ferndahl *et al.* [8, 9].

While the short channel lengths have enabled excellent small-signal high-frequency performance, it has also led to lower breakdown voltages and thus a smaller tolerable RF voltage swing. As a result the maximum output power is reduced and the design of CMOS power amplifiers becomes challenging. Hence, there is a need to study CMOS power amplifiers above 10 GHz to understand how, e.g., higher output power can be achieved.

This paper reports a study of power amplification at 20 GHz in 130-nm CMOS technology. The presented findings are based on both large signal transistor measurements and five different power amplifier designs, exploring different transistor types, single transistor versus cascode, combining power amplifiers as well as the effect of total transistor gate width.

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Furthermore, the modeling of the transistors, using RF extension to the intrinsic model, is presented as well as the modeling of the passive components in the matching network.

The paper is organized as follows. Section II explains the modeling of the transistors and passive components. In Section III the result of small and large signal measurements of several different transistor layouts and types are presented. The circuit design is covered in Section IV and results in Section V. Comparisons and conclusions are made in Sections VI and VII, respectively.

II. MODELING

The available transistor model for the used process is based on the BSIM4 model, with some extensions of library cells to handle the layout parasitics up to the polysilicon/metal 1 layers. To include the effects of the metal interconnects up to the top metal layer, series resistances and inductances were added to all three terminals (gate, drain, source), see Fig. 1(a). The bulk terminal was connected directly to the source terminal.

Before the extraction of the parameter values for the RF extension the measured *S*-parameter data was de-embedded to remove the influence of pad capacitance and access lines in the test structure, see Fig. 1(b). The pads and access lines to the device are thus not part of the RF extension. A statistical equivalent-circuit-based de-embedding procedure was used [10] with the package model shown in Fig. 1(b).

The parameter values of the RF extension, describing the parasitics upto the top metal layer, there the transmission lines are connected, to the polysilicon/metal 1 layer, were then found through a multi-bias optimization using measured extrinsic (de-embedded) data and simulated intrinsic data.

Standard transmission lines models were used with parameters based on process information such as substrate thickness and conductivity. These models were also validated using 2.5D EM simulations and found sufficiently accurate, at these

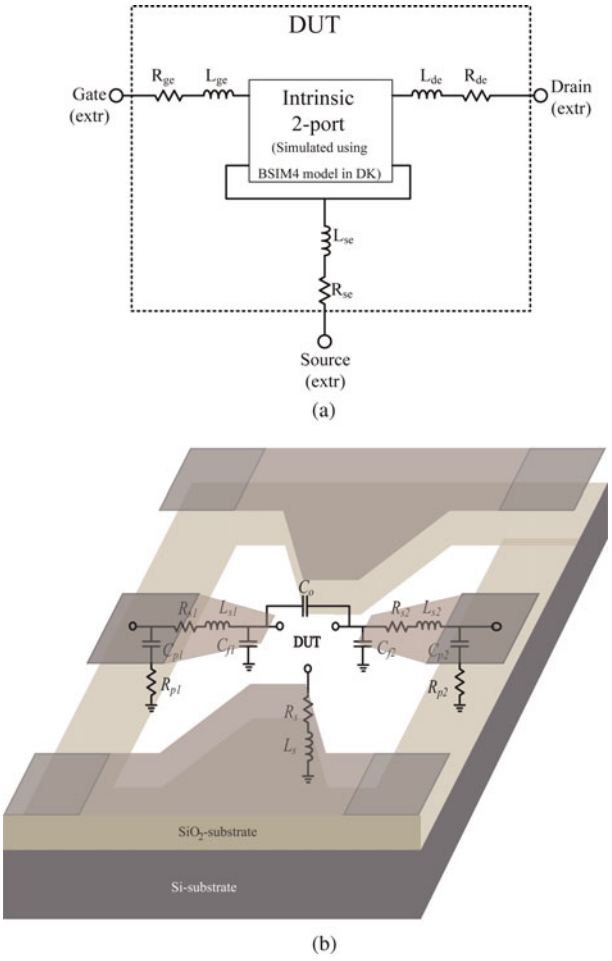

Fig. 1. (a) Intrinsic BSIM4 model with RF extension. (b) Layout of transistor test structure with package model of pad capacitances and access lines overlayed used in the de-embedding.

frequencies. The models for the input and output pad capacitance were taken from the de-embedding data, using an RC series network, i.e. C_{p1} and R_{p1} in Fig. 1(b).

III. EVALUATION OF 130-NM CMOS FOR 20 GHZ POWER AMPLIFIERS

To evaluate 130-nm CMOS as a technology for power amplification around 20 GHz, several devices were fabricated and measured to evaluate their performances. The measurements were carried out in two steps. First bias dependent small signal measurements were performed, using a network analyzer up to 50 GHz to find the available gain at 20 GHz and also extract the parameter values for the RF extension mentioned in Section II. The most promising devices were then measured in a large signal setup to find their maximum output power and their corresponding optimal input and output impedance levels using load and source pull with impedance tuners.

At lower frequencies it is quite common to use I/O transistors with thicker oxide and longer gate lengths as they allow a higher drain voltage supply and therefore can deliver more output power at a higher impedance level. Therefore, I/O transistors were measured and compared to regular transistors with minimum gate length having nominal oxide thickness. The gain of the I/O transistors were, however, too low at these

Table 1. Comparison between different device options in a 130-NM RF-CMOS process*.

Device	V_{dd} (V)	*fmax* (GHz)	ft (GHz)	$G_{m,max}$ (mS/mm)	$I_{d,sat}$ (mA/mm)
I/O†	1.5	30	22	150	210
Regular‡	1.5	50	65	350	490

*Transistor gate width 10 μm × 100 fingers (not optimized for maximum gain).
†Thick gate oxide and larger gate length.
‡Thin gate oxide and minimum gate length.

frequencies, i.e. above 10 GHz, to be usable in a power amplifier design, and regular transistors had to be used, see Table 1.

The regular transistor, with minimum gate length, was designed with different layouts, having 1-mm total gate width and varying unit gate finger width, from 5 μm and up. This in order to find an optimum in terms of both gain, output power, and reliability. The layout of large transistor cells for power amplification at high frequencies, about a fifth of f_T, is problematic from two aspects. First, the gate finger width should be kept short enough to have sufficient gain, since the high gate resistance from a wide gate finger transistor will deteriorate the high-frequency performance. The second issue is how to layout a multi-finger transistor to avoid problems with electromigration and reliability due to the large drain/source currents, this while keeping the parasitic capacitances and resistances as low as possible. For example the source return path, drawn above the drain and gate connection, was too narrow in the 5 μm × 200 finger transistor layout with almost immediate degradation during large signal measurements. A unit gate finger width of 10 μm gave satisfactory performance in terms of both gain and metal current density-related reliability. The resulting measured maximum output power, gain, and power-added efficiency (PAE) for the 100 fingers × 10 μm device are shown in Fig. 2. The maximum achieved output power density at 3-dB compression was 148 mW/mm with a maximum PAE of 20%. To the authors' knowledge this is the highest reported output power density for CMOS at these frequencies. The gain of the 1-mm device was, however, too low (5 dB) and smaller transistor

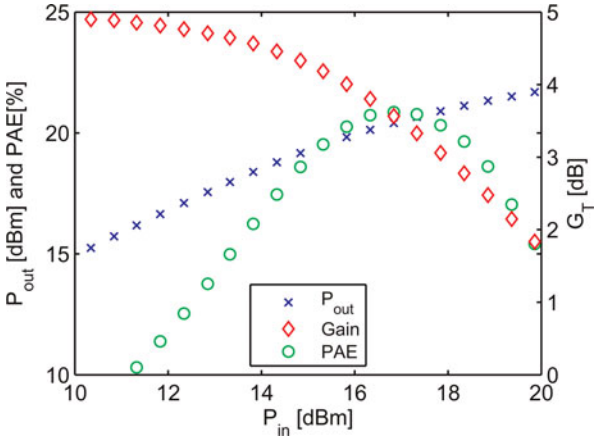

Fig. 2. Measured transducer gain, output power and PAE from load pull characterization of a 1-mm gate width 130 nm CMOS at 23 GHz. Source and load impedance were optimized for maximum output power (Z_S = 9–0.13, Z_L = 9.2–0.16).

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sizes (200 and 500 μm total gate width) were chosen for the power amplifier designs. Two sizes were chosen to be able to obtain insight on the effect of device size in the amplifier design. The transistors were also put in a cascode configuration. As the supply voltage in the cascode cell is partitioned between the input and the output/common gate transistor, see Section VI, a higher supply voltage may be used which will increase the output power.

IV. CIRCUIT DESIGN

Five different power amplifiers were designed and characterized: single transistor power amplifiers, cascode power amplifiers, both with 200 and 500 μm transistors, and a power amplifier with two 200-μm cascode power amplifiers, which were combined on-chip using Wilkinson combiners. Figure 3 gives an overview of the schematics.

All power amplifiers were single stage. Additional gain can be added by using one or several driver stages in front of the power amplifiers, but will not affect the maximum output power, which was of main interest in this study. Microstrip transmission lines were used as matching elements with the signal line in the top metal layer and ground plane in the bottom metal layer. Distributed components were chosen over lumped due to ease of modeling the transmission lines and lack of accurate inductance models in the design environment. The drawback of the distributed approach is a larger chip area, although the present designs could be shrunk considerably with more aggressive meandering. All transmission lines were designed to have a 50-Ω characteristic impedance, except for the shorted stubs to the drain, which were made 20 μm wide, corresponding to an impedance level of 27 Ω. The wider drain line helps to accommodate the large drain current, so that problems with electromigration and/or Joule heating are avoided. The lengths of the lines, and stubs were appropriately chosen for best performance in terms of matching, gain, and output power.

The power amplifiers were fabricated in a 130-nm RF CMOS process with four Cu layers, two thick top Al metal layers, and MIM capacitors. The designs were made using

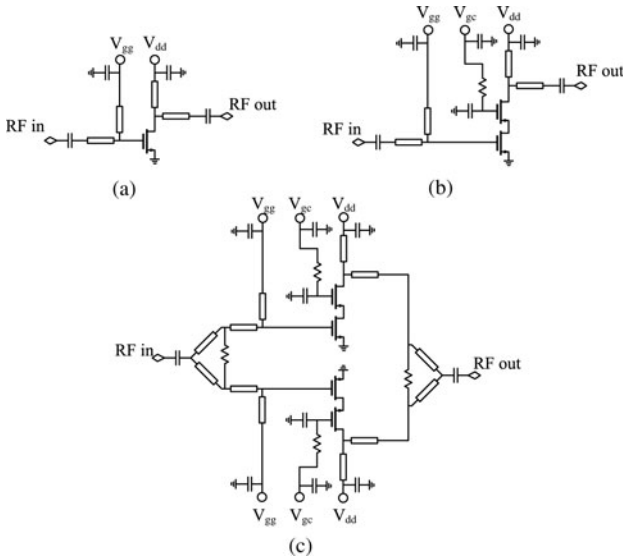

Fig. 3. Schematic of (a) the single transistor power amplifiers, (b) the cascode power amplifiers, and (c) two combined cascode power amplifiers.

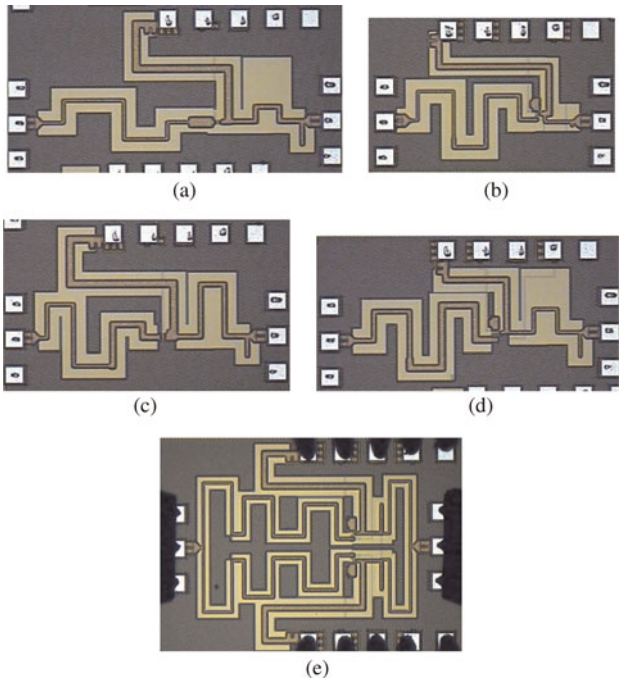

Fig. 4. Chip photo of the five different power amplifiers.

Agilent's ADS simulator and Cadence layout environment. Chip photos of the power amplifiers can be found in Fig. 4.

V. RESULTS

The power amplifiers were measured on wafer with 1.5-V drain bias for the single transistor power amplifiers and 3.0-V drain and cascode bias for the cascode power amplifiers. The gain versus output power at 20 GHz for all five power amplifiers are presented in Fig. 5.

A comparison with simulated and measured *S*-parameter data of the combined 200-μm cascode amplifiers shows good agreement, see Fig. 6, although a slight frequency shift toward lower frequencies is observed. The transducer gain and PAE of both the combined 200-μm cascode power amplifier and

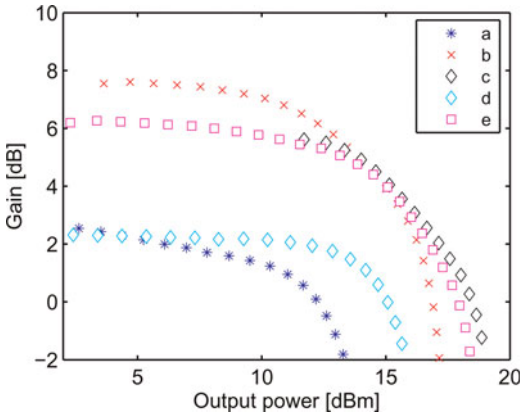

Fig. 5. Transducer gain versus output power for the single transistor 200-μm power amplifier (a), the 200-μm cascode power amplifier (b), the two combined 200-μm cascode power amplifiers (c), the single transistor 500-μm power amplifier (d), and the 500-μm cascode power amplifier (e). All at 20 GHz.

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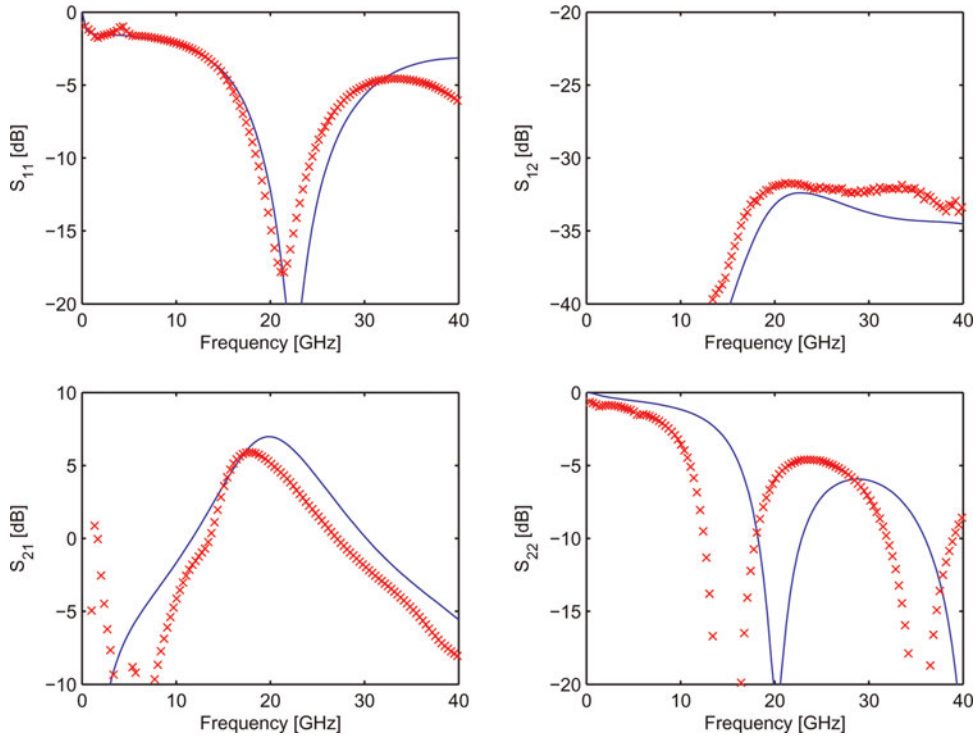

Fig. 6. Measured (crosses) and simulated (solid lines) *S*-parameters of the combined 200-μm cascode power amplifier.

the 200-μm cascode power amplifier show very good agreement between simulation and measurement, see Figs 7 and 8.

The agreement between both small and large signal simulations and measurements shows that the used models are valid both for the transistors and passive matching networks, including the Wilkinson combiner. Furthermore, in Fig. 8 the simulated transducer gain without the RF-extension of the transistor model is shown. As can be seen from the figure the simulation without the RF extensions overestimates the gain with almost 2 dB, corroborating the need of the RF extension for accurate simulations.

A summary of these and previously published power amplifiers is made in Table 2.

Even though a thick top metal layer is used for the transmission lines in the matching network, the *Q*-value is still quite limited due to a lossy dielectric, the SiO_2, and resistive losses in the metal. The partitioning of the losses between the input and output matching network as well as the power splitter/combiner were simulated and is presented in Table 3. The input and output matching networks contribute together with about 2 dB to the loss. The combiner adds another 1.1 dB in loss, but as the combination of two power amplifiers will add 3 dBm it is still beneficial to use a power combining scheme to increase the output power.

VI. DISCUSSION ON THE LIMITS FOR 20 GHZ POWER AMPLIFIERS

From the data in Table 2 it is seen that a cascode configuration is preferred, both from a gain and output power perspective. The output power is higher for the cascode power amplifiers as a higher supply voltage can be applied. This is possible

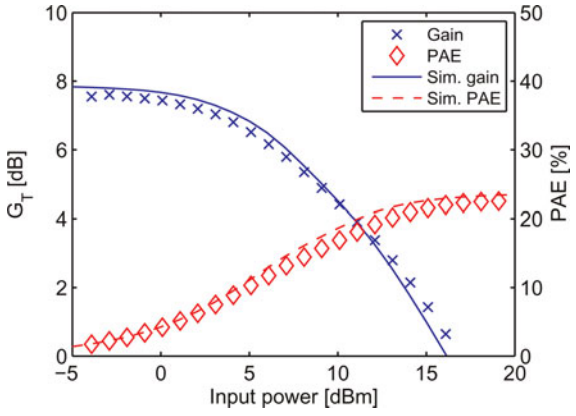

Fig. 7. Measured and simulated transducer gain and PAE of the 200-μm cascode power amplifier.

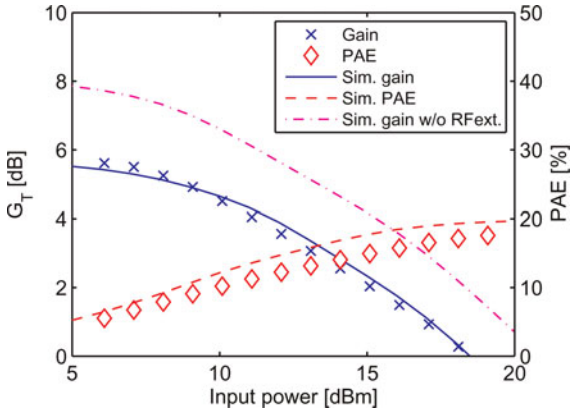

Fig. 8. Measured and simulated transducer gain and PAE of the combined 200-μm cascode power amplifier.

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Table 2. Summary of results and comparison of 10–40 GHz CMOS power amplifiers

Power amplifier	Frequency (GHz)	G_T/stage (dB)	P_{1dB} (dBm)	P_{sat} (dBm)	PAE (%)	V_{supply} (V)	Size (mm²)	Tech.	Stages
This work									
(a) Single 200 μm	20	2.8	7.8	12	36	1.5	0.91	130 nm	1
(b) Cascode 200 μm	20	7.5	11.6	16.9	22	3.0	0.7	130 nm	1 (cascode)
(c) Two cascode 200 μm comb.	20	5.6	14.6	18.3	17	3.0	1.13	130 nm	1 (cascode)
(d) Single 500 μm	20	2.5	13.6	15	22	1.5	0.72	130 nm	1
(e) Cascode 500 μm	20	6.2	13	18	16	3.0	0.72	130 nm	1 (cascode)
Previously published work									
[11]	17	7.3	15	17.1	15.6	1.5	0.9	130 nm	2 (balanced)
[12]	18	6.3	8	10.9	23.5	1.5	0.78	130 nm	4 (2 cascode)
[13]	24	3.5	11	14.5	6.5	2.8	1.3	180 nm	2 (cascade)
[14]	36–51	3.6	7.5	10.6	10	1.5	0.72	90 nm	4 (balanced)
[15]	24	9.4	13.3	19.1	15.6	3.6	0.325	180 nm	2 (cascode)

Table 3. Loss partitioning in the different power amplifiers.

Power amplifier	Losses of matching networks [dB]		
	Input*	Output*	Splitter†
Single 200 μm	1.06	1.05	–
Cascode 200 μm	1.14	0.64	–
Two cascade 200 μm comb.	1.07	1.42	1.1‡
Single 500 μm	1.0	1.23	–
Cascode 500 μm	1.07	1.44	–

*Including input or output MIM capacitors and bias network.
†Combiner at output is the same.
‡Only the loss, i.e. excluding the 3 dB due to the splitting.

since the drain–source voltage is partitioned between the input and the cascode transistor, as can be seen from Fig. 9, which shows the simulated drain–source voltage waveforms in the 500-μm power amplifier having a 3-V supply.

From Fig. 10(b) it can be seen that the peak voltages exceed the maximum permitted DC supply voltage of the technology, in this case 1.5 V. There are indications, e.g. [8, 9, 16], that the peak-to-peak can exceed the DC reliability limits; however, more research on the topic is necessary to fully understand these effects. From short-term measurements, i.e. up to 1 h, of the power amplifiers no degradation was seen for any of the presented power amplifiers, even when overdriven with a large input signal, up to 25 dBm during shorter intervals.

The effect on peak-to-peak voltage, gain, and output power versus supply voltage was also studied for the 500 μm cascode power amplifier, see Fig. 10(a). The output power drops slowly with decreased supply voltage to a level around 2 V then the roll off is more pronounced. The gain is, however, unaffected, as expected. The peak-to-peak values follow the output power with a faster roll off, versus lower supply voltage, for the drain–source voltage of the cascode transistor, see Fig. 10(b).

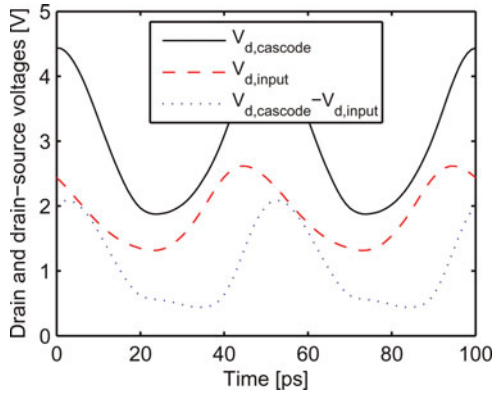

Fig. 9. Simulated drain and drain–source voltage waveforms for the 500-μm power amplifier with 3-V supply voltage, at 20 GHz.

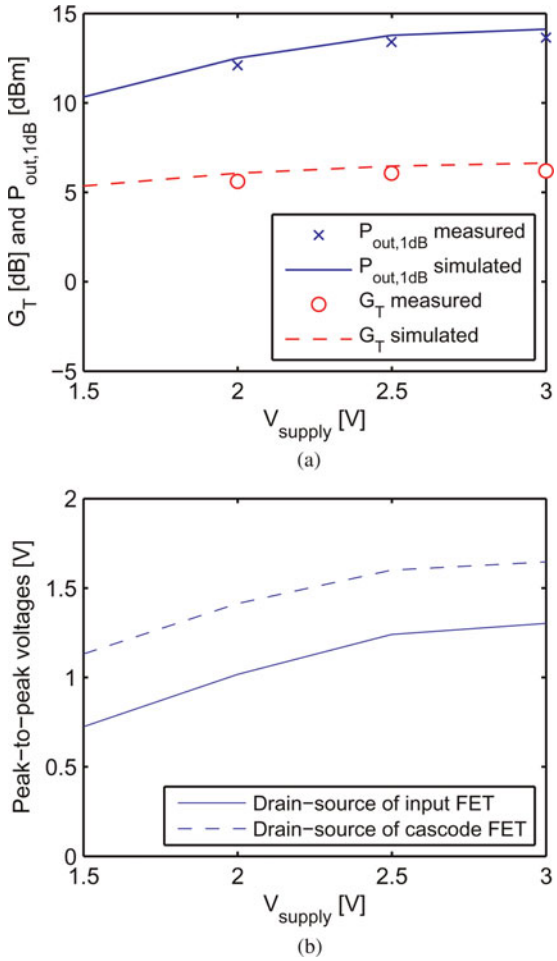

Fig. 10. (a) Simulated and measured gain and output power versus supply voltage of the 500-μm cascode power amplifier. (b) Simulated peak-to-peak voltage between source and drain for the common-source and common-gate transistor of the cascode cell. Both at 20 GHz.

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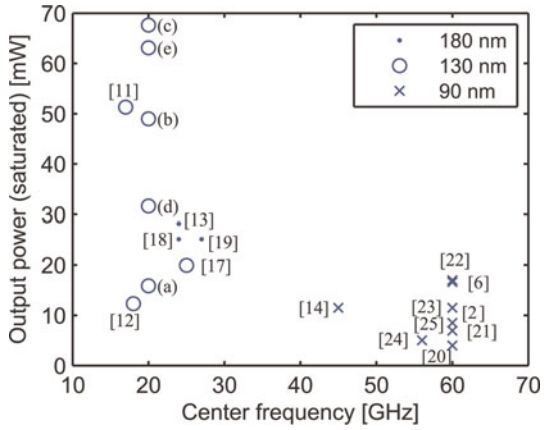

Fig. 11. Output power versus frequency for published power amplifiers in CMOS between 10 and 70 GHz. This paper: (a)–(e).

The output power of these and previously published power amplifiers [6, 11–13, 17–25] are marked versus frequency in Fig. 11. The saturated output power is presented but it is important to realize that the 1 dB compression point in some cases is significantly lower, some examples can be seen in Table 2.

VII. CONCLUSIONS

Using both device level measurements and a set of different designs, the limits and tradeoffs for power amplifier design in 130-nm CMOS at 20 GHz have been investigated.

Transistor size and configuration as well as the combining of two power amplifiers using Wilkinson splitter/combiners were studied. A maximum output power of 63 mW at 20 GHz for two on-wafer combined cascode power amplifiers and 148 mW/mm from load pull characterization of a single transistor were achieved. Both these values are, to the authors' knowledge, the highest reported above 10 GHz for CMOS. Furthermore, transistor modeling and the layout of transistors for power amplifiers were discussed.

From the results presented in this paper it is concluded that the maximum output power for 130 nm CMOS power amplifier at 20 GHz is between 100 and 200 mW, probably closer to 200 mW. If two of the 500 μm power amplifier presented in this paper were combined on-wafer it would be possible to achieve 100 mW in output power. Combining up to four amplifiers using five-port splitters/combiners is feasible and would result in an output power close to 200 mW.

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