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RESEARCH PAPER

Study on mechanisms of InGaP/GaAs HBT safe operating area using TCAD simulation

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The safe operating area (SOA) of InGaP/GaAs heterojunction bipolar transistors has been studied using two-dimensional Technology Computer-Aided Design (TCAD) tool. Comprehensive physical models, including hydrodynamic transport-based impact ionization and self-heating models were implemented. The simulations for two DC modes (constant I_b and V_b modes) captured all the SOA features observed in measurements and some failure mechanisms were revealed for the first time by TCAD simulations. The simulated results are also in agreement with analytical modeling. The simulation not only gives us insight to the detailed failure mechanisms, but also provides guidance for the design of devices with better ruggedness and improved SOA performances.

Keywords: Simulation, HBT, Safe operating area, TCAD

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I. INTRODUCTION

GaAs-based heterojunction bipolar transistors (HBTs) are widely used for power amplifiers in today's wireless communication systems. This technology offers high power density, high efficiency, and high linearity. But the increasing demand for high performance puts a stringent requirement for the device ruggedness [1–6]. A clear understanding of GaAs HBTs' safe operating areas (SOAs) and an accurate way to characterize them are extremely important.

Recently, the SOAs of industrially fabricated InGaP/GaAs HBTs have been intensively studied [4, 7]. A typically measured SOA boundary under DC operation for an intrinsic device (with no added ballasting resistors) is shown in Fig. 1, in which with stepping constant base voltage: V_b mode (a) or constant base current: I_b mode (b), and sweeping the collector voltage, the collector current density is monitored until the device fails as denoted with red dots. For V_b mode two distinct regions are clearly seen in the SOA boundary. One region is at high current and low voltage and the other one at low current and high voltage. The I–V characteristics before failures in these two regions are very different. At low voltage and high current, the current goes up quickly with V_{ce}, reaches a maximum, and then comes down before it fails. At low current and high voltage, however, the current usually bends up before it fails. The analytical modeling in [7] has successfully demonstrated the same phenomenon as observed experimentally. It shows that at low voltage and high current, the failure is controlled by the impact ionization because of the Kirk effect induced breakdown (KIB) (Kirk effect occurs when the mobile carrier density exceeds the space charge density in the collector causing the base push-out and electric field reversal [8]), and at low current and high voltage, the failure is governed by the self-heating effect. The physical picture of the device operation around SOA boundary, however, could not be clearly illustrated with the simplified analytical models. For I_b mode the phenomenon of current "hogging" in two-finger devices has been experimentally found [9], but to the authors' knowledge, it has never been numerically demonstrated with Technology Computer-Aided Design (TCAD). Most interestingly Fig. 1 shows that SOA boundaries for V_b and I_b modes are different, which also needs to be demonstrated with TCAD.

TCAD tool has been well recognized for revealing the operational mechanisms of the compound semiconductor devices [10, 11] owing to its fundamental physical models. In this work, we perform two-dimensional (2D) numerical simulations using TCAD tool, for the first time, to investigate the mechanisms of HBT's SOA formation, and theoretically demonstrate our experimental findings.

II. 2D SIMULATION SETUP

The TCAD tool Sentaurus is used for the simulation of a InGaP/GaAs HBT as shown in Fig. 2. The epi-layers are typical in the industry as described in [7]. The substrate thickness is 300 μm and lateral width on one side is 200 μm, which emulates the real device die under test.

Hydrodynamic model that accounts for the energy transport between the carriers and lattice is used [12], so that the device is heated up by the energy transferred from electrons

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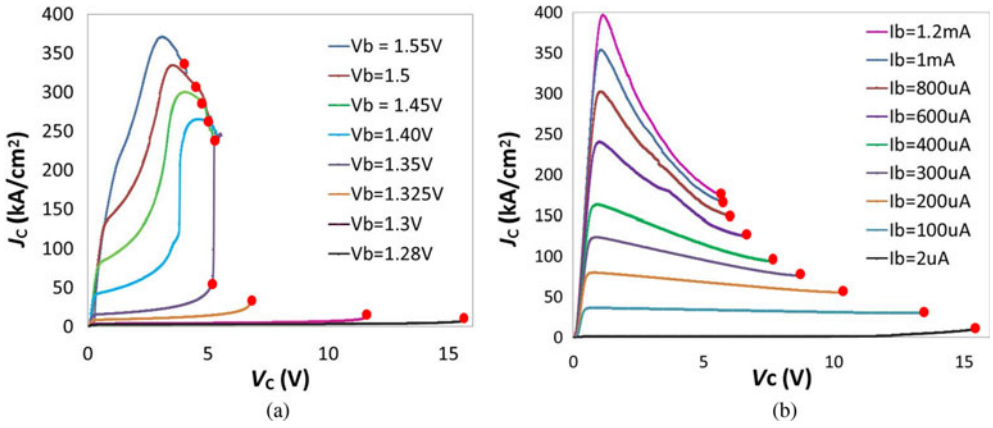

Fig. 1. SOA measurements at room temperature for devices of emitter area $2 \times 2 \times 6\ \mu m^2$ with constant V_b (a) and I_b (b) inputs. The red dots indicate the failure points the envelop of which defines the boundary of the SOA [7]. The current bent-over or snapback following each failure point is not shown here.

to the lattice. The carrier generation rate due to the impact ionization (*ii*) is expressed by

$$G_{ii} = \alpha_n \cdot n \cdot v_n + \alpha_p \cdot p \cdot v_p, \tag{1}$$

where n and p denote the electron and hole, respectively, α_n and α_p are the impact ionization coefficients, and v_n and v_p are the velocities. An empirical model is used for α_n and α_p:

$$\alpha_{n,p} = a_{n,p}F(1 + c_{n,p}\Delta T)\exp\left[-\left(\frac{b_{n,p}(1 + d_{n,p}\Delta T)}{F}\right)^{\delta_{n,p}}\right], \tag{2}$$

where $a_{n,p}$, $b_{n,p}$, $c_{n,p}$, $d_{n,p}$, and $\delta_{n,p}$ are coefficients, ΔT is the lattice temperature difference from 300 K, and F is the effective electric field that is dependent on the carrier temperature [12]. Generally the *ii* ratio for GaAs decreases with the temperature. The coefficient values are based on the reported data [13] but adjusted according to our breakdown measurement. To verify the aforementioned *ii* model we performed BV_{cbo} (emitter opened) simulation and the collector current exhibits very steep increase at collector voltage of ~24 V, which is aligned with our BV_{cbo} breakdown voltage (24 − 25 V) in manufacturing [7].

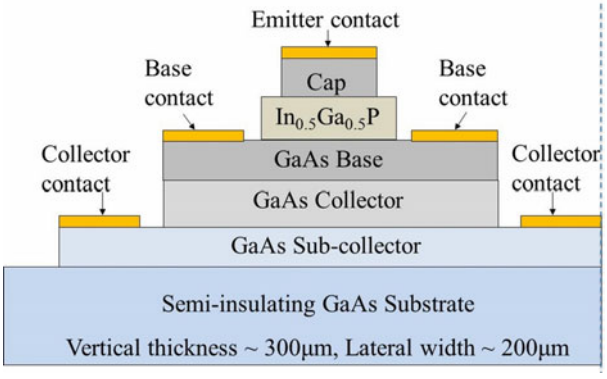

Fig. 2. Schematic InGaP/GaAs HBT layout of a single emitter finger for 2D simulations. Two-finger device is symmetrical with respect to the vertical dash line on the right side.

Energy band gap shrinks with increasing temperature and is calculated using

$$E_g = E_{g0} - \alpha \cdot T^2/(\beta + T), \tag{3}$$

where E_{g0} is the band gap at temperature of zero, and α, β are coefficients. The band gap of ternary materials such as $In_xGa_{1-x}P$ is calculated by

$$E_{g(InGaP)} = xE_{g(InP)} + (1 - x)E_{g(GaP)} + C_g \cdot x(1 - x), \tag{4}$$

where $E_{g(InP)}$ and $E_{g(GaP)}$ are the band gaps of InP and GaP, respectively, and C_g is the bowing parameter [14]. The low-field mobility is doping concentration (N) and temperature (T) dependent and expressed as [15]

$$\mu = \mu_{min} + \frac{\mu_{max}(T/300k)^{\alpha} - \mu_{min}}{1 + ((N/N_0)(300k/T)^{\beta})^{\lambda}}, \tag{5}$$

where μ_{min}, μ_{max}, α, β, and λ are the coefficients. The lattice thermal conductivity is expressed by

$$k_L = k_{300} \cdot \left(\frac{T_L}{300k}\right)^{\alpha}, \tag{6}$$

where k_{300} is the thermal conductivity at 300 K and α is a coefficient. k_L for ternary materials is calculated by the interpolation of the two basic materials in the same fashion as abovementioned energy band gap. The lattice-specific heat is assumed to be constant since the data show that it has no significant variation above 300 K [14]. All the parameters and coefficients are defined based on either publicized data or our own measurements.

For the thermal boundary conditions, we define a constant temperature of 300 K on the backside of the substrate, and a thermal dissipation surface simply on top of the emitter metal due to the thick metal stack right on top of the emitter in real devices.

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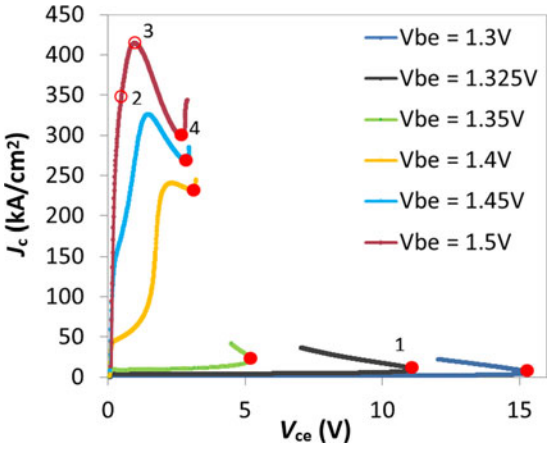

Fig. 3. Simulated collector current density versus collector voltage for a 24 μm² emitter area device with constant V_b inputs. The red solid dots indicate the failure points that define the SOA boundary.

III. RESULTS AND DISCUSSION

A) Constant V_b mode

The simulated collector current density (J_c) as a function of collector voltage (V_{ce}) with stepping constant V_{be} from 1.3 to 1.5 V is shown in Fig. 3. The solid red dots are the failure points where the J_c exhibits bent-over or snapback which is identical to the measurement [4, 7]. The boundary of SOA that is formed with these failure points demonstrates two distinct regions as experimentally shown in Fig. 1: one is of low currents and high voltages, and the other is of high currents and low voltages.

Let us first look at the device operations around failure points 1 and 4, which represent two different SOA regions. Figure 4 shows the calculated effective electric field in the collector along the center line of the device (see Fig. 2) at failure points 1 and 4. The normalized distance of zero and one indicate the base/collector and collector/sub-collector junctions, respectively. For comparison, the simulated field at the condition of BV_{cbo} as described previously is also displayed It should be noted that the field we are referring is so called "effective electric field" associated with electron's temperature or energy, which is different from the conventional electric field, because hydrodynamic transport model is used in the tool [12]. Therefore the peak field (~3.3E5 V/cm) can be approximately considered as an avalanche threshold in our device. It is obvious that impact ionization is not responsible for the failure at point 1, since the effective field (<1.5E5 V/cm) is way below the aforementioned avalanche threshold. At point 4, however, the peak field is located at collector/sub-collector junction due to Kirk effect (to be discussed next) and the field strength is almost the same as the avalanche threshold. This shows that the impact ionization is responsible for the failure at point 4.

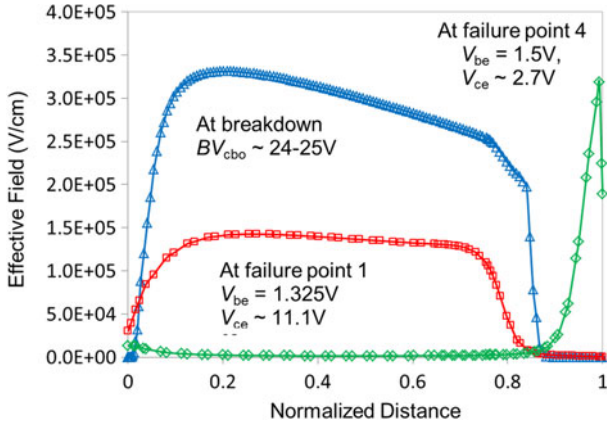

Fig. 4. Simulated effective electric field from base/collector junction to collector/sub-collector junction at three bias conditions: (1) (blue triangles) BV_{cbo} of around 24 V, (2) (red squares) the failure point of V_{be} = 1.325 and V_{ce} = 11.1 denoted as "1" in Fig. 3, and (3) (green diamond) the failure point of V_{be} = 1.5 V and V_{ce} = 2.7 V denoted as "4" in Fig. 3.

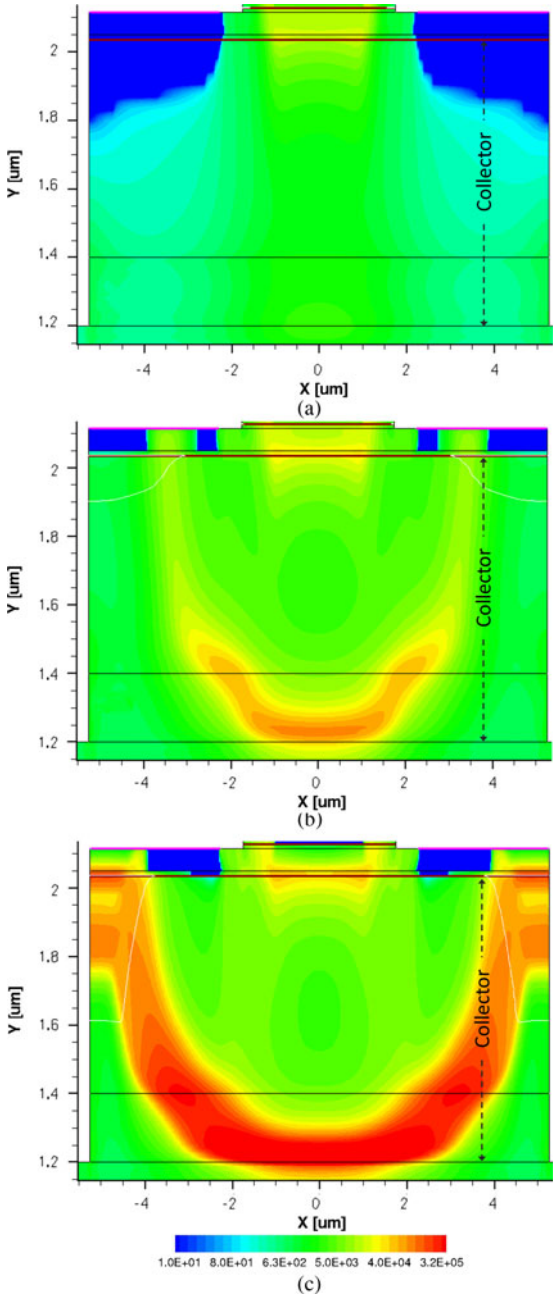

Fig. 5. Simulated effective field (V/cm) distributions for the point 2 (a), point 3 (b), and point 4 that is also failure point (c) in Fig. 3. The upper and lower boundaries of the collector are base/collector and collector/sub-collector junctions, respectively.

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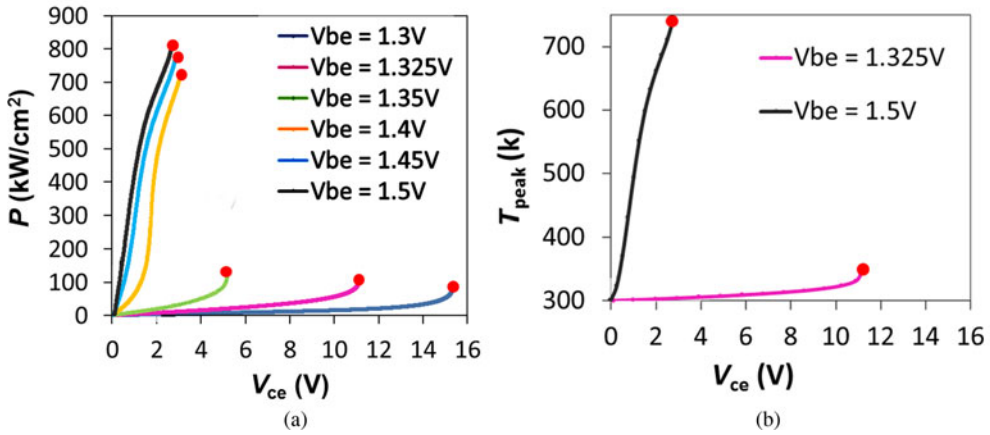

Fig. 6. Simulated power density (a) and peak temperature in the device for two V_{be} conditions representing two distinct regions (b).

To further reveal the physical mechanism for the high-current and low-voltage region which seems to be very unique, we study two more bias conditions indicated by points 2 and 3 in Fig. 3. The simulated 2D profiles of effective electric field for the points 2, 3, and 4 are shown in Fig. 5. With increasing collector current from points 2 to 3, the Kirk effect occurs and the peak field moves from the base/collector junction toward sub-collector at point 3. Then the collector current drops due to severe base push-out and at point 4, the field becomes so high at collector/sub-collector that avalanche breakdown occurs.

Here we need to answer an intuitive question. Is the failure because the temperature is so high that the device is burned? Figure 6 shows the output power density (a) and maximum temperature inside device (b) at V_b mode. Obviously, devices do fail when the output power or the device temperature is high, e.g., when $V_{be} = 1.5$ V, but devices also fail when the output power or the device temperature is low, e.g., when $V_{be} = 1.325$ V. The temperature variation at failure points is up to 400 K. Therefore, device temperature is not the root cause for the failure. It should be noted that the way we define the thermal boundaries is simplified compared with the real devices that are three dimensional and have thermal dissipation paths everywhere. The 3D thermal simulations with a different tool [4] showed that the peak temperature is lower by around 15%. Nevertheless, the results from our TCAD tool have no impact on the mechanism studies.

We have seen previously that at point 1 in Fig. 3 no avalanche occurs, but why the device still fails? Figure 7 shows the self-heating effect at low current range ($V_{be} = 1.325$ V). The snapback point (as denoted II) of the simulated curve without self-heating model is greater than the one (as denoted I) with self-heating model implemented by more than 6 V. In other words, the SOA boundary at low current is dominated by the self-heating mechanism. We can also see that the snapback behavior with self-heating effect is much sharper and more abrupt than that without self-heating. So the failure in this region is primarily due to the thermal effect that drives the device into an instable condition [7]. This is in agreement with our experimental observation.

B) Constant I_b mode

Figure 8 shows the simulated IV curves at constant I_b mode for a $2 \times 2 \times 6\ \mu m^2$ device. Similar to the V_b mode, the current snapback can be seen and those failure points denoted as red dots form the SOA boundary. It is noted that for some curves, e.g., $I_b = 3E{-}5A$, the current exhibits a very short dip following the snapback. This is probably caused by the instability around the failure point which is also numerically instable.

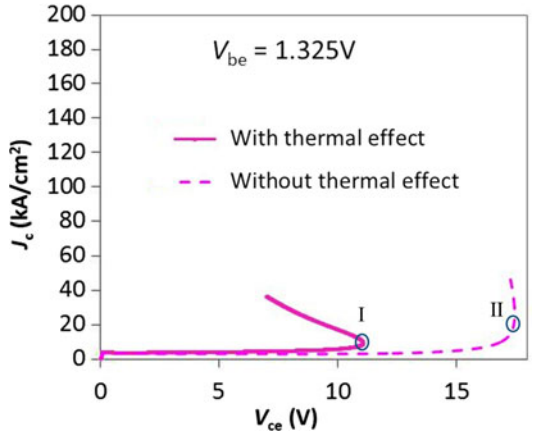

Fig. 7. Simulated collector current density versus collector voltage at V_{be} of 1.325 V with (solid line) and without (dash line) self-heating model. Impact ionization model is used for both cases.

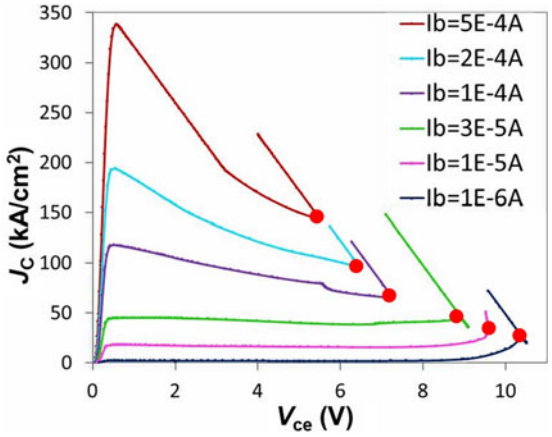

Fig. 8. Simulated collector current density versus collector voltage at I_b mode. Red dots indicate the failure points that form the SOA boundary.

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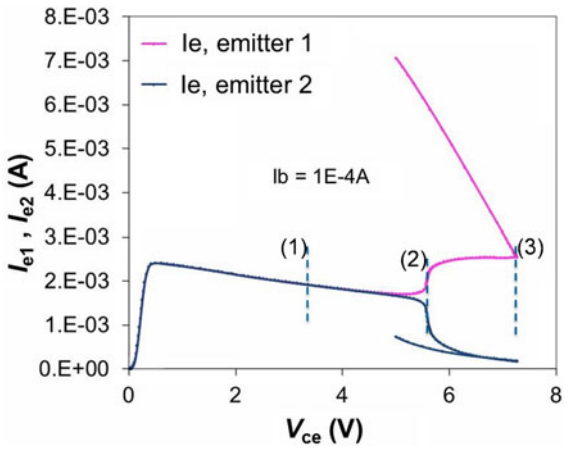

Fig. 9. Simulated emitter current for each of two emitter fingers at $I_b =$ 0.1 mA. The current split occurs at point 2 and the device fail at point 3.

It has been experimentally found [9] that for I_b mode one of the two emitter fingers eventually draws most of the device current before failure, and analytical modeling [16] shows that such a current "hogging" occurs when the device enters into an instable status in the real world due to the fact that two emitter fingers are not perfectly symmetrical. Now this phenomenon has been demonstrated with TCAD simulation. Figure 9 displays the current split between two fingers after certain V_{ce}. To better understand the device operations, let us look at the 2D impact ionization and temperature before the current split (1), at the current split (2), and at the failure point (3). Figures 10 and 11 show the 2D impact ionization ratio and lattice temperature respectively at above-mentioned three conditions in Fig. 9. We can see that at point (1) both impact ionization and temperature under two fingers are quite equal, but at point (2) where the current split occurs, the physical pictures of two fingers become noticeably different. At point (3) the impact ionization under one finger is so strong that avalanche occurs, in the meantime the lattice temperature under one finger gets much hotter but the other one gets much colder. It is interestingly noted that the simulated two-emitter structure is not intentionally built to be asymmetric (see Fig. 2) in terms of physical properties and geometries, but we think there is still subtle discrepancy of the automatically generated mesh nodes between two emitters, which causes the two emitter fingers numerically asymmetric. This simulation has further demonstrated that current "hogging" effect universally exists in real multi-finger HBTs.

Most importantly we can observe that for I_b mode, both peak impact ionization and field (not shown here) under one finger are at collector/sub-collector junction around the failure point. This demonstrates that the KIB is primarily responsible for the failure.

C) Comparison of SOA boundaries in V_b and I_b modes

Figure 12 plots all simulated (a) and measured (b) SOAs for I_b and V_b modes, respectively. The general behaviors of both simulated and measured boundaries are in good agreement. Both simulation and measurement show the boundary difference between two DC modes. This difference has been interpreted in [7] in which the SOA boundary of I_b mode is called the secondary boundary associated with the transition region

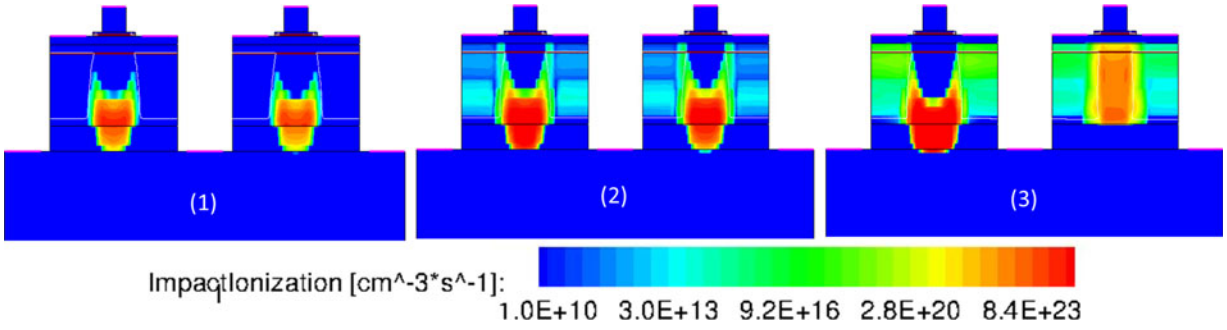

Fig. 10. Simulated impact ionization ratio for two-emitter device at bias condition (1), (2), and (3) as shown in Fig. 9.

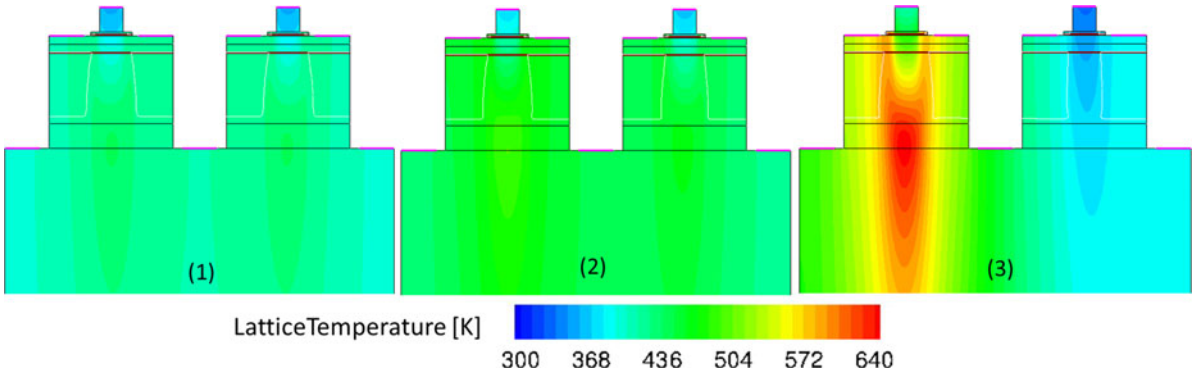

Fig. 11. Simulated lattice temperature for two-emitter device at bias condition (1), (2), and (3) as shown in Fig. 9.

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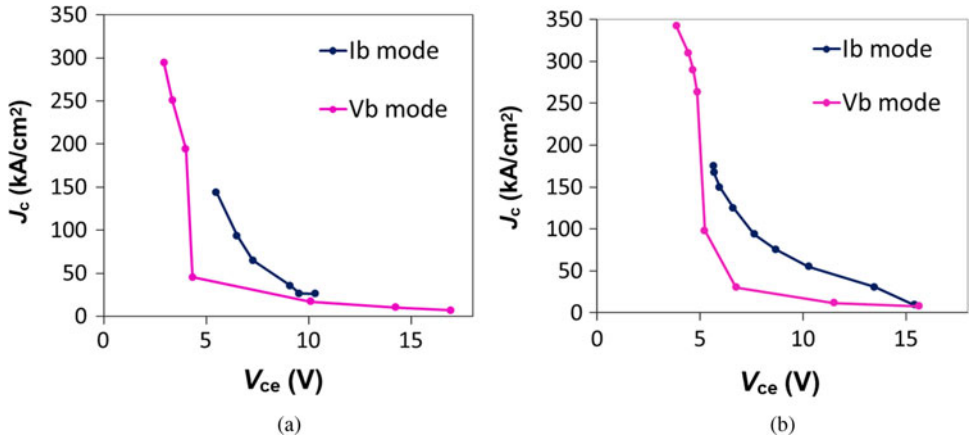

Fig. 12. Simulated (a) and measured (b) SOA boundaries for a 2 × 2 × 6 μm² device in both I_b and V_b modes.

between the high-current region and low-current region of the V_b mode SOA boundary. Both our measurement and simulation show that the aforementioned transition region in V_b mode is actually a gap without any failure points. This gap however can be broken in for I_b mode. The detailed discussion can be found in [7].

IV. CONCLUSION

We performed 2D TCAD simulations to study the SOA mechanisms for InGaP/GaAs HBTs. Comprehensive physical models including hydrodynamic transport, impact ionization, and self-heating were implemented. Simulated SOA boundaries for constant V_b and I_b modes were qualitatively in good agreement with measurements. Failure mechanisms in different SOA regions for V_b and I_b modes were revealed, which also verified the analytical modeling results. This study also showed that KIB plays an important role in the failure of GaAs HBTs, which is a distinguished feature compared with Si bipolar devices. This work demonstrates that the 2D simulation by TCAD is useful not only in predicting the I–V characteristics of a device, but also in understanding why and how a device fails. It can certainly aid us in designing HBTs with better ruggedness and larger SOAs in the future.

REFERENCES

[1] Wang, N.L. et al.: 28 V high-linearity and rugged InGaP/GaAs power HBT, in 2006 IEEE MTT-S Int. Microwave Symp. Digest, San Francisco, CA, USA, June 2006, 881–884.

[2] Tsai, S.-H.; Chiou, R.-B.; Chou, T.-Y.; Lin, C.-K.; Williams, D.: An ultra-high ruggedness performance of InGaP/GaAs HBT for Multi-Mode/Multi-Band power amplifier application, in 2012 CS MANTECH, Boston, MA, USA, April 2012, 145–149.

[3] Cismaru, C.; Banbrook, H.; Zampardi, P.J.: High volume test methodology for HBT device ruggedness characterization, in 2010 CS MANTECH, Portland, OR, USA, May 2010, 65–68.

[4] Tao, N.G.M.; Lee, C.-P.; Denis, A.S.; Henderson, T.: InGaP/GaAs HBT safe operating area and thermal size effect, in 2013 CS MANTECH, New Orleans, LA, USA, May 2013, 219–222.

[5] Jin, R.; Chen, C.; Halder, S.; Curtice, W.R.; Hwang, J.C.M.: Safe operating area of GaAs HBTs based on sub-nanosecond pulse characteristics. IEEE Trans. Microw. Theory Tech., **58** (2010), 3996–4003.

[6] Lee, C.-P.; Chau, F.H.F.; Ma, W.; Wang, N.L.: The safe operating area of GaAs-based heterojunction bipolar transistors. IEEE Trans. Electron Devices, **53** (2006), 2681–2688.

[7] Lee, C.-P.; Tao, N.G.M.; Lin, B.J.F.: Studies of safe operating area of InGaP/GaAs heterojunction bipolar transistors. IEEE Trans. Electron Devices, **61** (2014), 943–949.

[8] Kirk, C.T. Jr.: A theory of transistor cutoff frequency (fT) falloff at high current densities. Institute of Radio Engineers Transactions on Electron Devices, vol. ED-9, 1962, p. 164.

[9] Liu, W.: Handbook of III-V Heterojunction Bipolar Transistors, John Wiley & Sons, Inc., New York, 1998.

[10] Palankovski, V.; Wagner, S.; Selberherr, S.: Numerical analysis of compound semiconductor RF devices, in 2003 GaAs IC Symp. 25th Annual Technical Digest, San Diego, CA, USA, 2003, 107.

[11] Tao, N.G.; Bolognesi, C.R.: Kirk effect mechanism in type-II InP/GaAsSb double heterojunction bipolar transistors. J. Appl. Phys., **102** (2007), 064511.

[12] Synopsys, Sentaurus Device User Guide, 2013, http://www.synopsys.com/tools/tcad/Pages/default.aspx

[13] Ghin, R.; David, J.P.R.; Hopkinson, M.; Pate, M.A.; Rees, G.J.; Robson, P.N.: Impact ionization coefficients in GaInP p-i-n diodes. Appl. Phys. Lett., **70** (1997), 3567.

[14] Palankovski, V.; Quay, R.: Analysis and Simulation of Heterostructure Devices, Springer-Verlag/Wien, New York, 2004.

[15] Sotoodeh, M.; Khalid, A.H.; Rezazadeh, A.A.: Empirical low-field mobility model for III-V compounds applicable in device simulation codes. J. Appl. Phys., **87** (2000), 2890.

[16] Lu, K.; Snowden, C.M.: Analysis of thermal instability in multi-finger power AlGaAs/GaAs HBT's. IEEE Trans. Electron Dev., **43** (1996), 1799–1805.

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