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RESEARCH PAPER

A K-band delay line based on parasitic reduced artificial left-handed transmission line

HYUN-SEUNG LEE, EUN-GYU LEE AND CHOUL-YOUNG KIM

A K-band microstrip delay line based on parasitic reduced left-handed transmission line (LHTL) with interdigital capacitors and shunt inductors is demonstrated with the aid of printed circuit board technology. The proposed delay line has ground slots under the interdigital capacitors to reduce the parasitic capacitance. The time delay of the proposed LHTLs is approximately 2.6 times larger than that of the conventional LHTLs. The input return loss of the proposed LHTL at 24 GHz is −16.9 dB and less than −10 dB from 20.5 to 26.1 GHz.

Keywords: Delay line, Left-handed transmission line (LHTL)

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I. INTRODUCTION

Microwave delay lines are very important components in many applications, including radar and phased-array systems [1]. There are many types of delay lines. Examples include optical delay lines, magnetostatic wave delay lines, surface acoustic wave delay lines, high-temperature superconducting delay lines, and transmission line delay lines [2–5]. Delay lines based on a transmission line are typified by their low loss properties and their wide band characteristics; they are also suitable for microwave integrated circuits and monolithic microwave integrated circuits, though they require a larger area compared to other delay lines. A compact delay line can be formulated using an LHTL structure in a microwave integrated circuit and a monolithic microwave integrated circuit [6, 7], as in LHTLs, the phase constant β can be much larger than that in RHTLs [8]. Delay lines based on microstrip LHTLs have been implemented with planar transmission lines periodically loaded with interdigital capacitances and short-stub inductances at 1.5 and 9.5 GHz, respectively [8, 9].

In this paper, a microstrip delay line based on an LHTL with ground slots is proposed. A printed circuit board technology is used to demonstrate a K-band delay line based on an artificial LHTL. The time delay of the proposed three-unit LHTLs with ground slots is approximately 2.6 times larger at 24 GHz compared to three-unit conventional LHTLs without ground slots. The input return loss of the proposed LHTL at 24 GHz is −16.9 dB. Additionally, the input return loss of the proposed LHTL is less than −10 dB from 20.5 to 26.1 GHz. These findings were possible because the parasitic capacitance of an interdigit capacitor is reduced with ground slots.

Department of Electronics Engineering, Chungnam National University, Daejeon, Republic of Korea. Phone: + 82-42-821-5663
Corresponding author:
Choul-Young Kim
Email: cykim@cnu.ac.kr

II. DESIGN

A conventional LHTL based on an artificial transmission line with interdigital capacitors and shunt inductors is shown in Fig. 1 [8]. A LHTL can be realized artificially in the form of a lumped-element ladder network. In this model, there is no series parasitic inductance because the parasitic inductance is small enough. There is a parasitic capacitance present in the interdigital capacitor.

The propagation factor with the parasitic capacitance β_p is given by

$$\beta_P = -\frac{\sqrt{1-\omega^2 L' C_g}}{\omega\sqrt{L'C'}} = -\frac{1}{\omega\sqrt{L_p C'}} = \beta\cdot\sqrt{\xi}. \quad (1)$$

Here, ω denotes the angular frequency, L' is the unit length inductance, C' is the unit length capacitance, and C_g is the parasitic capacitance per unit length:

$$L_P = \frac{L'}{\xi}. \quad (2)$$

$$\xi = 1-\omega^2 L' C_g. \quad (3)$$

The characteristic impedance with the parasitic capacitance, Z_{o_P}, is given by

$$Z_{o\_P} = \sqrt{\frac{L'}{C'}\cdot\frac{1}{1-\omega^2 L' C_g}} = \sqrt{\frac{L_P}{C'}} = Z_o\cdot\frac{1}{\sqrt{\xi}}. \quad (4)$$

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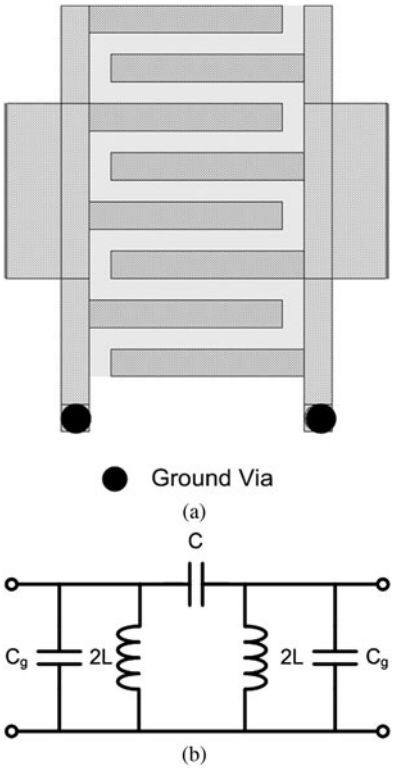

Fig. 1. (a) The figure and (b) the equivalent circuit model of a conventional unit delay line based on an artificial LHTL.

The time delay with the parasitic capacitance, t_{d_P} is given by

$$t_{d\_P} = \frac{1}{\omega^2 \sqrt{L_p C'}} = t_d \cdot \sqrt{\xi}. \quad (5)$$

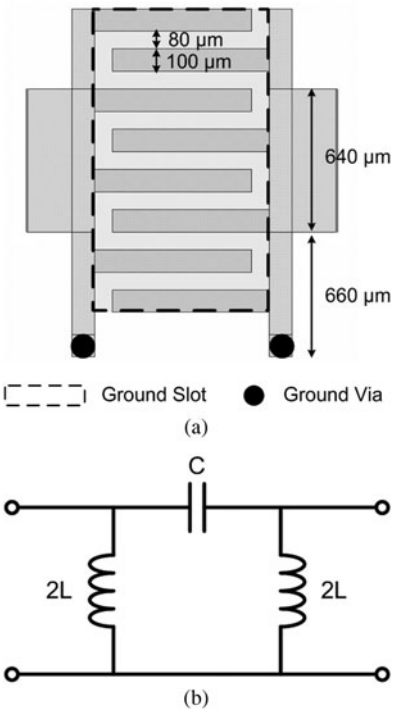

Fig. 2. (a) The figure and (b) the equivalent circuit model of the proposed delay line based on parasitic reduced artificial LHTL.

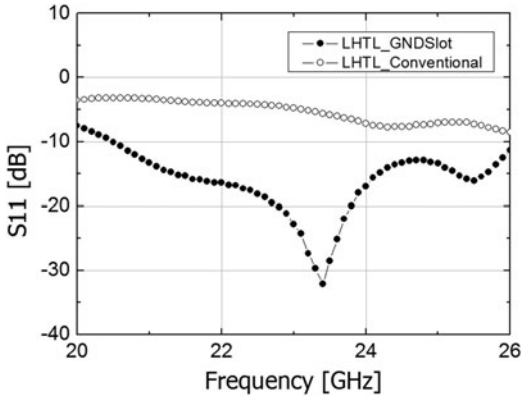

Fig. 3. Measured return losses of the three-unit LHTL with and without a ground slot.

The operating frequency is limited by the parasitic capacitance, as follows:

$$\frac{1}{2\sqrt{L'C'}} \leq \omega \leq \frac{1}{2\sqrt{L'C_g}}. \quad (6)$$

The effects of the parasitic capacitance known through equations (1)–(5) show an increasing impedance mismatch and a reduced the time delay in the range of equation (6).

The proposed LHTL with a ground slot that reduces the parasitic capacitance is shown along with the equivalent circuit model in Fig. 2. The parasitic C_g can be reduced by removing the ground metal under the interdigital capacitor. Capacitances and inductances are determined to have a 50 Ω port impedance and a small dispersion at a center frequency of 24 GHz. The test structures consist of the three-unit LHTL delay lines and 50 Ω lines that connect the connectors at each side. The test structures are designed on an RO3003 PCB, which has a dielectric constant of 3 and a thickness of 10 mil.

III. MEASUREMENT RESULTS

Conventional LHTL delay lines and the proposed delay lines with ground slots were measured with a short-open-load-through calibration up to the connectors to measure the S parameter. An Agilent 8510C vector network analyzer was used.

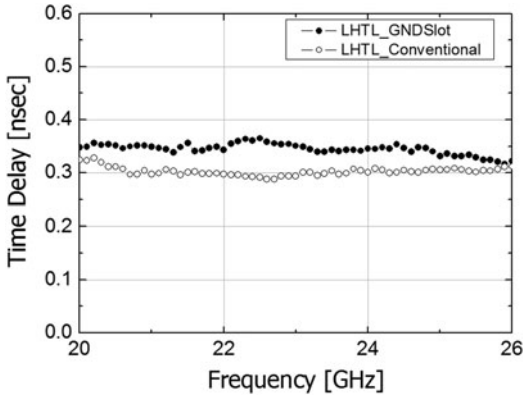

Fig. 4. Measured time delay of the test patterns of the proposed three-unit LHTL and that of a conventional LHTL.

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The input return loss of proposed LHTL is shown in Fig. 3. The input return loss of the parasitic reduced LHTL is less than −10 dB from 20.5 to 26.1 GHz. The measured time delays of conventional LHTL and the proposed structures are shown in Fig. 4. The 50 Ω line which has same length of 50 Ω line for connecting to the connectors in each side is also fabricated and measured. The time delay of proposed LHTLs with ground slots is approximately 78 psec at 24 GHz. The time delay of the proposed parasitic reduced LHTL is higher by approximately 45 psec at 24 GHz compared to a conventional LHTL. These results are also in accordance with equation (5).

IV. CONCLUSION

A K-band delay line based on parasitic reduced artificial transmission line is proposed. The proposed delay line shows superior performance compared to a conventional structure, as demonstrated through its time delay, due to the low parasitic capacitance effects.

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Hyun-Seung Lee received the B.S. and M.S. degree in electrical engineering from Wonkwang University, Iksan, Korea, in 2001. He is currently working toward the Ph.D. degree in electrical engineering at Chungnam National University. His research interests are RF filters and RF systems.

Eun-Gyu Lee received the B.S. degree in electronics engineering from Chungnam National University (CNU), Daejeon, Korea, in 2004 and M.S. degree in electrical engineering from Pohang University of Science and Technology (Postech), Pohang, Korea, in 2006. She is working on her Ph.D. degree in electronics engineering in CNU. Her research interests include mm-wave integrated circuits and systems for laser radar applications.

Choul-Young Kim received the B.S. degree in electrical engineering from Chungnam National University (CNU), Daejeon, Korea, in 2002 and M.S. and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2004 and 2008, respectively. From March 2009 to February 2011, he was a Postdoctoral Research Fellow at the department of electrical and computer engineering at the University of California, San Diego (UCSD). He is assistant professor of electronics engineering at Chungnam National University, Daejeon, Korea. His research interests include mm-wave integrated circuits and systems for short range radar and phased-array antenna applications.

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