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Theory and experimental validation of a Class E PA above theoretical maximum frequency

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This paper reports an investigation and a proposed solution to design Class E power amplifiers above the theoretical maximum frequency allowed by the adopted active device. Starting from the traditional time domain analysis, a numerical algorithm has been developed and presented in order to extend Class E feasibility through the optimization of the output voltage waveform. A hybrid Class E amplifier in laterally diffused metal oxide semiconductor (LDMOS) technology has been designed and measured. The final amplifier shows an output power of more than 10 W with an associated efficiency of 49% (power added efficiency (PAE) = 45%) over a 100-MHz bandwidth around 2.14 GHz.

Keywords: Class E, Power amplifier, High efficiency, High frequency, LDMOS

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I. INTRODUCTION

In modern communication systems highly efficient transmitters are desirable for simplifying heat sinking, reducing dc power consumption and cost, and increasing reliability, with regard to both base station and handset applications. On the other hand, the major contribution in overall efficiency is related to the final stage of the transmitter, that is the power amplification stage, and several efforts have been made during the last years to design highly efficient power amplifiers (PAs).

In this context, switched mode PAs are good candidates for high-efficiency operation. In particular, the adoption of Class E strategy, firstly proposed by Sokal and Sokal in the 1970s [1], has been receiving a large amount of interest from radio frequency (RF) PA designers, thanks to its simplified design formulas and its high performances in terms of output power and efficiency.

In a Class E PA, the switching behavior of the active device and the absence of power delivered at harmonics of the fundamental frequency allow one to minimize DC power consumption and achieve an ideal unitary efficiency.

These conditions are obtained by the proper design of the output matching network, whose component's values are determined in closed-form expressions and satisfy the operating conditions stated by Sokal and Sokal [1].

To date, many papers have already demonstrated the possibility of integrating the Class E PA either in wireless systems such as global system for mobile communications/general packet radio service (GSM/GPRS), universal mobile telecommunications system (UMTS), and wireless local area network (WLAN) terminals [2] or in PA architectures such as envelope elimination and restoration [3].

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However, the nonideal switching operation of the active device is still a critical issue, in particular when the operating frequency increases. In fact, a maximum operating frequency (f_{Max}), derivable from a simplified analysis, exists even for an ideal Class E PA and is directly dependent on the device physical limits (I_{Max} and breakdown voltage) and inversely dependent on bias point (V_{DC}) and device output capacitance (C_{ds}). Even if some solutions could be adopted by changing the value of V_{DC}, Class E maximum operating frequency is mainly determined by the value of C_{ds}, andis usually limited to a few gigahertz [4].

Nonetheless, Class E PA development recently registered an improvement related to the proliferation of emerging technologies such as SiGe–HBT and Si–LDMOS devices [5]. The former, thanks to high cut-off frequencies, represents a useful solution to minimize problems related to f_{Max} [6]. Anyway, for base station applications a high output power level is required, thus making LDMOS devices preferable when compared to SiGe–HBT [7], thanks to their higher breakdown voltage and maximum allowable current. However, LDMOS maximum frequency in Class E operation is limited to hundreds of megahertz.

The aim of this contribution is to determine how it is possible to extend the Class E operating mode above the stated maximum frequency, through the optimization of the voltage waveform and the proper choice of fundamental load impedance. The approach described herein is based on a numerical optimization of load impedance. In order to validate the proposed methodology, a 2.14-GHz Class E PA in LDMOS technology has been designed and characterized and its performances are discussed in this paper.

II. FREQUENCY DOMAIN ANALYSIS

A) Low frequency-domain analysis

The basic topology of the single-ended Class E PA is depicted in Fig. 1. The power dissipated in the active device is

minimized through a switching mode operation, while the output network is designed to ideally filter out the power delivered at harmonic frequencies of the fundamental one. As a result, a theoretical maximum efficiency of 100% is achieved. In order to carry out a simplified closed-form analysis of a Class E amplifier, referring to Fig. 1, it is convenient to assume the active device as a perfect switch, its output capacitance C_{ds} included in the capacitance C_1, and the series C_o–L_o acting as an ideal filter at operating frequency. Under these assumptions, the values of R_L, ΔL, and C_1 can be dimensioned to satisfy the Class E operating conditions formulated by Sokal and Sokal in [1], i.e.

1) a purely sinusoidal current across the load R_L;
2) zero voltage switching condition (ZVS), which implies nonsimultaneous nonzero voltage and current across the switch;
3) zero voltage derivative switching condition (ZVDS), which implies that the current starts to increase from zero after the switch is turned on.

Time domain expressions derived in [4] are herein reported for convenience, considering the most common case of a 50% duty cycle. The total current is written as the sum of a DC component that is the bias current I_{DC}, and a sinusoidal component, having its own amplitude a and its phase ϕ, which are determined applying ZVS and ZVDS conditions [4]:

$$i_{SW}(\vartheta) = \begin{cases} 0, & 0 < \vartheta < \pi, \\ i_{DS}(\vartheta) = I_{DC} & \\ \quad (1 - a\sin(\vartheta + \phi)), & \pi < \vartheta < 2\pi. \end{cases} \tag{1}$$

The voltage across the switch is obtained by integration of the current during the OFF period and is given by

$$\begin{aligned} v_{DS}(\vartheta) &= \frac{1}{\omega C_1}\int_0^{\pi} I_{DC}(1 - a\sin(\vartheta + \phi))d\vartheta \\ &= \frac{I_{DC}}{\omega C_1}(\vartheta + a(\cos(\vartheta + \phi)) - a\cos\phi). \end{aligned} \tag{2}$$

Class E ideal voltage and current waveforms are shown in Fig. 2. Although Class E PA time domain analysis is a relatively simple and straightforward process, a frequency domain approach is useful to better describe the harmonic content of switch voltage and current and to easily determine the load impedances Z_n at fundamental frequency and at its harmonics.

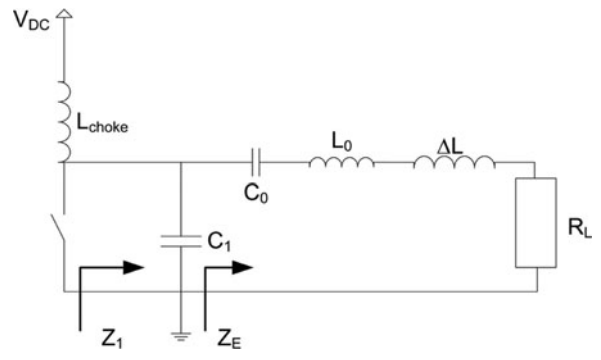

Fig. 1. Classical Class E topology.

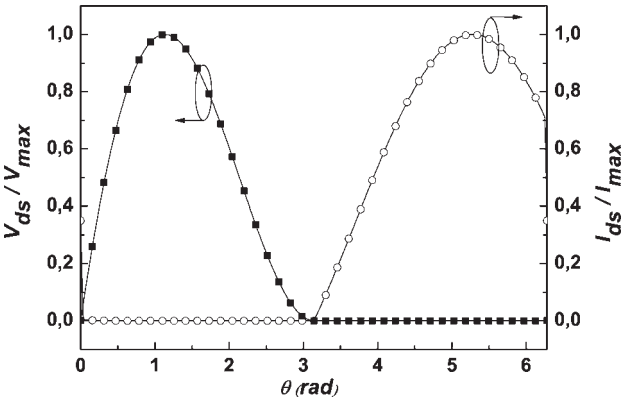

Fig. 2. Ideal Class E waveforms.

Applying a Fourier analysis on the current and voltage waveforms, their harmonic coefficients are expressed by [4]

$$I_n = \begin{cases} I_{DC}, & n = 0, \\ \dfrac{I_{DC}}{8\pi}(2\pi + 8i + i\pi^2), & n = 1, \\ \dfrac{I_{DC}}{2} i \dfrac{2n + in}{\pi(n^2 - 1)}, & n > 1, \text{ even}, \\ \dfrac{I_{DC}}{n\pi} i, & n > 1, \text{ odd}, \end{cases} \tag{3}$$

where I_{DC} is the DC drain current component, and

$$V_n = \begin{cases} V_{DC}, & n = 0, \\ |\Psi_n| e^{j\arg(\Psi_n)}, & \text{otherwise}, \end{cases} \tag{4}$$

where Ψ_n assume the following expression:

$$\Psi_n = \begin{cases} \dfrac{I_{DC}}{2\pi^2 f C_1}\left(\dfrac{\pi^2}{8} - 1 - i\dfrac{\pi}{4}\right), & n = 1, \\ \dfrac{I_{DC}}{2\pi^2 f C_1}\left(\dfrac{2n + in}{2n(1 - n^2)}\right), & n > 1, \text{ even}, \\ \dfrac{I_{DC}}{2\pi^2 f C_1}\left(-\dfrac{1}{n^2}\right), & n > 1, \text{ odd}. \end{cases} \tag{5}$$

Therefore, the optimum fundamental impedance Z_1 (see Fig. 1) to be synthesized at the switch terminals to fulfil Class E requirements is simply expressed by the ratio between fundamental frequency components of device voltage and current, given by

$$Z_1 = \frac{V_1}{I_1} = \frac{0.35}{2\pi f C_1} e^{j36^\circ} = Z_E \| \frac{1}{j2\pi f C_1}. \tag{6}$$

From the above analysis, it is worth noting that a dependence on frequency only appears in the voltage Fourier coefficients, while current coefficients are unaffected. This would suggest some consequence on high-frequency Class E design and it has been exploited in the presented analysis, leading to interesting conclusions reported in the following.

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B) High frequency-domain analysis

Closed-form expressions and the use of a very simple load network justify the attractiveness of the Class E approach. However, even considering ideal conditions for the output matching network and waveforms, a frequency limit in Class E operation can be inferred [4, 8], depending upon bias voltage, device maximum current, and device output capacitance C_{ds}. An approximate expression is given here:

$$f_{Max} = \frac{I_{DC}}{2\pi^2 C_1 V_{DC}} \approx \frac{I_{Max}}{56.5 C_1 V_{DC}}. \quad (7)$$

Being a lower limit of C_1 represented by the device output capacitance C_{ds}, the Class E operating frequency is intrinsically limited by the active device itself. Above this maximum frequency, Class E wave shaping is no longer satisfied and the ideal Class E behavior could not be obtained.

This limitation has to be taken into account, especially for micro- and millimeter-wave applications. Usually, at these frequencies the switching behavior of any active device suffers from the presence of parasitic effects, which tend to increase switching time transitions, resulting in low-pass filtering behavior. Hence, the loss of higher frequency voltage components does not allow the desired wave shaping, with a consequent degradation in power and efficiency levels.

As a consequence, considering the active device as the parallel connection of a perfect switch and the parasitic capacitance C_{ds}, the higher voltage harmonics are assumed as effectively shorted by C_{ds} and only a few harmonic loads can be reasonably controlled [4, 9]. At the same time, the current waveform can still be considered unaffected. The resulting drain voltage and current waveforms are depicted in Fig. 3.

Although still representing a good approximation of Class E behavior [9], it is clear from Fig. 3 that the new drain voltage waveform does not fulfil ZVS and ZVDS conditions [8]. Moreover, device physical constraints are violated, since negative values on the voltage waveform are observed. As pointed out in [8, 10], two solutions can be adopted in order to optimize the drain voltage waveform, while avoiding the occurrence of negative values. Obviously, it is possible to increase the drain bias voltage, but this would mean a nonnegligible increase in the DC dissipated power with a consequent degradation of output performance. In addition, an increased peak voltage value could exceed breakdown limitations of the transistor. A second strategy consists in the optimization of the Z_1 value, assuming that the current components previously determined are unchanged, in order to meet the device limits and without losing Class E behavior.

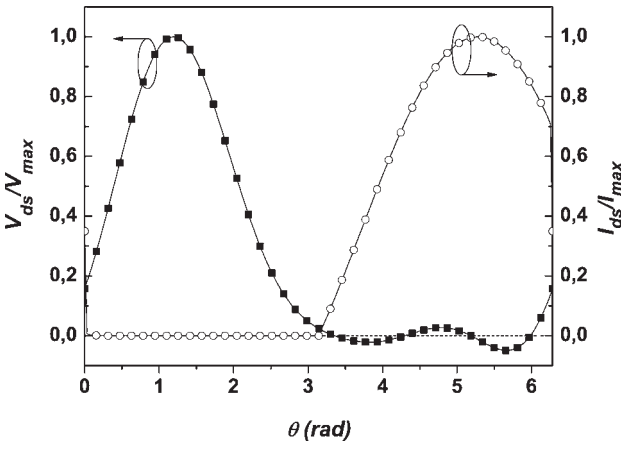

Fig. 3. Drain waveforms considered in the analysis: the current is unaffected, while the voltage is truncated at the third order.

Then, a numerical algorithm has been developed, in order to overcome the limitations related to C_{ds} and to extend the Class E approach above its maximum operating frequency, as described in the following section.

III. DEVELOPED ALGORITHM

Using the above-described frequency domain approach, voltage and current expressions are written as functions of circuit parameters, and in particular as functions of output capacitance C_1. Without loss of generalization, the following assumptions are possible:

1) the switch has zero on-resistance and infinite off-resistance,
2) a purely sinusoidal current still flows into the load (i.e. the band-pass filter in the output network is ideal); and
3) the harmonic loads are only due to the output capacitance C_1.

Defining harmonic load at every harmonic component as

$$Z_n = \frac{V_n}{I_n}, \quad (8)$$

the voltage waveform can be rewritten as the sum of contributions of current at each harmonic multiplied by the respective value of impedance, assuming $\theta = \omega t$:

$$v_{DS}(\vartheta) = V_{DD} - 2\mathrm{Re}\left(\sum_{n=1}^{\infty} Z_n I_n e^{jn\vartheta}\right). \quad (9)$$

Based on the above-listed assumptions, the impedance presented at each harmonic after the first one is only due to the capacitance C_1. Thus the above expression (9) is modified into the following:

$$v_{DS}(\vartheta) = V_{DD} - 2\mathrm{Re}\left(Z_1 I_1 e^{j\vartheta}\right) - 2\mathrm{Re}\left(\sum_{n=2}^{\infty} \frac{1}{j2\pi n f C_1} I_n e^{jn\vartheta}\right). \quad (10)$$

When operating below f_{Max}, at fundamental frequency it is possible to provide an expression for Z_1:

$$Z_1 = Z_E \| Z_C = \frac{0.35}{2\pi f C_1} e^{j36^\circ}. \quad (11)$$

When operating at high frequencies, usually above a few gigahertz, the high-order harmonics – above third order – can be considered as effectively shorted because of the presence of C_1, and their effect neglected. This results in truncating at the third order the expression describing the voltage waveform.

Thus the drain voltage expression is rewritten, introducing a normalization parameter, k, defined as the ratio between

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actual operating frequency and maximum frequency ($k = \omega/\omega_{\mathrm{Max}}$) rated from a time domain analysis [4]. The parameter k is assumed to be greater than or equal to unit, to adequately describe the PA behavior at and above f_{Max}:

$$v_{DS}(\vartheta) = V_{DD} - 2\mathrm{Re}\left(Z_1 I_1 e^{jk\vartheta}\right) - 2\mathrm{Re}\left(\sum_{n=2}^{3} \frac{1}{jnk\omega C_1} I_n e^{jnk\vartheta}\right). \quad (12)$$

Then, considering capacitance C_1 to be constant and the bias point to be given by V_{DD} and I_{DC}, the proposed solution implies finding the optimum value of Z_1 in order to simultaneously satisfy the following conditions:

1) to prevent negative voltage on the drain and
2) to maximize the amplitude of the fundamental component of drain voltage, and consequently the output performances.

As a first step, a discrete formulation for the function $v_{DS}(t)$ has been derived:

$$v_{DS}(m) = V_{DD} - 2\mathrm{Re}\left(Z_1 I_1 e^{jm2\pi/M}\right) - 2\mathrm{Re}\left(\sum_{n=2}^{3} \frac{1}{jnk\omega C_1} I_n e^{jnm2\pi/M}\right) \quad (13)$$

taking into account the relationship

$$k\theta = 2\pi\frac{m}{M} \quad (14)$$

so that the number of samples of v_{DS} is equal to M in a period, regardless of actual frequency. Nonetheless, the dependence on operating frequency still appears in the higher harmonics impedance expression. In order to maintain a good approximation, the number of samples per period M was chosen relatively high and equal to 200.

Then, the unknown fundamental impedance Z_1 was written in a polar form and its value was swept around the ideal one. In particular, the magnitude was varied in a range 0.1–1.9 times the ideal value and the phase was varied between -90 and 90° in steps of 1°, so assuming whatever realizable value using passive components. Therefore,

$$\begin{cases} Z_1 = |Z_{1,ideal}|\Delta Z e^{j\Delta\Phi} \cong \dfrac{0.35}{\omega C_1}\Delta Z e^{j\Delta\Phi}, \\ \Delta Z \in \left[\dfrac{1}{10}, \dfrac{19}{10}\right], \\ \Delta\Phi \in \left[-\dfrac{\pi}{2}, +\dfrac{\pi}{2}\right]. \end{cases} \quad (15)$$

Function $v_{DS}(m)$ was numerically computed inferring at the end the couples of ΔZ and $\Delta\Phi$ that avoid negative values in the voltage waveform and simultaneously maximize the amplitude of the fundamental component of the drain voltage, so determining the optimum load for Class E operation at selected normalized frequency. The process was iterated for k going from 1 to 5 in steps of 0.1, obtaining a plot of impedance variation versus normalized frequency.

Figure 4 reports the ΔZ and $\Delta\Phi$ behaviors as a function of k. A quasi-monotonic decrease in the variation of the magnitude of fundamental impedance is observed, leading to a consequent decrease in the fundamental voltage amplitude as well as in maximum drain voltage. The phase behavior is monotonically decreasing, causing almost purely resistive impedance at the fundamental harmonic as the frequency increases.

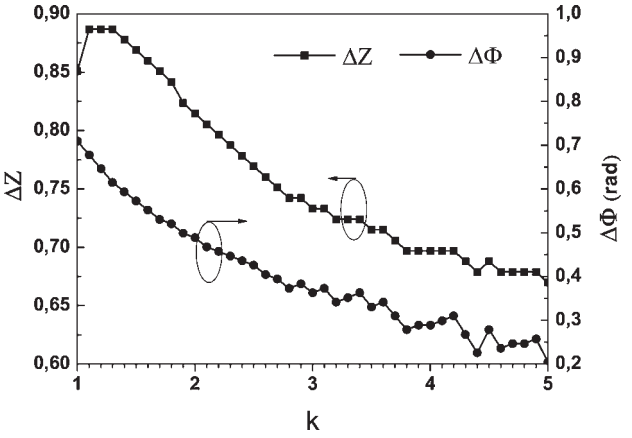

Fig. 4. ΔZ and $\Delta\Phi$ behaviors as a function of k.

The resulting drain efficiency, reported in Fig. 5, is significantly different from unity, due to the nonideal operating conditions that a finite number of harmonics causes even for $k = 1$. The main reason for efficiency decrease is the lower value of fundamental voltage amplitude with respect to the ideal one.

A peak value of the drain efficiency is observed at 1.6 times the maximum frequency, resulting in a combination of voltage and current that effectively minimizes the power dissipated in the transistor.

The above analysis suggests a useful and immediate approach in the design of a high-frequency Class E PA, improving the closed-form relationships of the classical methodology.

IV. PA DESIGN AND REALIZATION

Based on the results obtained previously, and in order to validate the developed algorithm, a Class E PA was designed at 2.14 GHz, using a medium-power LDMOS transistor. The

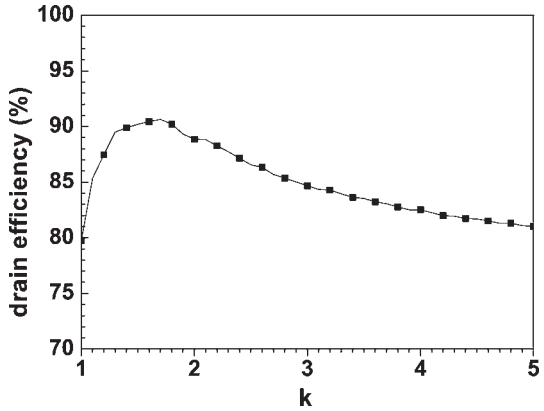

Fig. 5. Drain efficiency as a function of normalized frequency.

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device non-linear model was available from the foundry, allowing direct access to the intrinsic section.

The bias point was chosen in order to maintain the Class E operating point within the physical limits of the device. Maximum current and breakdown voltage are, respectively, 2.5 A and 70 V, estimated by DC simulation on the device model. The theoretical Class E boundary conditions impose

$$V_{DC} \leq V_{Break}/3.562,$$
$$I_{DC} \leq I_{Max}/2.862.$$

Thus a V_{DC} of 20 V and a V_{GS} of 3.3 V ($I_{DC} = 800$ mA) were chosen. The device output capacitance C_{ds} was estimated by S-parameter simulations in 4.2 pF. This implies a maximum frequency of about 520 MHz for pure Class E conditions.

The ideal Class E impedance is $Z_1 = 25.1e^{j36^\circ}$, calculated at the intrinsic section of the active device.

Since the nominal frequency chosen for the design was 4.1 times greater than the maximum one allowable for Class E ideal operation, as can be deduced from Fig. 4, a decrease of 30% in magnitude and an absolute phase of 17° are expected for high-frequency Class E impedance. Initial values of load impedance, determined in simulation with ideal harmonic tuners, effectively demonstrate the pertinence of the used approach. An optimum impedance of $Z_{1,opt} = 17.5e^{j17^\circ}$ was obtained.

Simulated performance at the intrinsic drain section is reported in Fig. 6, showing a maximum efficiency of about 76%, slightly less than the value expected from Fig. 5. In fact, the knee voltage effect (i.e. on-resistance value) has been omitted in the algorithm for the sake of simplicity, but it has some influence on the overall performance when it is not negligible.

Simulated drain voltage and current waveforms and intrinsic load line are reported in Fig. 7, demonstrating a good approximation of ideal Class E behavior even above f_{Max}.

An essential schematic of the amplifier is reported in Fig. 8. The output matching network was designed to present the optimum load at the intrinsic section of the transistor. It was synthesized using a hybrid approach, with the use of surface mounting lumped elements. Additional work was performed on the input matching network to assure unconditional stability (by resistors R_1 and R_2 in Fig. 8) and the conjugate input matching of the PA. Then, both networks were implemented on a commercial substrate ($\varepsilon_r = 10$, $h = 640$ μm). The realized PA is depicted in Fig. 9.

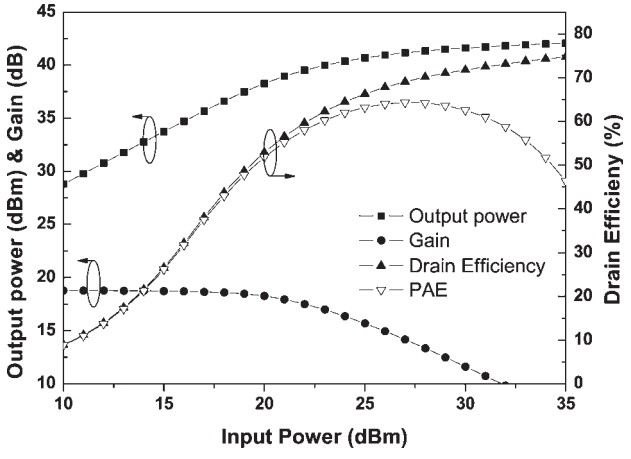

Fig. 6. Simulated output performance at the intrinsic section.

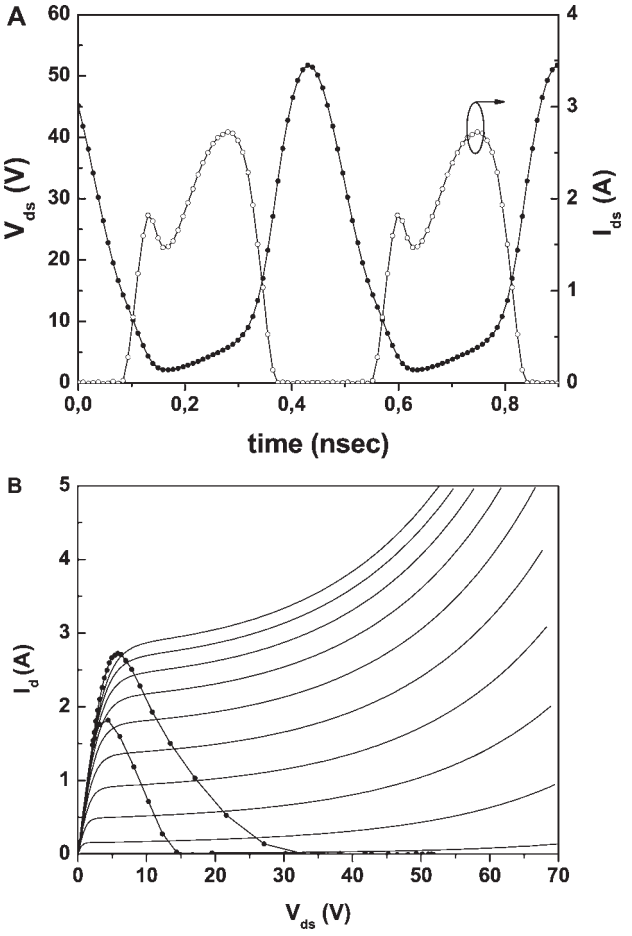

Fig. 7. Simulated drain waveforms (a) and load line (b).

V. EXPERIMENTAL RESULTS

Linear and nonlinear measurements were finally performed on the realized PA and compared with simulations with non-ideal circuit elements at the nominal bias point ($V_{DC} = 20$ V and $I_{DC} = 800$ mA).

Measured small signal S-parameters are reported in Fig. 10, showing good agreement with the simulations.

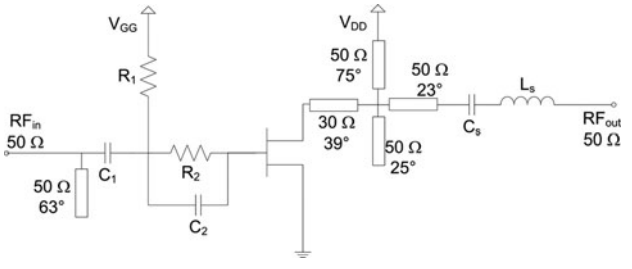

Fig. 8. PA schematic.

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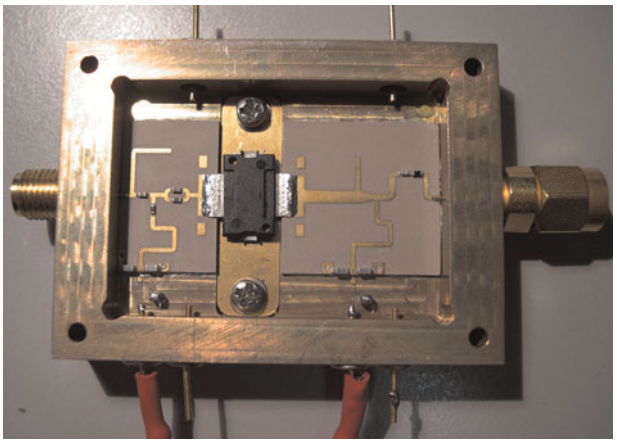

Fig. 9. Photograph of the realized PA.

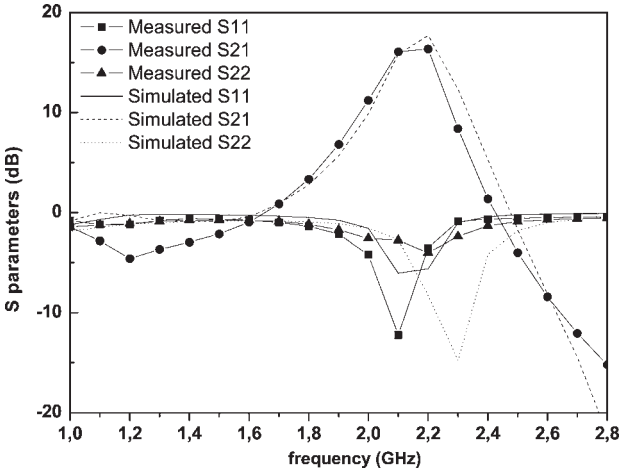

Fig. 10. *S*-parameters simulations and measurements.

Large signal measurements were performed at 2.14 GHz using continuous wave excitation. As a consequence, the amplifier should be considered to operate in Class E only when reaching a deep compression level, i.e. above 25 dBm of input power, with reference to Fig. 11.

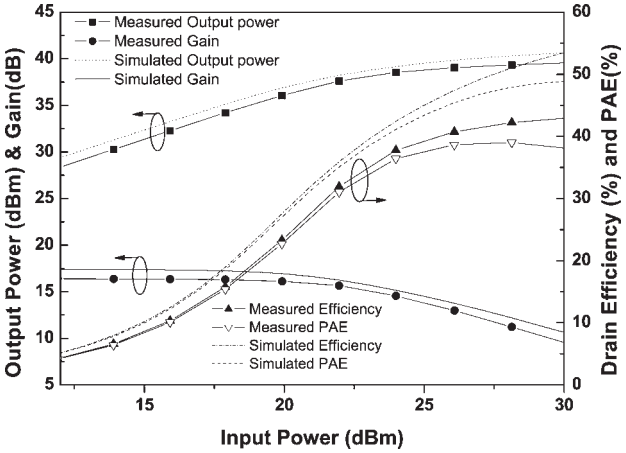

Fig. 11. Output performance of the designed PA at 2.14 GHz at nominal bias point.

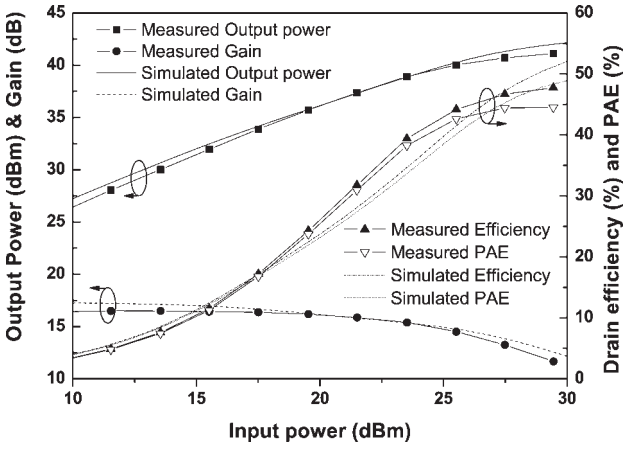

Fig. 12. Output performance of the designed PA at 2.14 GHz at $V_{DC} = 26$ V.

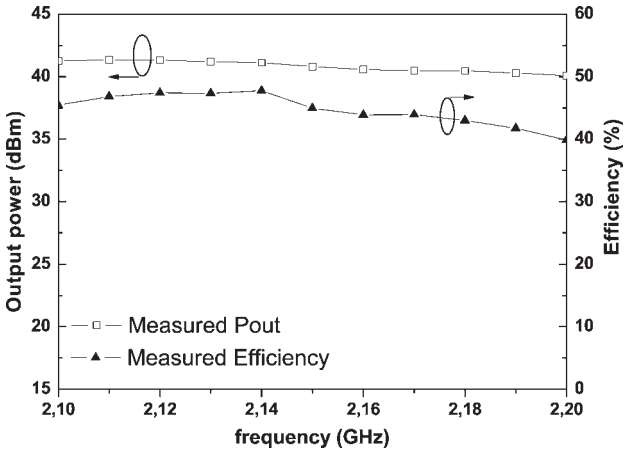

Fig. 13. Output performance as a function of frequency.

From Fig. 11, an appreciably lower measured efficiency and PAE as compared to simulation (40% instead of 56%) is evident. In fact, the measured output power is about 1 dB lower than the simulated value (39.8 dBm against 40.7 dBm at 30 dBm input power), and above all the actual DC current absorption predicted by the nonlinear model of the active device was lower than that measured, causing a decrease in efficiency.

Try to increase efficiency, further measurements were performed with a slightly higher drain bias voltage and at a lower bias current, i.e. $V_{DC} = 26$ V and $I_{DC} = 500$ mA. Measurements against simulations are depicted in Fig. 12. In such conditions, the amplifier can reach 41 dBm of output power and a maximum efficiency of 49% at 2.14 GHz.

In Fig. 13, plots of drain efficiency and output power versus frequency are reported, measured in the frequency range of 2.1–2.2 GHz at a constant gain of about 11 dB, namely in the Class E operating region.

VI. CONCLUSION

In this paper analysis on the high-frequency Class E design approach was presented. Starting from the classical approach, a numerical analysis, based on the optimization of the

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fundamental impedance, was performed to extend Class E feasibility at higher frequencies. The method developed was validated designing a PA based on an LDMOS device, at a frequency 4.1 times higher than the maximum allowable for a traditional Class E design. The PA was realized and characterized, showing an output power of 10 W with an associated efficiency of 49% over a 100-MHz bandwidth.

REFERENCES

[1] Sokal, N.O.; Sokal, A.D.: Class E – a new class of high efficiency tuned single ended switching power amplifiers. IEEE J. Solid State Circuits, **10** (1975), 168–176.

[2] Ui, N.; Sano, S.: A 45% drain efficiency, −50 dBc ACLR GaN HEMT Class-E amplifier with DPD for W-CDMA base station, in 2006 IEEE International Microwave Symposium Digest, June 2006, 718–721.

[3] Narisi Wang; Xinli Peng; Yousefzadeh, V.; Maksimovic, D.; Pajic, S.; Popovic, Z.: Linearity of X-band class-E power amplifiers in EER operation. IEEE Trans. Microwave Theory Tech., MTT-53, **3** (Part 2) (2005), 1096–1102.

[4] Mader, T.B.; Bryerton, E.W.; Markovic, M.; Forman, M.; Popovic, Z.: Switched-mode high-efficiency microwave power amplifiers in a free-space power-combiner array. IEEE Trans. Microwave Theory Tech., MTT-46, **10** (Part 1) (1998), 1391–1398.

[5] Popp, J.; Lie, D.Y.C.; Feipeng Wang; Kimball, D.; Larson, L.: Fully-integrated highly-efficient RF Class E SiGe power amplifier with an envelope-tracking technique for EDGE applications, in Proc. Radio and Wireless Symp., January 2006, 231–234.

[6] Milosevic, D.; van der Tang, J.; van Roermund, A.: A high-efficiency HBT-based class-E power amplifier for 2 GHz, in Proc. Gallium Arsenide and Other Semiconductor Application Symp., 2005, EGAAS 2005, Paris, France, October 2005, 45–48.

[7] Litwin, A.; Chen, Q.; Johansson, J.; Ma, G.; Olofsson, L.A.; Perugupalli, P.: High power LDMOS technology for wireless infrastructure, in Proc. Gallium Arsenide Applications Symp., GAAS 2001, London, September 2001.

[8] Colantonio, P.; Giannini, F.; Giofrè, R.; Yarleque Medina, M.A.; Schreurs, D.; Nauwelaers, B.: High frequency Class E design methodologies, in Proc. Gallium Arsenide Applications Symp., GAAS 2005, Paris, France, October 2005, 329–331.

[9] Raab, F.H.: Class-E, Class-C and Class-F power amplifiers based upon a finite number of harmonics. IEEE Trans. Microwave Theory Tech., MTT-49 (2001), 1462–1468.

[10] Cipriani, E.; Colantonio, P.; Giannini, F.; Giofrè, R.: Optimization of Class E power amplifiers above theoretical maximum frequency, in Proc. European Microwave Conf., EuMC 2008, Amsterdam, The Netherland, October 2008, 1541–1544.

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