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RESEARCH PAPER

GaN HFET MMICs with integrated Schottky-diode for highly efficient digital switch-mode power amplifiers at 2 GHz

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This work describes the integration of Schottky diodes into fast GaN MMIC process technology suitable for the realization of switch-mode power amplifier core chips for class-S operation at 2 GHz. With the demonstration of this technology, the so-called third-quadrant issue, which reduces the efficiency in band pass-Δ-Σ class-S operation can be diminished on device level. Compared to a hybrid diode assembly, the broadband properties of the amplifier module with on-chip-integrated diode can be improved by the reduction of parasitic losses. The GaN heterostructure field effect transistors (HFETs) with integrated series diode show a cut-off frequency of 28 GHz with drain breakdown voltages exceeding −100 and +100 V and comparable large signal performance to conventional GaN HFETs at 10 GHz. MMIC core chips for class-D and class-S switch-mode power amplifier modules are demonstrated for the operation at mobile communication frequencies between 0.45 and 2 GHz and signal bit rates up to 8 Gbps. The circuits yield broadband output power levels between 4 and 9 W with efficiencies of up to 80%.

Keywords: power amplifier, switch mode, gallium nitride, mobile communications, integrated diode, MMIC, class-S

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I. INTRODUCTION

Switch-mode amplifiers have been suggested to provide another leap in efficiency of power amplifiers (PAs) for mobile communications [1–5]. The realization of high-efficiency switch-mode PAs at a frequency of 2 GHz demands a power transistor with low output capacitance, high current capability, and high breakdown voltage which operates up to multiple harmonic frequencies. Because of its unique material properties the GaN-based heterostructure field effect transistor (HFET) technology combines high operation frequency and high output power [6, 7], and therefore becomes a favorable candidate for switch-mode applications.

When using advanced digital modulation schemes, e.g. band pass-Δ-Σ (BPDS) modulation, long bit sequences can occur having a constant bit level longer than one RF-period given by the output filter [8]. In case of utilizing a current-mode PA output stage these long constant bit sequences force the output transistors in the third-quadrant operation, namely a negative voltage at the drain of the devices. As delineated below, for conventional Schottky-gate HFETs a negative V_{DS} (with $V_{DS} < V_{GS}$) leads to a strong forward conduction of the gate–drain diode, which on the one hand causes a distortion of the RF signal, and on the other hand may result in the destruction of the device.

Thus in this work the integration of a series high-voltage Schottky-diode in the HFET device is investigated to suppress the undesired effects of the third-quadrant operation. A characterization of these new series diode HFETs (SD-HFETs) on device level will show the suitability for their implementation in switch-mode amplifiers. Based on this device, high-efficiency digital switch-mode PA monolithic microwave integrated circuit (MMIC) were designed for application in current-mode class-S amplifiers for operation in the mobile communication frequency range up to 2 GHz.

II. APPROACHES TO THE CLASS-S THIRD-QUADRANT ISSUE

In a class-S amplifier a digital data stream, generated by a BPDS modulator, is amplified by a high-efficiency differential amplifier and reconstructed by a filter to an analog output signal. Closing the gap between the low-power modulator and the GaN PA MMIC input, recently, a high-power preamplifier based on SiGe heterostructure bipolar transistor (HBT) was presented, able directly to drive a GaN input stage [9]. The BPDS-modulated signal requests a very high signal bandwidth. The frequency spectrum of the BPDS signal is defined from nearly direct current (DC) to at least third harmonic, when using a signal over sampling of about 2.5 [10].

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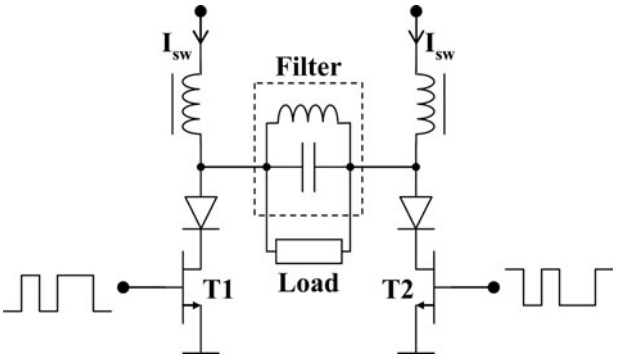

Fig. 1. Principle schematic of a current-mode class-S amplifier.

Therefore, a signal bit rate of about 5.2 Gbps is needed for a desired application in mobile communications, e.g. at 2 GHz fundamental.

The current-mode class-S amplifier, depicted in Fig. 1, is an amplifier class susceptible to the third-quadrant issue [8]. The third-quadrant issue for current-mode class-S amplifiers is related to the long constant bit sequences as mentioned before. While the PA output current is switched simultaneously to the input bit stream, the frequency and shape of the output voltage are dictated by the output reconstruction filter. Besides, the total current I_{sw} is set by the supply current source. For example during a long on-condition for the current at T1, the output voltage independently alternates driven by the resonating filter. The typical load lines of properly operating switches for class-S operation are shown in Fig. 2. The switching transistor T2 (in off-condition) is forced to negative V_{DS} by the output filter (marker 1), whereas T1 (in on-condition) keeps providing a constant on-state current (marker 2). This negative drain voltage for T2 is described as the third-quadrant issue in this work. Note that for simplified visibility the voltage for T1 is drawn with negative values, since it mainly provides the negative part of the voltage waveform to the load. However, the present drain–source voltage at T1 is positive in this example.

For a conventional HFET, a negative drain voltage drives the gate–drain diode of T2 into forward conduction, resulting in a critical device state with a high negative drain/gate current and

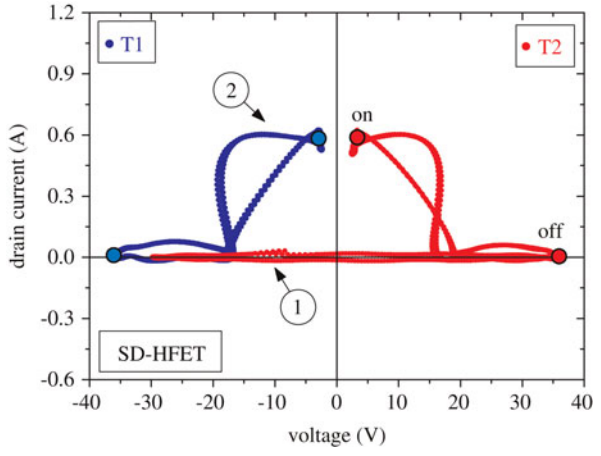

Fig. 2. Simulated load lines of a properly performing switch device operating in class-S amplifier configuration, e.g. the SD-HFET presented in this work, a HFET with integrated diode connected in series.

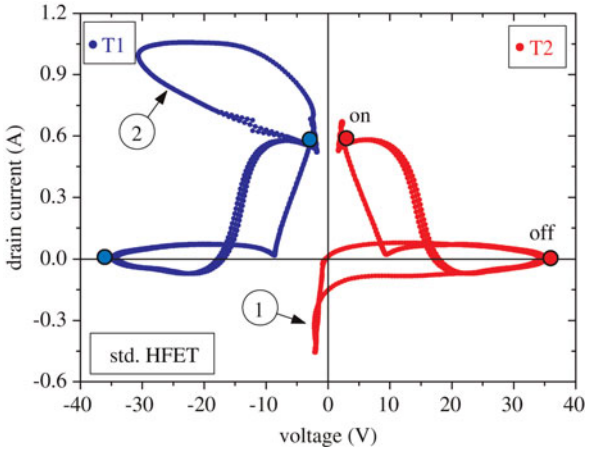

Fig. 3. Simulated load lines for conventional HFET switch device operating in class-S amplifier configuration.

a very low negative drain voltage. Typical load lines related to the described behavior are shown in Fig. 3. However, the resonating filter still dictates the output voltage and the current I_{sw} is constant. Therefore, the on-switched T1 is forced to balance the negative current of T2 and to provide simultaneously the high voltage at the output. Finally, T1 is driven to a highly lossy state with high current and high voltage at the same time (marker 2), while the gate–drain diode of T2 is compromised by the high forward current (marker 1).

To avoid this destructive effect for the HFET switch, usually an external hybrid blocking diode is implemented in series in the amplifier module. However, an external diode solution is very challenging since the amplifier broadband capability will be degraded by additional parasitics, e.g. bond wire inductances and the large separation distance between the switch and filter. Further, a compact high-current, high-voltage, and high-speed diode is needed. Therefore, an integrated solution is favorable for preserving a high-bandwidth, -speed, -efficiency, and high output power.

Possibilities on device level solving this issue by blocking the negative drain voltage are: (a) an integration of a series diode (SD) in the transistor [11], or (b) on the amplifier MMIC, or (c) an introduction of a high forward-voltage-resistant gate insulator. In the case of GaN, gate insulators were extensively studied recently for so-called MISHFETs (metal–insulator–semiconductor HFETs) [12, 13]. Nevertheless, under forward bias of the insulated gate diode, only low voltages in the range of 10 V can be applied due to the required thin insulator layer thickness. No results were shown yet for both, a high forward voltage bias and a high reverse breakdown voltage. The integration of a SD into the transistor was realized in this work by the development of the SD-HFET.

Figure 4 visualizes the improvement in the class-S switch-mode PA module built-up by a higher degree of integration on device and functionality level, which is enabled by the SD-HFET. First, the electrical parasitics are reduced compared to a hybrid diode module due to the absence of bond wire connections and a reduced size of the module area and therefore less unwanted impedance transformation or frequency dispersion. Further, the enabled integration of filter elements on the MMIC allows the realization of high-performance output filter solutions with improved parasitic resonance frequency and higher operation frequencies.

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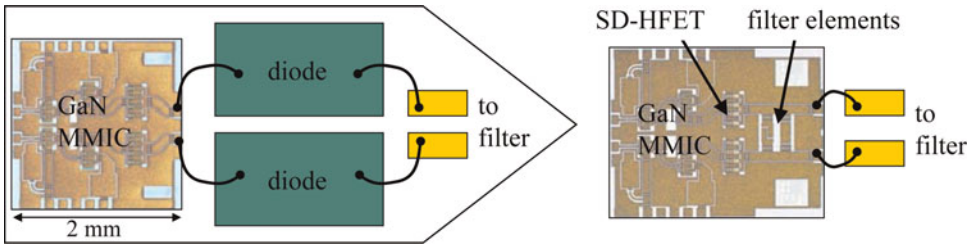

Fig. 4. Reduced size and parasitics of integrated diode solution versus hybrid diode on class-S amplifier module level.

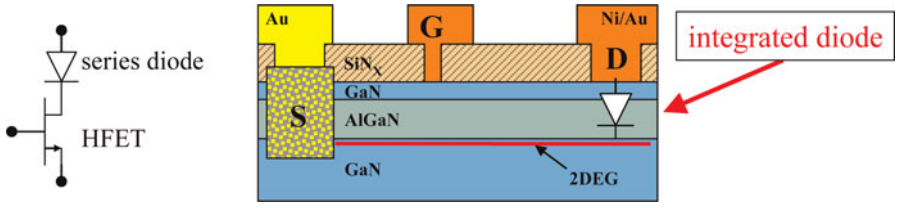

Fig. 5. Schematic and schematic cross section of a GaN HFET with integrated series Schottky diode (SD-HFET).

III. GaN MMIC TECHNOLOGY WITH SD-HFETs

The epitaxial structures used in this work were grown by metal-organic chemical wafer deposition (MOCVD) on 3-inch semi-insulating SiC substrates. The layers consist of a highly resistive *c*-plane GaN buffer, followed by a 25 nm barrier layer of $Al_{0.22}Ga_{0.78}N$ and a thin GaN cap layer. Room temperature Hall-measurements on the two-dimensional electron gas (2DEG) formed at the buffer to barrier interface resulted in a sheet resistance, a sheet carrier concentration, and a mobility of 500 Ω/sq, 8×10^{12} cm^{-2}, and 1600 cm^2/(V s), respectively. The processing is based on a 0.25 μm GaN HFET device technology [7, 14]. The ohmic contacts were formed by rapid thermal annealing, resulting in a low contact resistance of 0.2 Ω·mm. The Schottky diodes provide a barrier of 1.2 eV with an ideality factor of <1.5, and are used for both gate and Schottky-drain contacts. The nitride assisted T-gate with a gate length of 0.25 μm was defined by e-beam lithography. Furthermore, the coplanar transmission line MMIC passive process includes NiCr based 50 Ω/sq thin film resistors, metal–insulator–metal (MIM) capacitors as well, as a thick plated Au-based air bridge technology.

IV. GaN SD-HFET DEVICE

All devices presented in this work are based on the Schottky-drain approach for realizing a SD integrated in the HFET. GaN HFETs with regular ohmic drain contacts are added for comparison on the same wafer. Figure 5 gives the schematic of the Schottky-drain approach. Contrary to the classical formation of the ohmic contact, a second Schottky contact is employed at the drain contact, which forms the integrated diode in series.

A) Impact of the integrated Schottky-diode under DC operation

Typical output characteristics of a SD-HFET and a conventional HFET are compared in Fig. 6. Compared to the HFET, one can note the two main effects caused by the integrated diode: first, a highly reduced drain current under negative drain voltage, the main purpose of the diode. Second, the diode characteristic of the active device region, which causes a parasitic increase of the effective on-resistance of the SD-HFET due to the diode forward voltage drop.

Figure 7 gives a more detailed insight on the reverse voltage behavior of the SD-HFET. The measurements clearly show the excellent current blocking behavior of the SD-HFET, at elevated ambient temperature of 100°C. In this case the off-state currents ($V_{GS} = -4$ V) under negative drain bias as well as under positive drain bias are well below a value of 1 mA/mm.

However, in on-state conditions, the integrated Schottky-diode approach leads to an increase of the effective on-resistance (R_{on}), once the Schottky diode is forward biased. As shown in Fig. 6, the diode's forward voltage drop causes a relatively higher R_{on} for the SD-HFET at low drain currents. The rising drain current reduces the effective R_{on} nonlinearly.

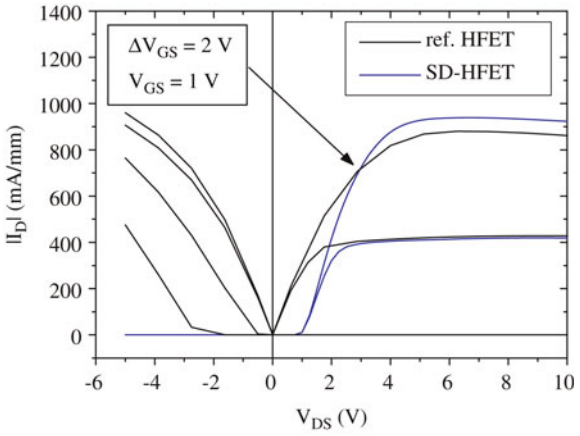

Fig. 6. Measured DC output characteristics of a conventional GaN HFET (reference) and a GaN SD-HFET under negative and positive drain voltage conditions (absolute current values).

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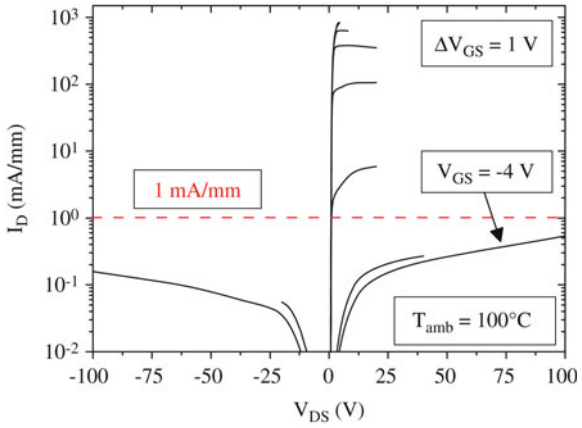

Fig. 7. Measured DC output characteristics at 100°C ambient temperature of a GaN SD-HFET ($W_G = 1.2$ mm) under negative and positive drain voltage conditions in logarithmic scale (absolute current values).

Derived from measured output characteristics, the R_{on} dependency on the drain current for SD-HFETs is compared to conventional HFETs in Fig. 8. The conventional HFET shows nearly constant R_{on} for low drain currents, followed by a continuous increase of R_{on} with a strong increase in saturation. However, for the SD-device a rising drain current in on-state reduces the effective R_{on} to a broad minimum at high drain current values. Consequently, the negative influence of the increased R_{on} on the efficiency and available output power for SD-HFETs is mitigated for high operation currents.

Employed in a switch-mode amplifier, the on-resistance of a GaN switching transistor is the main cause of static losses. Therefore, the use of the SD increases static losses due to the increased effective on-resistance. To partially compensate the static loss resulting from the diode, a scaling of the transistor towards reduced on-resistance is applied in parallel to the diode integration. The on-resistance reduction was applied with respect to a preserved breakdown voltage >100 V. The results are shown in Fig. 8. The reference HFET device shows a typical on-resistance of 3 Ω·mm at medium drain current (600 mA/mm). A successfully scaled HFET device obtains a reduced R_{on} of about 2 Ω·mm. Based on a comparable design to achieve the identical reduced nominal on-resistance, a minimal value of 4.5 Ω·mm was measured for the SD-HFET for a drain current between 500 to 950 mA/mm. Furthermore, at high drain current (>800 mA/mm) the SD-HFET achieves an on-resistance comparable to the reference HFET without integrated Schottky diode and non-reduced on-resistance.

B) RF measurements of SD-HFETs

Small-signal measurements were performed on SD-HFETs as well as conventional HFETs as reference, both with a total gate width of 1.2 mm. Figure 9 illustrates the results for the different FETs versus the nominal on-resistance. While a reduction of the parasitic resistances in the HFET slightly increases the small-signal current-gain (h_{21}) as well as the maximum stable gain (MSG) and maximum available gain (MAG), the integration of the diode leads to a reduction of these parameters. Additional parasitic capacitances in the SD-HFET contribute to the decrease of the small-signal gain. Compared to a reference HFET with an on-resistance of 3 Ω·mm, the MSG of the SD-HFET deteriorates by less than 0.5 dB. The impact on h_{21} can be directly seen by the drop in the current-gain cut-off frequency f_T from 31 to 28 GHz, measured at $V_{DS} = 7$ V. However, no influence on the transition frequency MSG/MAG was observed for the devices measured at the operation bias of 30 V. Therefore, one can expect relatively small difference in terms of device speed and broadband capabilities of the compared transistors.

CW-large-signal load pull measurements performed at 10 GHz show a slight reduction of the output power and power added efficiency (PAE) due to the integration of the diode (Fig. 10). SD-HFETs (conventional HFETs) obtain a maximum output power of 4.9 W/mm (5.4 W/mm) and a PAE of 48% (50%) for a drain-bias voltage of 30 V.

The SD devices, however, provide a loss in RF gain of 0.5 dB, which can be attributed to the reduction of MSG/MAG based on the drain resistance increase and the capacitance added. A linear gain of 13 dB was measured for the SD-HFET. Tuning the SD device for optimal PAE yields load impedances for the standard HFET (120 $\Omega \cdot e^{j64}$), which are slightly different from the SD-HFET (105 $\Omega \cdot e^{j67}$).

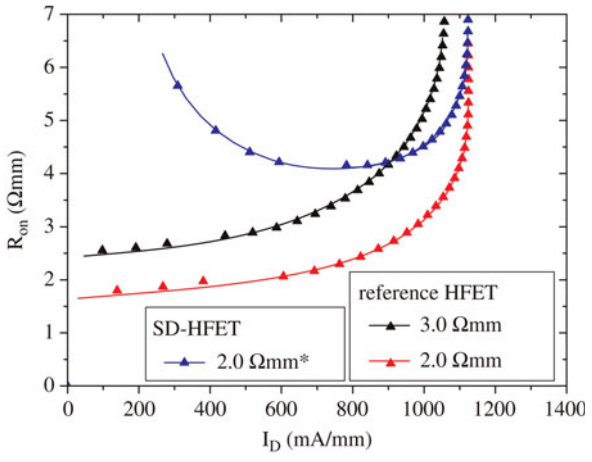

Fig. 8. Effective device on-resistance versus drain current for conventional HFETs as reference and SD-HFETs for devices with different nominal on-resistance values (* nominal value).

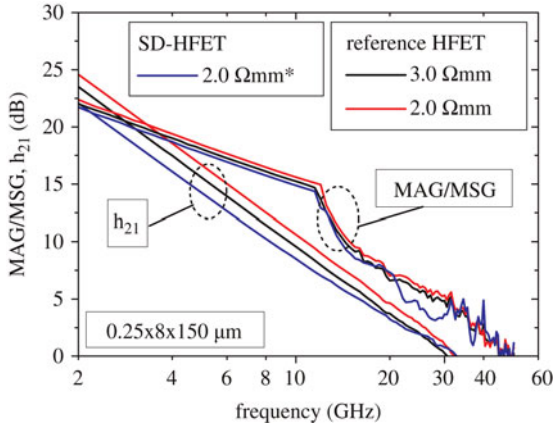

Fig. 9. Measured small-signal gain at peak transconductance of SD-HFETs and conventional HFETs as reference for devices with different nominal on-resistance values (V_{DS}: 7 V for h_{21} and 30 V for MAG/MSG).

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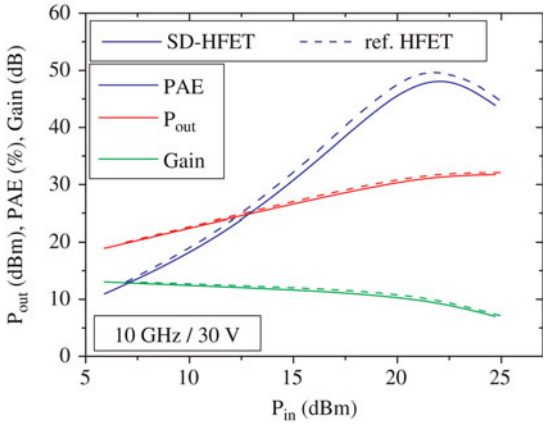

Fig. 10. Measured large signal characteristics at 10 GHz and 30 V drain bias for a GaN SD-HFET and a conventional HFET ($W_G = 0.3$ mm).

C) Summary of device characteristics

The main device properties of the SD-HFET in comparison to the standard HFET are given in Table 1. In summary, with the standard HFET, the gate–drain diode opens under forward operation for negative drain–source voltage exceeding V_{GS}. The resulting high gate-current leads to device damage or even destruction. The power dissipated in the gate is further a strong loss mechanism for switch-mode operation. Concerning the amplified RF signal, the signal distortion by the forward conduction of the gate drain diode also generates intermodulation products in the output signal [8].

For the SD-HFET, the integrated series Schottky diode operates in reverse during the critical negative V_{DS}, therefore, only small reverse currents are dissipated through the SD and no signal distortion occurs. The additional on-resistance in SD-HFETs is to be traded for the enhanced efficiency, and signal quality in complex digital operation, and reduced parasitics in the amplifier module as discussed above.

V. DIGITAL POWER AMPLIFIER MMIC DESIGN AND PERFORMANCE

Two digital PA MMICs were designed using dual-stage amplifier circuits with an advanced inverter-based driver, as reported in [5]. Conventional HFET devices were used for the driver circuit, since only the output-stage transistor is exposed to the negative drain voltage. The output stage was realized either by a SD-HFET (circuit_3SD) or by a standard device with the same nominal on-resistance of 2 Ω·mm for comparison (circuit_3A). The output stage has a total gate width of 1.6 mm. In Fig. 11 the chip image and schematic of the realized MMIC are shown. Because of the very high signal bandwidth of the BPDS-modulated input signal, no matching circuit can be applied at the input of the MMIC.

Table 1. Device Properties compared for standard HFET and SD-HFET.

	Std. HFET	SD-HFET
$I_{D,max}$(mA/mm)	1050	1100
$g_{m,max}$(mS/mm)	330	330
R_{on} (at $I_D = 600$ mA/mm) (Ω·mm)	3	4.5
BV_{GD} ($T = 100°C$) (V)	>120	>100
$V_{DS\_reverse}$ ($T = 100°C$)	Applied V_{GS}	<− 100 V
f_T(GHz)	31	28
P_{out} (at 10 GHz, 30 V) (W/mm)	5.4	4.9

The circuits are evaluated in digital switching operation driven by a 50 Ω source with a digital bit stream generated by a 12.5 Gbps bit pattern generator (Anritsu MP1758A). Two main signal types are used, a square wave signal representing the class-D equivalent operation, and a BPDS-modulated signal representative for the class-S equivalent operation. All measurements are single-ended digital on-wafer measurements in a broadband 50 Ω environment. Consequently, the given output power is related to the unfiltered signal spectrum. This allows a direct evaluation of the pure MMIC switching behavior without the influences of an output filter or packaging issues. A more detailed description of the measurement method is given in [5].

Figure 12 depicts the measured drain efficiency (DE), circuit PAE, and RF-output power over operating voltage of the MMICs for a square wave operation (class-D). This operation at 0.9 Gbps was used for evaluating the maximum output power capability of the MMICs. Both circuits yield an output power up to 9 W, and a maximum DE of 86% (circuit_3A) and 79% (circuit_3SD). The peak PAE of 80 and 75% is achieved at similar output power levels for the circuit_3A and circuit_3SD, respectively. Nevertheless, the output power at the same voltage is reduced for the circuit with integrated diode. This is due to the forward voltage drop induced loss of integrated SD, which also causes the decrease in efficiency.

Note the different behavior of the DE versus operation voltage. The DE for the circuit with conventional HFET (circuit_3A) steadily decreases, mainly due to increased switching losses. For the circuit with integrated diode (circuit_3SD), the DE increases to a maximum at 18 V due to two competing effects: First, the reduction of the on-resistance and therefore reduced static losses. The on-resistance is influenced by the increase of the on-state current with rising operating voltage. Note that a constant load of 50 Ω is used. As shown in Fig. 8, the on-resistance of a SD-HFET decreases to a minimum value with increased drain current. Consequently, the DE increases with the lower static losses. The second effect is the increased switching loss due to higher voltage amplitudes for a higher operation voltage. The switching loss increase dominates over the static loss reduction above the maximum DE at an operation voltage of 18 V, equivalent to an on-state current of approximately 400 mA/mm.

Representing class-S equivalent digital operation, Fig. 13 gives the measured DE and RF-output power over signal bit rate of the MMICs for a 1-tone BPDS-modulated signal. At the desired bit rate of 5.2 Gbps, comparable to a frequency of 2 GHz, the reference design circuit_3A shows a good DE of 71% at 5 W output power. For the SD-HFET design circuit_3SD the DE and power are reduced to 66% and 4.3 W, respectively. Despite this frequency-independent difference in efficiency and output power, there is no deterioration of the circuit speed visible by integrating the SD-HFET, since the slope of efficiency versus bit rate is equal for both circuit types. This agrees perfectly with the small-signal measurements, where only a small difference in terms of device speed and broadband capabilities of the compared transistors was expected. However, the frequency-independent

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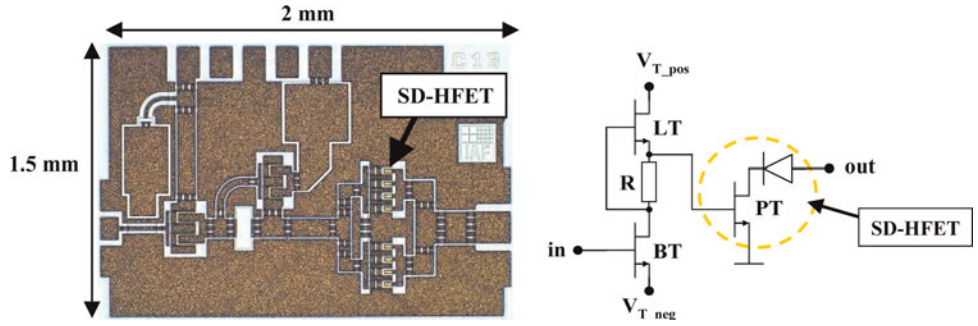

Fig. 11. Chip image and schematic of a digital PA MMIC using a SD-HFET output stage in 0.25 μm gate length technology (chip size 2 × 2 mm²).

deterioration is induced by the higher on-resistance of the SD-HFET devices as mentioned above. The extrapolation of the measurements to a bit rate of zero, equal to zero switching losses, allows the calculation of the effective on-resistance under large signal switching operation. For the considered operating voltage of 20 V, both circuits operate at an average on-state current between 450 and 500 mA/mm. Under the assumption of negligible off-state losses, an effective on-resistance of 3.5 and 6 Ω·mm was extracted for the HFET and SD-HFET based circuit, respectively. The calculated values are about 1.5 Ω·mm higher than the measured DC-values, similar for both circuits. Origins of the increased effective on-resistance are mainly expected from channel temperature increase or dispersion effects. Furthermore, a minor contribution can be correlated to nonzero off-state losses, where an off-state current of 1 mA/mm causes an error of $<$0.3 Ω·mm.

Furthermore, eye diagram measurements in Fig. 14 (identical scale) show reduced signal amplitude at the load for the SD device. The observations lead to reduced output power and efficiency related to an increased R_{on} in the SD devices, as argued before. Supporting the previous statement, no speed deterioration is observed in the slope of the waveforms. The fall time amounts to 54 ps whereas the rise time is 68 ps, equal for both device types. In BPDS mode, the two presented circuits achieve a maximum bit rate of operation of about 5.5 Gbps, evaluated by the eye diagram distortion. This enables the operation of the class-S amplifier at 2 GHz with required over sampling for the BPDS modulation.

It has to be stated that this comparison made so far is not fair to be 1:1, as the MMIC with the standard HFET needs an additional (potentially hybrid) lossy diode to protect itself from self-destruction under operation with a filter in a packaged class-S amplifier operation. Also, the critical broadband requirements of the BPDS-modulated signal are improved tremendously by integrating the diode in the transistor instead of an external connection, e.g. by a frequency-limited bond wire. However, the SD-MMIC can be operated as it is and simplifies the mounting of the full transceiver chain in a module. An integration of passive filter elements on the MMIC will further improve the whole amplifier complexity and performance.

VI. ADVANCED 2 GHZ CLASS-S AMPLIFIER MMIC

Based on the developed SD-HFET, a modified circuit was developed for the application in class-S switch-mode amplifiers operating at 2 GHz. To further increase the switching speed, the gate length of the devices was reduced to 0.15 μm and the total output gate width of the circuit was reduced to 1.2 mm. As consequence, the switching performance at high bit rates above 4 Gbps was improved. The class-S switch-mode amplifier core MMIC was designed in a differential configuration, which includes integrated capacitive filter elements with high parasitic resonant frequency. The chip photograph and schematic of this circuit are depicted in Fig. 15.

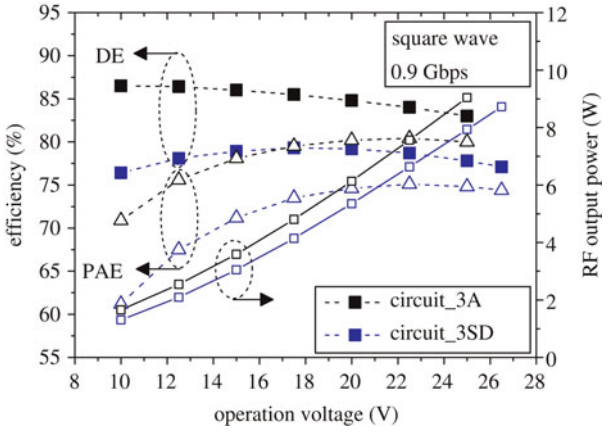

Fig. 12. Measured DE, PAE, and RF output power over operating voltage for a digital PA MMIC using a standard HFET (circuit_3A) and SD-HFET (circuit_3SD) output stage under digital square wave operation (0.9 Gbps).

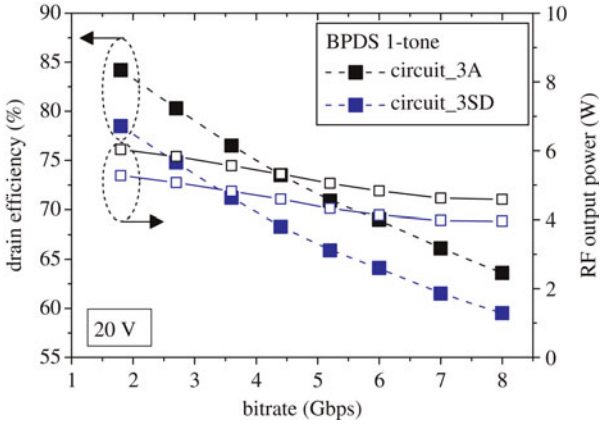

Fig. 13. Measured DE and RF output power over signal bitrate of a 1-tone BPDS-modulated signal for a digital PA MMIC using a standard HFET (circuit_3A) and SD-HFET (circuit_3SD) output stage (20 V operating voltage).

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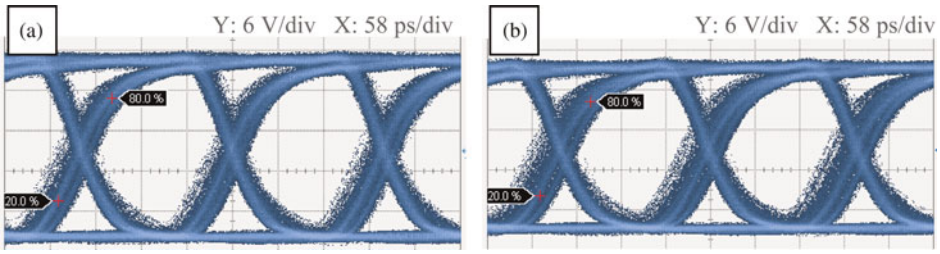

Fig. 14. Measured output waveform eye diagrams of a digital PA MMIC with a standard HFET output stage (a) and a SD-HFET output stage (b) operating at 5.2 Gbps BPDS-modulated input signal.

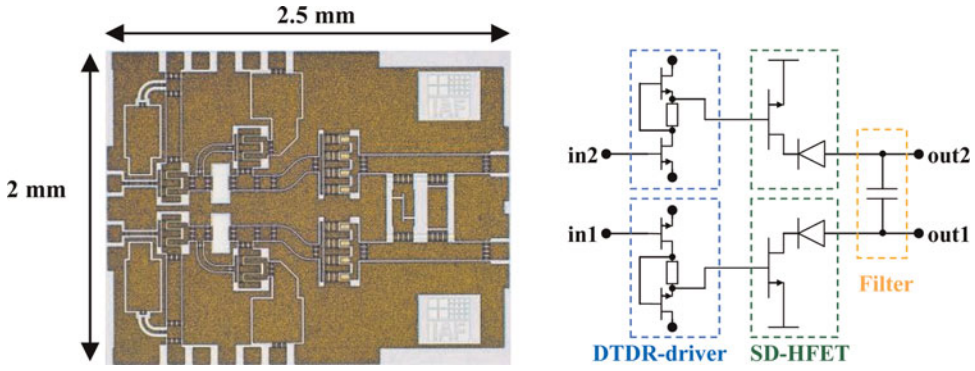

Fig. 15. Chip image (left) and schematic (right) of a differential class-S switch-mode amplifier core MMIC with integrated SD-HFET and passive integrated filter elements (chip size 2 × 2.5 mm^2).

Measurements in square wave operation on an equivalent single-ended circuit result in a maximum digital output power of 7.9 W and 74% PAE at a low bit rate of 0.9 Gbps. In BPDS mode, class-S equivalent, the single ended MMIC operates up to a maximum bit rate of 8 Gbps, where about 5 W output power and 57% DE was measured. Estimated from simulations, the differential MMIC in current-mode configuration is able to deliver twice the output power, about 10 W at 8 Gbps with a similar efficiency.

VII. CONCLUSION

This work describes the integration of Schottky diodes into fast GaN MMIC technology suitable for the realization of switch-mode amplifier core chips at 2 GHz. The GaN HFET with integrated diode shows a low effective on-resistance of 4.5 Ω·mm at high on-state current up to 950 mA/mm and withstands an off-state drain voltage between −100 to +100 V. With the demonstration of this technology, the so-called third-quadrant issue of switch-mode PA can be diminished on device level, which reduces the PAE and causes signal distortion in BPDS class-S-type operation. This is due to the fact that the integrated diode approach presented in this paper has lower parasitic losses, reduces the amplifier complexity, and potentially also enables on-chip filter integration, as compared to a hybrid implementation of a protection diode. Furthermore, switch-mode PA core MMICs realized with the developed integrated diode HFETs show a reduction of the PAE by 5%, but no measurable deterioration of the circuit switching speed as compared to circuits based on conventional HFETs. MMIC core chips are demonstrated which provide high DE under class-S equivalent digital operation at mobile communication frequencies. At 2.3 Gbps (0.9 GHz) DE of 75% and at 5.2 Gbps (2 GHz) DE of 66% at an output power level between 4 and 9 W was obtained including the diode. A speed improved differential MMIC able to operate up to 8 Gbps and with additionally integrated on-chip filter elements was developed for an application at 2 GHz.

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