International Journal of Microwave and Wireless Technologies, 2010, 2(1), 135–141. © Cambridge University Press and the European Microwave Association, 2010
doi:10.1017/S1759078710000152

# GaN-based amplifiers for wideband applications

PATRICK SCHUH[1], HARDY SLEDZIK[1], ROLF REBER[1], KRISTINA WIDMER[1], MARTIN OPPERMANN[1], MARKUS MUßER[2], MATTHIAS SEELMANN-EGGEBERT[2] AND RUDOLF KIEFER[2]

*Different wideband amplifiers, hybrid designs at lower frequencies, and monolithically integrated circuits (MMIC) at higher frequencies were designed, fabricated, and measured. These amplifiers are all based on AlGaN/GaN HEMT technology. The future applications for these types of amplifiers are mainly electronic warfare (EW) applications. Novel communication jammers and especially active electronically scanned array EW systems have a high demand for wideband high power amplifiers. The second application also needs high robust low noise amplifiers for its receive path. Output power levels of 38 W for hybrid amplifiers at lower frequencies up to 6 GHz and 15 W for the MMIC power amplifiers at higher frequencies are measured. With these building blocks, novel EW system approaches can be investigated.*

**Keywords:** AlGaN/GaN, MMICs, Wideband, HPA, LNA

Received 18 November 2009; Revised 1 February 2010; first published online 19 April 2010

## I. INTRODUCTION

In the wireless communication industry the GaN technology is already established. It will complete or even replace the state-of-the-art LDMOS technology widely used today. This is especially true when looking for high-efficiency amplifiers for the third generation and the upcoming fourth generation in the frequency range above 2 GHz. New amplifier concepts like envelope tracking or Doherty amplifiers [1] are already demonstrated using GaN technology.

The second field of application, where GaN technology has already shown its potential, is amplifiers for radar transmit/receive (T/R) modules. These T/R modules are key elements in active electronically scanned array (AESA) radars, which are increasingly being favored over conventional mechanically scanned systems. The achievable radar range of such an AESA radar is mainly determined by the output power and the noise figure of the antenna. Both properties can be improved using GaN technology [2–4]. With the GaN technology, high power amplifiers (HPAs) with higher output power compared to GaAs monolithically integrated circuits (MMICs) are already demonstrated [5–7]. Based on such MMICs the first T/R module demonstrators are realized [8, 9].

Besides the need for more output power, there is a trend for wide bandwidth power amplifiers in the secure communications, radar, and specially electronic warfare (EW) business. In this context wideband means relative bandwidth up to 100%. Possible applications for high power wideband amplifiers can be:

- Secure communication systems realized with spread spectrum techniques or realized as software defined radio have a demand for high power wideband amplifiers in the frequency range from some MHz up to 4 GHz.
- Future radar systems with multiband functionality, e.g. combining the C- and X-band [2].
- Small communication jammers in the frequency range from 2 to 6 GHz for dealing with remote controlled improvised explosive devices (IEDs).
- EW jammers based on an AESA approach for intelligent jamming for frequencies up to 18 GHz.

In the future there is even a combination of these functionalities possible. In such multi-function arrays, there are different functions integrated, like radar, all kinds of EW functionality and communication. The GaN technology is an enabling technology for these multi-functional array systems.

In his paper the design and the achieved performance of different wideband amplifiers, both hybrid assemblies and MMICs based on GaN technology, are presented.

The MMIC and hybrid amplifier designs, simulations, and measurements are done at EADS Defence Electronics, Ulm. The wafer and MMIC fabrication is done at the Fraunhofer Institute of Applied Solid-State Physics, Freiburg.

## II. HYBRID HIGH POWER AMPLIFIERS

With the upcome of remote-controlled IEDs, a new field of application for communication jammers grew up. Before that threat jamming in the communications frequencies usually was performed by large, dedicated EW platforms. They were designed to jam communications at higher distance. The new threat is more demanding to jam in the direct surrounding of the unit to be protected. For this

[1]EADS Deutschland GmbH, Defence Electronics, Wörthstrasse 85, 89077 Ulm, Germany.
[2]Fraunhofer Institute of Applied Solid-State Physics, Tullastrasse 72, 79108 Freiburg, Germany.
**Corresponding author:**
P. Schuh
Email: patrick.schuh@ieee.org


https://doi.org/10.1017/S1759078710000152 Published online by Cambridge University Press

application new wideband amplifiers with output power levels up to 50 W are necessary.

A one-stage HPA for pulsed and CW applications in a frequency range from 2 to 6 GHz was designed as building block for this type of application (Fig. 1). The active element is a GaN powerbar in 0.5 μm gate technology on 100 μm SiC substrate with eight transistors each 6 × 250 μm gate length. The powerbar is soldered with AuSn on a 60 mil gold-plated CuMoCu heat spreader.

The pre-matching networks and the drain bias stub are realized on high-k substrate with a dielectric constant $\varepsilon_r = 36$ (Zirconium Tin Titanate, TD-36). For low loss microstrip applications, the substrate material is used with a polished surface finish and a 26 μm gold layer. The different substrate heights of SiC and TD-36 are adapted by a milled powerbar pedestal of 200 μm thickness at the heat-spreader. Hence, short bonding distances between powerbar and matching networks are achieved.

The intention of this first step design was the evaluation of the high-k substrate and the heat-spreader material concerning electrical and thermal performance in broadband HPA applications. High-k material offers the possibility to realize compact low impedance matching networks, especially for broadband applications down to 2 GHz. An important aspect of combining the eight transistors to the matching networks is the application of slotted tapers bonded to the gate and drain contacts. In addition with the thin film resistors, integrated on the powerbar, excellent odd-mode suppression is obtained. In this first step design, an exponential tapered line for the output impedance matching with distributed reactive matching elements is used. The input line width is modulated to reduce the total circuit length. For even-mode stabilization, a NiCr thin film resistor in parallel to ceramic capacitors is used. The planar matching networks are EM simulated with ADS Momentum. Due to the high $\varepsilon_r$, simulation accuracy with standard microstrip ADS models seems not to be sufficient in general. Especially the EM simulations of microstrip junctions for wide lines and open stubs differ to the results obtained with standard models. However, the simulations of tapered, respectively, width modulated microstrip lines using the tapered microstrip model provide good results during the design optimization phase.

Furthermore, due to the high $\varepsilon_r$ and the low substrate thickness lines with an impedance of 50 Ω would be very narrow. For low loss, respectively, high power applications input and output matchings have been carried out to a reference impedance of 20 Ω. For testing the building block in a 50 Ω coaxial-jig, transformations from 20 to 50 Ω are realized by exponential tapered lines on standard soft substrate (Rogers RO4003C).

The gate bias network is connected to the input line on the soft substrate close to the 20 Ω port. The RLC circuit is implemented in SMD technology. Resistive elements in the gate bias network are important for even-mode stability at low frequencies and pulsed mode operation. The drain bias stub on TD-36 substrate is connected to ceramic and SMD capacitors. Total capacitance value is chosen as small as possible to achieve short rise and fall times in case of drain bias pulsing.

The simulated small signal performance versus measurement is shown in Fig. 2. The amplifier is measured in CW mode with 40 V drain bias voltage in class-AB operation. The building block was designed for 10 dB linear gain up to 6 GHz. For frequencies close to 2 GHz the measured linear gain increases to 16 dB. Close to 6 GHz the measured linear gain decreases stronger as expected. A part of the measured slope is linked to a weak input matching at frequencies around 6 GHz as it can be seen in Fig. 2. Limiting effects of the powerbar, not accounted in the nonlinear transistor model during the first design phase, are an additional reason for that slope. A reduced drain voltage of 30 V instead of 40 V results in max. 1 dB drop in linear gain. Due to the very low input impedance of the powerbar, the measured broadband input matching is 3 dB to 8 dB, only.

Pulsed power measurements (Fig. 3) at 40 V with 50 μs pulse length and 10% duty cycle results in a peak output power of 75 W at 2.25 GHz and 20 W at 5.75 GHz at 5 W input power. The associated efficiency is measured between 57% at 2.25 GHz and 23% at 5.75 GHz. However, due to self-heating of the powerbar the output power decreases in CW operation more than expected. Maybe, there is a significant thermal limitation due to the milled powerbar pedestal, which reduces the thickness of the first copper layer at the heat-spreader outside the powerbar area. Thermal simulations for different mounting topologies are under investigation. Measurements with reduced drain bias voltage of 35 V result in a good tradeoff between dissipated and output power. Up to 38 W output power is measured in CW mode.

In a redesigned building block the powerbar with 12 mm gate width is driven by a powerbar with 6 mm gate width. Input and interstage matching networks are resistive to achieve flat broadband gain response and good even-mode stability. Two amplifier branches are combined on one heat-spreader as drop-in submodule. The total size of the drop-in

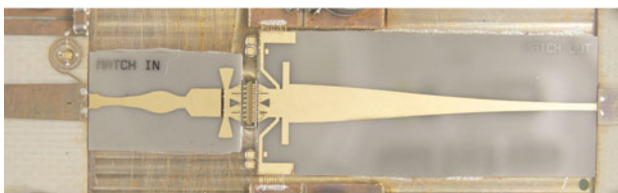


**Fig. 1.** Photo of the hybrid power amplifier building block.

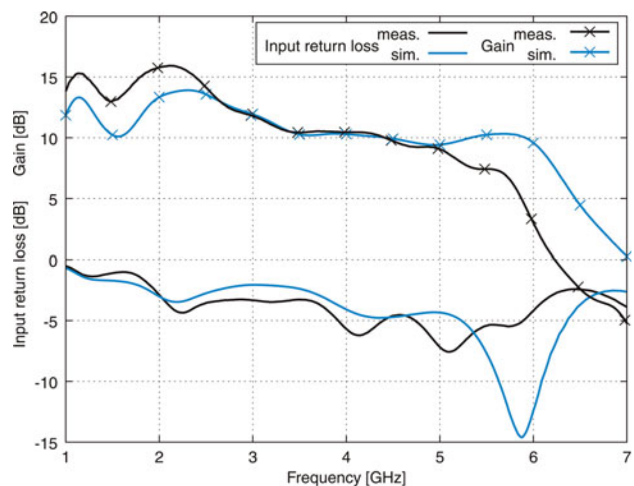


**Fig. 2.** Measured small signal gain and input return loss versus frequency of the GaN hybrid amplifier at $V_{DS} = 40$ V compared with the simulated performance.

https://doi.org/10.1017/S1759078710000152 Published online by Cambridge University Press

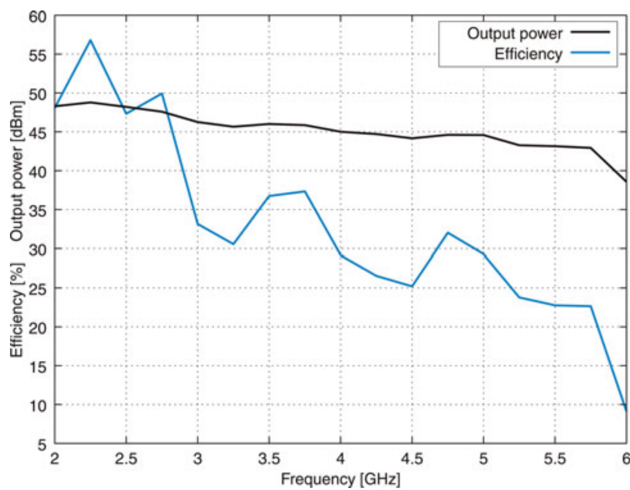


**Fig. 3.** Measured output power and efficiency versus frequency of the GaN hybrid amplifier at $V_{DS} = 40$ V in pulsed operation mode.

amplifier is 46 mm × 24 mm. In opposition to the first design, no powerbar pedestals are used to improve heat spreading. Hence, the longer bond distances, respectively the higher bond inductances, have to be compensated in the broadband design.

Furthermore, the accurate positioning of the powerbars during the solder process takes more efforts.

The input and output matching from 20 Ω, per amplifier branch of the submodule, to the 50 Ω SMA connectors is placed on soft substrate. The matching networks consist of a line transformer and the first stage of a broadband three-stage Wilkinson coupler. The next two stages, including the NiCr resistors for odd-mode suppression, are carried out on the high-k substrate. With this three-stage Wilkinson coupler, distributed on two different substrates, a matching and port isolation of better than 16 dB is realized over the whole frequency range from 2 to 6 GHz. The expected additional loss of this 3 dB coupler is less than 0.8 dB. The low loss and the compact topology benefit from the application of the two substrate materials.

The simulated input pre-matching of the amplifier branches is better than 5 dB to the 10 Ω reference impedance. The output pre-matching of the amplifier branches is realized to a 10 Ω reference impedance, too.

A even more compact solution compared to the first building block is possible. To improve the input and output matching a balanced configuration is used. For that, a quarter wavelength line at center frequency is added to one branch at the input and output Wilkinson coupler. This results in simulated 8 dB input matching at the edge frequencies and 20 dB at the center frequency. The expected linear gain at the SMA ports between 2 and 6 GHz is between 17 and 20 dB. To reduce the thermal stress in CW operation, the amplifier is optimized for a drain bias voltage of 28 V instead of 40 V. The simulated output power level is about 35 W versus the specified frequency range, with an associated power gain of 15 dB. Furthermore, due to the medium drain bias voltage of 28 V the optimum load resistance of the powerbar is close to 1:1.52 of the optimum load resistance at 40 V (5 V knee voltage accounted). Assuming a constant drain–source capacitance, this results in up to 52% more frequency bandwidth or an improved drain matching versus the frequency bandwidth.

## III. WIDEBAND POWER AMPLIFIER MMICS

Another field of applications besides the substitution of GaAs is the substitution of microwave power tubes. With GaN MMICs it is possible to realize AESA EW jammers, due to the output power level and also the broadband capability. With these new jammers an intelligent directed jamming is possible, reducing the total radiated power. The solid state solution has an extremely higher linearity compared to the realization with tubes.

In the frequency range from 6 to 18 GHz several power amplifiers were designed and measured, this includes both driver amplifiers and HPA. For the HPAs different amplifier topologies were realized. These MMICs are building blocks for future wideband HPA chains.

### A) Driver amplifier (DA)

The MMIC driver amplifier is designed as a two-stage amplifier with one transistor of 8 × 75 μm gate width in the first stage and two transistors in the second stage (see Fig. 4). The amplifier is designed for 50 Ω impedance at the input and output port. One design objective was to provide enough input power for two HPAs in parallel configuration in the frequency band from 6 to 18 GHz.

The maximum measured output power in CW mode is higher than 4 W while operating in saturation mode with up to 5 dB gain compression (Fig. 5). The operational frequency band of this MMIC is compressed toward lower frequencies. Detailed resimulations showed that the root cause for this frequency limitation was an inaccuracy in the passive MIM capacitor models used during the design.

The measured saturated output power is even a little bit higher than predicted by the simulation. The achieved output power is sufficient for driving one or two HPAs in the frequency range between 6 and 16 GHz.

### B) High power amplifier

In Fig. 6 a wideband HPA MMIC optimized for 6–18 GHz is shown. The HPA is a two-stage design with two transistors (6 × 100 μm gate width) in the first stage and four transistors

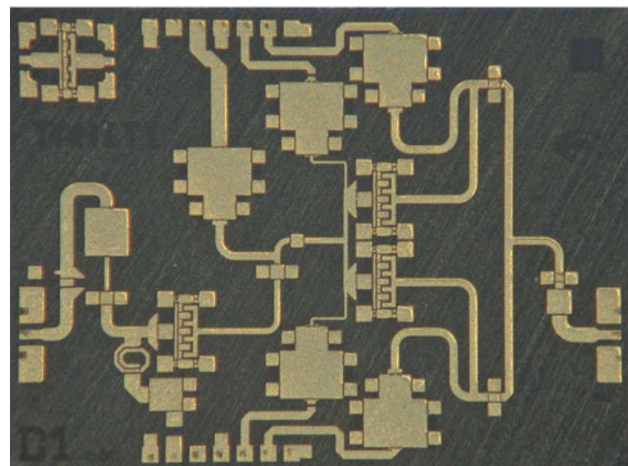


**Fig. 4.** Photo of a GaN DA MMIC chip. Chip size: 4 × 3 mm.

https://doi.org/10.1017/S1759078710000152 Published online by Cambridge University Press

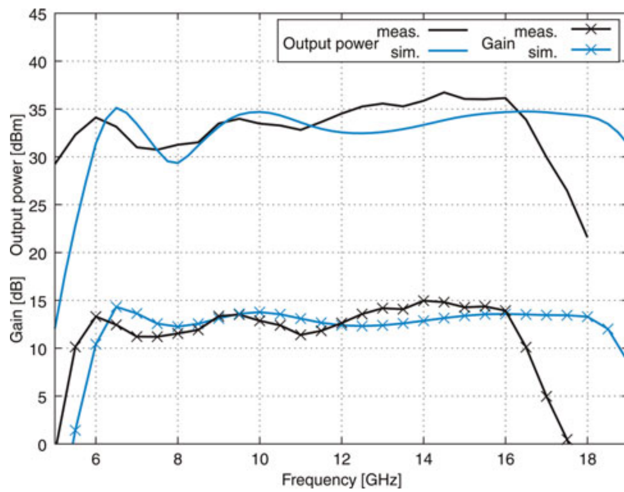


**Fig. 5.** Comparison of the simulated and measured saturated output power and small signal gain versus frequency of the GaN DA MMIC.

(8 × 100 μm gate width) in the second stage. The simulated linear gain response was 13–18 dB versus specified frequency range with more than 10 dB port matching (Fig. 7). On-wafer small signal measurements of the HPA have shown a strong limitation of bandwidth for frequencies higher than 15 GHz, this is also linked to the inaccuracy of the MIM capacitor model used for the design.

In CW operation mode, an output power level up to 7 W is measured for 30 V drain bias voltage. Figure 8 shows the output power versus frequency up to 17 GHz for pulsed operation. In this case, the peak output power level increases up to 13 W due to the improved thermal conditions. A small signal gain between 22 dBm at 6 GHz and 14 dB at 15 GHz is measured.

## C) Nonuniform distributed power amplifier (NDPA)

A different approach to satisfy the requirement, high output power over a wide frequency range, is the NDPA [10]. Figure 9 shows a 10 transistor NDPA MMIC designed for 6–18 GHz applications. The first transistor of the NDPA has a gate width of 6 × 125 μm and each of the following nine transistors have a gate width of 6 × 50 μm. The design goal was to find matching lines at gate and drain as short as possible to obtain small chip sizes. In an NDPA all transistors have to be loaded with their optimum impedance to achieve maximum output power of each transistor. To obtain

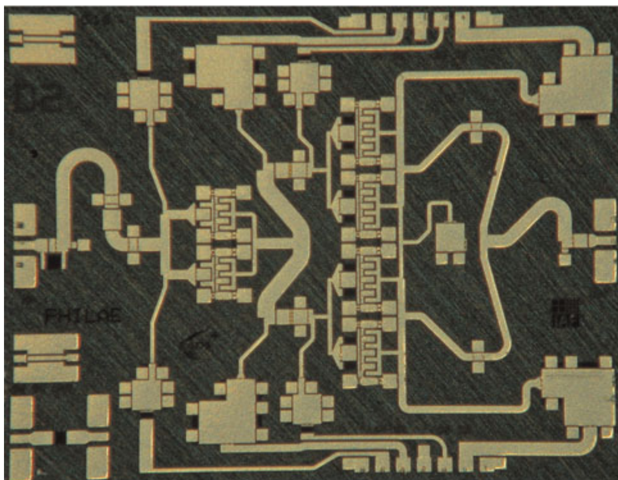

**Fig. 6.** Photo of a GaN HPA MMIC chip. Chip size 4.5 × 3.5 mm.

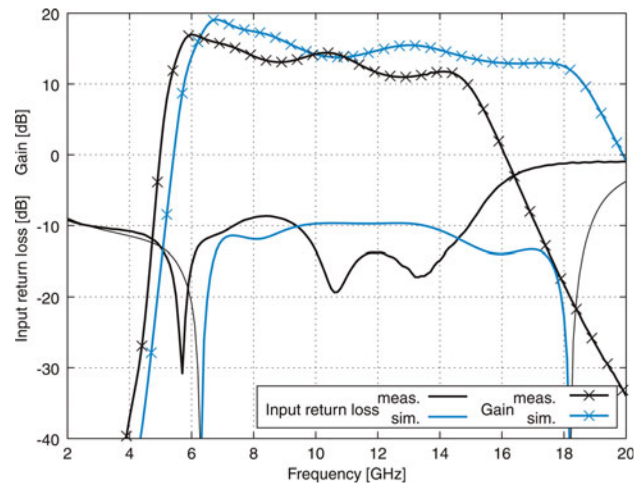


**Fig. 7.** Measured small signal gain and input return loss versus frequency of the GaN HPA MMIC at $V_{DS} = 30$ V compared with the simulated performance.

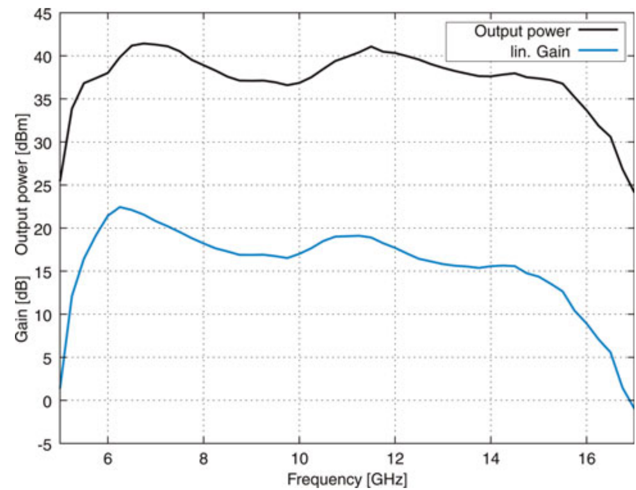


**Fig. 8.** Measured output power and linear gain versus frequency of the GaN HPA MMIC at $V_{DS} = 30$ V in pulsed operation mode.

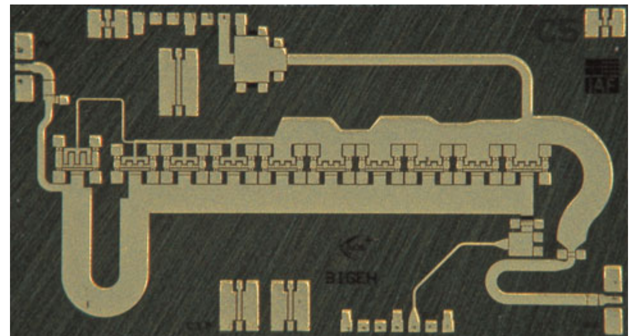

**Fig. 9.** Photo of a GaN NDPA MMIC chip. Chip size: 5.5 × 3 mm.

https://doi.org/10.1017/S1759078710000152 Published online by Cambridge University Press

reasonable matching results in microstrip technology, the first transistor will be chosen usually with a two to three times larger gate width as the following transistors. The limiting factor is the minimal line width in the first section of the drain matching line. The drain matching is optimized better than 6 dB for the first transistor and better than 9 dB otherwise. To realize a compact design as shown, each transistor must be weakly capacitive coupled to the gate matching line. Best results can be achieved with a low impedance gate line. Due to the weak coupling the achievable linear gain of the NDPA is small (Fig. 10). One solution of this problem is using cascode transistors instead of using normal transistors in common source configuration. The model of these cascode transistors was not available for this first design iteration, they will be used in the next iteration.

However, the measured and simulated linear gain shows a good flatness versus the specified frequency range (Fig. 10). The simulated matching is better than 10 dB at the input and better than 15 dB at the output. The measured results are close to 10 dB. Furthermore, the obtained frequency bandwidth is close to the expected performance. The measured output power level for CW operation is 8 W. Due to improved thermal conditions in pulsed operation, an output power level of 15 W is obtained.

## IV. ROBUST LOW NOISE AMPLIFIER MMICS

Good power-handling capabilities of GaN devices are not only advantageous for high power applications but also can serve for constructing highly robust LNAs. In the receive path of modern EW systems these robust LNAs are required. In particular when AESA EW systems will be realized, the receive path needs the same frequency bandwidth as the transmit path. For the lack of space a bank of filters cannot be used and a single wideband LNA must be used.

In overdrive condition the input transistor can fail due to excessive gate current. This gate current can occur either by turn-on of the gate diode during forward conduction or by impact ionization break down under very high gate reverse voltage [11]. One method to keep the gate current within save limit is the introduction of a gate series resistor. In this way, a feedback mechanism is introduced which decreases gate current by shifting the gate voltage to more negative values. However, this method solves the gate current problem during forward conduction but increases the reverse voltage. Since gate breakdown voltage in GaN devices is usually rather high this will normally impose no drawback. However both limitations have to be considered for optimum design.

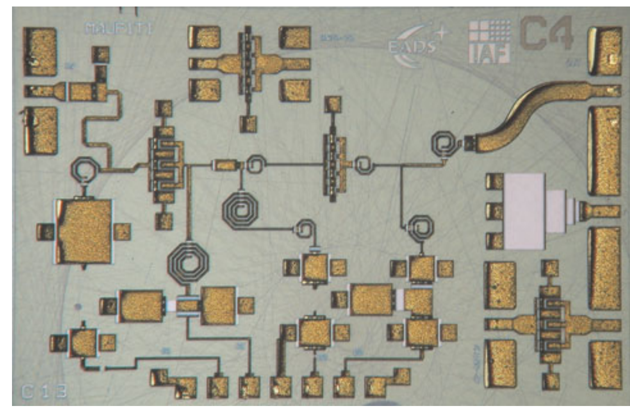


**Fig. 11.** Photo of a GaN LNA MMIC chip. Chip size: $3 \times 2$ mm.

A second method for increasing robustness is reducing the RF input power to the first stage. For this purpose a self-controlled limiter (patent pending) was designed. Under small signal condition this circuit acts as a small parallel capacitance which is incorporated in the input matching circuitry for the first stage. When imposed to high input power the parallel transistor of the limiter is forced into conduction. The input match becomes detuned and reduces the input power to the first LNA stage.

Several two-stage LNA designs have been realized with gate resistor. The resistor was chosen to ensure a safe limit in gate current dependant of the device gate width ($I_G = 10$ mA/mm) and simultaneously not exceeding the breakdown voltage of the gate diode ($BV = 80$ V). This applies to the first stage and in a relaxed manner also for the second stage. In Fig. 11 one of these LNA MMIC is shown.

In Fig. 12 the simulated and measured noise figure of the GaN LNA MMIC is shown. The obtained noise figure is very

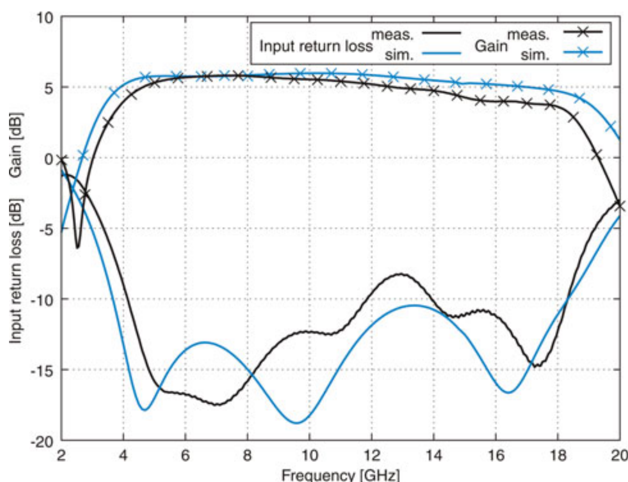


**Fig. 10.** Measured small signal gain and input return loss versus frequency of the GaN NDPA MMIC at $V_{DS} = 30$ V compared with the simulated performance.

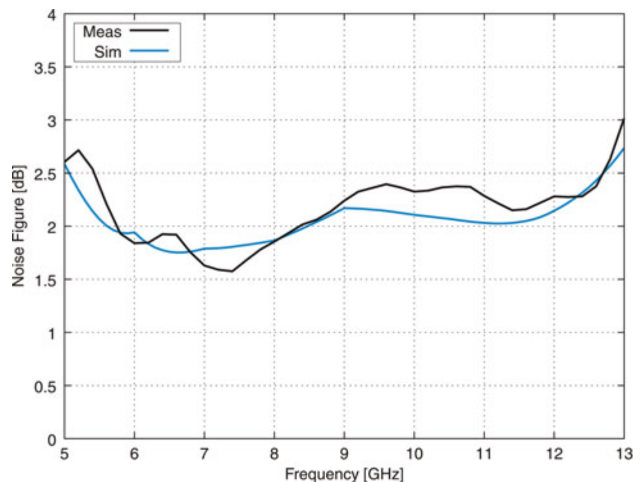


**Fig. 12.** Comparison of the simulated and measured noise figure versus frequency of the GaN LNA MMIC with $V_{DS} = 15$ V. $NF_{min} = 1.6$ dB.

https://doi.org/10.1017/S1759078710000152 Published online by Cambridge University Press

close to the expected one over the whole frequency band. The minimum noise figure is only about 1.6 dB. Over a frequency range of 7 GHz a noise figure below 2.5 dB is achieved.

The saturated output power of the LNA is about 27 dBm. First robustness tests have been performed up to 10 W input power level, leading not to any destruction at the LNA. At this input power level, the LNA is about 30 dB in compression.

## V. CONCLUSION

First hybrid building blocks for future HPA applications in the frequency range from 2 to 6 GHz are demonstrated. Output power levels in the range of 38 W are measured. A whole GaN MMIC wideband amplifier chip set for new AESA EW applications was designed, simulated, fabricated, and measured. Output power levels up to 15 W for the transmit path HPA and a noise figure of 1.6 dB for the receive path robust LNA are achieved. The limitation in the frequency bandwidth is analyzed and will be solved in the next designs.

## ACKNOWLEDGEMENTS

This work was partly funded by the German Bundeswehr Technical Center for Information Technology and Electronics (WTD81), Greding and the German Federal Ministry of Defence (BMVg), Bonn. This financial support is gratefully acknowledged.

The authors thank all involved colleagues from EADS, Ulm, and IAF, Freiburg for their strong support, especially the IAF clean room personal with Christian Libal and the measurement group.

## REFERENCES

[1] Pelk, M.; Neo, W.; Gajadharsing, J.; Pengelly, R.; de Vreede, L.: A high-effciency 100-W GaN three-way doherty amplifier for base-station applications. IEEE Trans. Microwave Theory Tech., **56** (7) (2008), 1582–1591.

[2] Kinghorn, A.M.: Where next for airborne AESA technology?, In IEEE Radar Conf. Proc., Rome, May 2008, 287–290.

[3] Ender, J.H.G. et al.: Progress in phased-array radar applications, In European Radar Conf. Proc., Amsterdam, October 2004, 113–116.

[4] Janssen, J.; van Heijningen, M.; Provenzano, G.; Visser, G.; Morvan, E.; van Vliet, F.: X-band robust AlGaN/GaN receiver MMICs with over 41 dBm power handling, In Compound Semiconductor Integrated Circuits Symp. Proc., October 2008, 1–4.

[5] Fanning, D.M. et al.: 25W X-Band GaN on SI MMIC, In Compound Semiconductor Manufacturing Technology Conf. Digest, 2005.

[6] Schuh, P. et al.: 20W GaN HPAs for next generation X-band T/R-modules, In IEEE Microwave Theory and Techniques Symp. Digest, San Francisco, June 2006, 726–729.

[7] Piotrowicz, S. et al.: State of the art 58 W, 38% PAE X-Band AlGaN/GaN HEMTs microstrip MMIC amplifiers, in Compound Semiconductor Integrated Circuits Symp. Proc., October 2008, 1–4.

[8] Schuh, P. et al.: X-band T/R-module front-end based on GaN MMICS. Int. J. Microwave Wirel. Technol., **1** (4) (2009), 87–394.

[9] Bettidi, A. et al.: X-band T/R module in state-of-the-art GaN technology, In European Radar Conf. Proc., Rome, October 2009, 258–261.

[10] Duperrier, C.; Campovecchio, M.; Roussel, L.; Lajugie, M.; Quere, R.: New design method of uniform and nonuniform distributed power amplifiers. IEEE Trans. Microwave Theory Tech., **49** (12), (2001), 2494–2500.

[11] Rudolph, M. et al.: Analysis of the survivability of GaN low-noise amplifiers. IEEE Trans. Microwave Theory Tech., **55** (1), (2007), 37–43.

**Patrick Schuh** received the Dipl-Ing. degree and the Dr.-Ing. degree in electrical engineering from the University of Ulm, Ulm, Germany, in 1998 and 2003, respectively, and the Masters degree in business administration from the University of Applied Sciences Neu-Ulm, Neu-Ulm, Germany, in 2004. From 1998 to 2002 he was a Research Assistant with the Microwave Techniques Department, University of Ulm, where he was involved with the analysis and the design of packages for microwave applications, utilizing electromagnetic simulations. Since 2002 he has been with, European Aeronautic Defence and Space (EADS) Company Deutschland GmbH, Defence Electronics, Ulm, Germany. Since 2009 he is heading the GaN and SiGe group inside the “MMICs and T/R-modules” department. His current area of interest is MMIC and T/R module design, especially high power amplifiers in GaN and GaAs technology.

Dr. Schuh is a member of IEEE, MTT.

**Hardy Sledzik** was born in Oberhausen, Germany, in 1959. He received the Dipl.-Ing. degree and the Dr.-Ing. degree in electrical engineering from the University of Duisburg, Duisburg, Germany, in 1986 and 1990, respectively. From 1986 to 1990, he was a Research Assistant at the Institute of Electromagnetic Theory and Engineering, University of Duisburg. Since 1990, he has been with EADS Deutschland GmbH, Defence Electronics, Ulm, Germany. His current area of interest is high power amplifier design, in GaN and GaAs technology.

**Rolf Reber** received his Diplomingenieur’s degree from the University of Karlsruhe, Germany. He joined the Radar Group of AEG-Telefunken Ulm/Germany (which is now part of EADS) in 1987, where he has been engaged in the design and development of microwave components for active phased array antennas.

His current work include the development and design of MMICs in GaAs- and GaN-technology dedicated for T/R-modules and the research in the field of modern amplifier topologies for wireless communication.

https://doi.org/10.1017/S1759078710000152 Published online by Cambridge University Press

**Kristina Widmer** received her diploma (Dipl.-Ing.) in electrical engineering from the University Stuttgart, Germany, in 2003. In the same year she joined EADS Deutschland GmbH, Defence Electronics, department "T/R modules and MMICs" in Ulm. There she has been working on the development of hybrid circuits, MMICs, and transmit/receive modules. She was involved in the space projects TerraSAR-X and TanDEM-X. Her current research interest is in GaN MMIC design with focus on amplifiers and T/R module design.

**Martin Oppermann** was born 1960 in Cologne (Germany). He holds a diploma degree and a doctor's degree in physics from the University of Tübingen. In the department of Applied Physics and in the NMI (Natural and Medical Science Institute), his research activities were in semiconductor electronics and thin film technologies for application in optics and electronics.

After 2 years semiconductor processing and engineering with the BOSCH company in Reutlingen he started 1993 inside EADS in the department of RF module development and ceramic substrates. As an expert of module technologies, he focused on mm- and microwave qualified substrate and assembly technologies. In 2007 he became the head of department "T/R modules and MMICs".

Dr. M. Oppermann is a member of the DPG (German Physical Society) and an international member of IMAPS (Intern. Microelectronics and Packaging Society).

**Markus Mußer** was born in Villingen, Germany on April 24, 1974.

He received the diploma in electrical engineering in 2007 from the University of Applied Sciences Nuremberg, Germany.

In 2007 he joined the RF Devices and Circuits Department of the Fraunhofer Institut of Applied Solid-State Physics in Freiburg, Germany, where he is currently working on GaN RF power bars and RF-high-power amplifiers.

**Matthias Seelmann-Eggebert** received his Diploma and Ph.D. degree in physics from the University of Tübingen in 1980 and 1986, respectively. From 1980 to 1996 he was involved in R&D related to infrared detectors based on HgCdTe and developed electrochemical and surface physical methods for the characterization of compound semiconductor surfaces. From 1990 to 1991 he was a visiting scientist at Stanford University. From 1997 to 2000 he was engaged in the growth of CVD diamond. Since 2001 he is a member of the department of high frequency electronics of the IAF in Freiburg, Germany, and is concerned with the preparation and development of simulation models for active and passive III–V devices.

**Rudolf Kiefer** received his Dip. Phys. degree in physics from the University of Freiburg in 1979. He joined the Fraunhofer Institute of Applied Solid State Physics (IAF) in 1980 starting work on liquid crystal displays. For work on this topic he received the Ph.D. degree in physics in 1984 from the University of Freiburg. From 1984 to 1991 he investigated electro-optic effects in ferroelectric, liquid crystalline polymeric materials for optical storage applications. Afterwards he focused his work on studying a new switching effect of nematic liquid crystals to improve the viewing angle characteristics of thin film addressed liquid crystal displays (TFT-LCD). For this work he received a SID-Award in 1998. In 1994 he moved to the field of III–V optoelectronic semiconductor technology. He managed different technology projects developing processes for fabrication and laser facet deposition of InP-based high speed laser and GaAs as well as GaSb-based high power laser. Since 2000 his work is focused on the development of GaN semiconductor technology for MMICs.

https://doi.org/10.1017/S1759078710000152 Published online by Cambridge University Press