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On-chip spiral inductor in flip-chip technology

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Performance comparison is made between on-chip spiral inductor in flip-chip versus wirebond package technology. Full-wave electromagnetic simulation and on-strip measurement techniques were used to study the performance fluctuations of inductor within flip-chip environment. Results show that the performance of a flipped silicon-based spiral inductor is affected by the radio frequency (RF) current return path differences. The RF current return path for flip-chip is concentrated on the surface of silicon layer exclusively because back side ground under silicon is floating in flip-chip technology. In addition, the bump proximity effect is also considered. On-chip inductors in flip-chip environment must be optimized by reducing the eddy current in the silicon substrate and parasitic affects by adjusting design parameters. The equivalent circuit model of the flipped on-chip spiral inductor is verified with measured results over broadband frequencies. Also, the RF flip-chip characterization technique using on-strip measurement method is presented.

Keywords: On-chip spiral inductor, Flip-chip, On-strip measurement, Coplanar Waveguide, Electromagnetic coupling

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I. INTRODUCTION

Wireless communication systems are projected to be one of the fastest growing electronics industries in the next several years. Recent advances in integration technology and device performance demands higher packaging density from high-frequency integrated circuits (ICs). Flip-chip technology is emerging as a leading technology to meet the high-frequency and the high-density requirements [1]. Recent works have shown that it is suitable to integrate all circuits on GaAs microwave monolithic integrated circuit technologies in the millimeter wave frequency range. However, the low cost of silicon-based IC compared to GaAs makes silicon the process of choice in many radio frequency (RF) integrated circuit (RFIC) applications [2]. Silicon-based RFIC requires integrated on-chip inductors as one of the key elements for voltage-controlled oscillator (VCO), low noise amplifiers, and single-chip transceivers. Silicon-based IC technologies have not been widely used with flip-chip technology for RF applications. Passive and active circuitries on flipped silicon chip face different coupling and parasitic mechanisms compared to the traditional wirebond package technology. Two major differences arise in the flip-chip technology compared to wirebond technique. First, the back plane of the flipped chip is no longer sitting on a solid ground plane but instead it is a floating ground. Second, the top of the die faces ground plane whereas wirebond faces away from ground plane. Several papers have addressed inductor performance on silicon substrate based on wirebond packaging technology since the introduction of inductor on silicon [3, 4]. Meanwhile, passive devices on flip-chip packaging technology are not studied extensively. On-chip inductors generally enhance the reliability and the efficiency of silicon-integrated RF cells and contribute to a higher level of integration. The limitation of inductors on flipped silicon chip should be clearly characterized and understood by the circuit designers in order to make appropriate design optimizations. Conventional on-wafer measurement techniques to characterize RF flip-chip face some difficulties because conventional on-wafer technique cannot characterize changed electric and magnetic field effects due to flip-chip configuration. The development of a characterization technique for flip-chip packages is motivated by the need to predict the behavior of devices in flipped environment at RF frequencies. In order to minimize the effect of the parasitics on flipped spiral inductor, the electromagnetic couplings as well as the neighboring bump effects from both chip and package substrate should be further analyzed and investigated.

In this paper, the effect of the flip-chip technology on the performance of on-chip silicon inductor is presented. Results from measurements and simulations are shown. It shows that the inductance of flipped on-chip spiral inductor on silicon substrate is affected by flip-chip environment. An on-strip technique was used to measure the RF performance of the flipped chip inductors. The on-strip measurement setup was further analyzed by using three-dimensional (3-D) full-wave electromagnetic simulation and experimentally validated up to 20 GHz by using vector network analyzer and on-wafer probe station. Assessment and characterization of a flipped on-chip spiral inductor is also presented as a validation of this technique. The organization of the paper is as follows: The difference between wirebond and flip-chip technology is reviewed in Section II. In this section, different electrical and magnetic behaviors on RF of flipped on-chip spiral inductor are shown. Section III explains the on-strip flip-chip measurement setup. Section IV discusses the effects of flip-chip technology on circuit performance and provides

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an equivalent circuit model for flipped on-chip spiral inductor. The *S*-parameters of the measured flipped spiral inductor is compared to those of the equivalent circuit model. The proximity effects between bump and inductor in flip-chip environment are studied in Section V.

II. ON-CHIP SPIRAL INDUCTOR IN FLIP-CHIP AND WIREBOND TECHNOLOGY

RFIC around 2 GHz has been successfully implemented using wirebond technology. However, flip-chip package provides a long-term potential alternative for significantly reducing package cost and system size using direct chip attach to PCB system boards. Flip-chip also stands to benefit from improved performance for RF, digital, and mixed signal applications in highly integrated chips [5]. Low impedance signal paths can be achieved from the inherent inductance drop of the two technologies (nHs' to pHs' in wirebond versus flip-chip). Flip-chip technology can furthermore draw size benefit from bumps instead of wirebonds for interconnections. Two major differences exist between flip-chip and wirebond technology. The back plane of the flipped chip is no longer a solid ground plane meanwhile the top of the chip faces ground plane instead. Figures 1(a) and 1(b) show the cross-section of an inductor using wirebond and flip-chip package technology, respectively [6, 7].

Conventional wirebond package technology usually relies on die attachment to the top of ground plane of the silicon substrate. In general, the location of the ground plane impacts the RF current return path since electric energy is coupled to the substrate through displacement of current. Displacement and conduction of currents into the substrate lead to the electromagnetic field losses in silicon substrate. Since loss and quality factor (Q) are related, it is desirable to quantify it. The Q of an inductor is defined as

$$Q = 2\pi \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss}}. \quad (1)$$

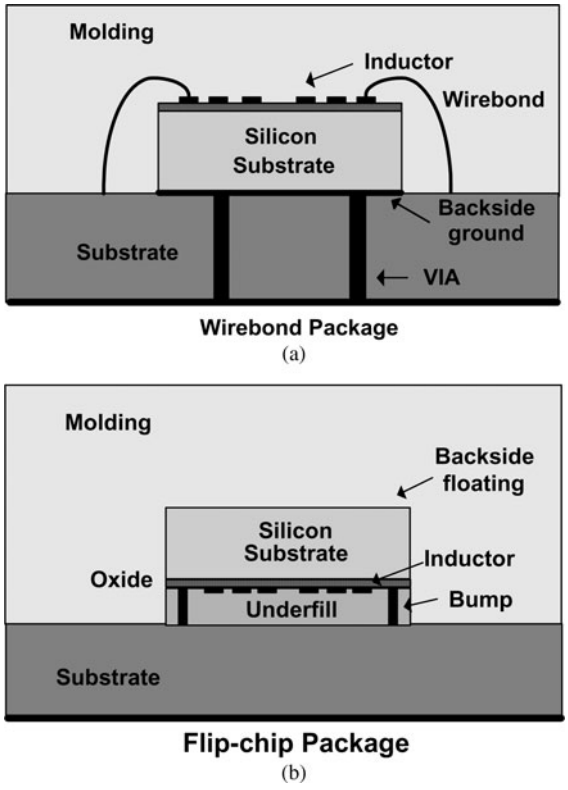

Fig. 1. Cross-sectional view of spiral inductor in (a) wirebond and (b) flip-chip technology.

Spiral inductors on silicon substrate suffer from several power dissipation mechanisms, which yield lower inductor Q. The resistance of metal trace causes a high series resistance, which limits the performance of the inductors at low frequencies, while the capacitive coupling to the lossy silicon substrate is responsible for the degradation of the Q at higher frequencies [8]. For frequencies below 1 GHz, the skin effect is relatively small since the thickness of metal trace is typically comparable to the skin depth [9]. Above 2 GHz, however, the sheet resistance worsens as skin effect increases and electric energy is coupled to the substrate through displacement current. The substrate losses arise from the displacement current flowing through the oxide and conduction current to nearby grounds, either at the surface of the substrate or at the back plane of the substrate. Induced current flowing in the substrate furthermore causes substrate current due to the time-varying fields of the inductor. The time-varying fields are determined by the scalar and vector potentials [10].

$$E = -j\omega A - \nabla\phi, \quad (2)$$

$$B = \nabla \times A. \quad (3)$$

Using Maxwell's equations, the following equation is obtained:

$$\nabla^2 A = \mu\big(j\omega\sigma A - \omega^2\varepsilon A(\sigma + j\omega\varepsilon)\nabla\phi\big). \quad (4)$$

The first term identifies the magnetically induced eddy currents in the substrate of the metal conductors. The second term represents the dynamic radiation current. The third term includes the electrically inducted conductive and displacement currents in the substrate. The quality factor is proportional to the net magnetic energy stored, which equals to the difference between the peak magnetic and electric energy for an inductor. Magnetic coupling is largely responsible for the degradation of the Q of on-chip inductor. Since the magnetic field induced by the eddy current in conductive material is orthogonal to the magnetic field, and the top of the chip faces the package substrate and ground in flip-chip as shown in Fig. 1(b), the Poynting's theorem can be used to calculate the total power crossing the surface enclosing the inductor trace. It can also be used to quantify the eddy current losses with magnetic vector potential. The complex Poynting's vector is given by

$$S = \frac{1}{2}(E \times H^*). \quad (5)$$

Poynting's vector is integrated over the surface y, the power crossing the substrate is obtained from

$$P + jQ = \frac{1}{2}\int_{-\infty}^{\infty} (E \times H^*)\hat{y}\, dx. \quad (6)$$

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For the time-varying case, the real component of total power is due to the lossy substrate since no other loss mechanisms exist for spiral inductor in wirebond technology [11]. However, flipped on-chip spiral inductor creates eddy current in the package substrate and ground plane. The eddy current in the package substrate is a negative increasing function that represents decreasing inductance as a function of frequency. The inductance decreases as the eddy currents flow in the package substrate. The eddy currents in substrate flow in a direction opposite to the current on inductor trace and generate a magnetic field. This magnetic field tends to cancel the penetrating magnetic field of the inductor and decrease the effective inductance. This can be explained by Lenz's law. However, the eddy currents flowing in the package substrate can be ignored due to low conductivity of package substrate material. Figure 2(a) shows the measured inductance of wirebond and flip-chip inductor on lossy silicon substrate. The measured on-chip spiral inductor has the following geometrical characteristics: outer dimension of 160 μm by 160 μm, metal trace width of 10.7 μm, and metal spacing between traces of 2.1 μm. The metal traces are insulated from the silicon layers by a SiO_2 layer having a thickness of 4.39 μm and a dielectric constant of 4.2. The lossy silicon substrate under the SiO_2 is 271 μm thick. The measured flipped on-chip spiral inductor uses the same geometrical characteristics of the wirebond inductor with the exception of the presence of the backside metal. The measured flip-chip inductance includes bump height of 80 μm, underfill between package substrate and flipped inductor. Figure 2 shows measured inductance and *Q*-factor of wirebond and flip-chip on-chip spiral inductor. Figure 2(a) displays the effective inductance of the wirebond on-chip spiral inductor, which is similar to that of the flipped on-chip spiral inductor up to 4 GHz. However, the effective inductance of the flipped on-chip spiral inductor shows peaking behavior around 6 GHz due to low self-resonance frequency (10.5 GHz). This difference can be explained by associated package structure. The flipped inductor has eddy current in package substrate and parasitic capacitance due to flipped inductor facing package substrate and ground. As already mentioned, eddy current in package substrate can be ignored due to low conductivity of package substrate, while parasitic capacitance due to different ground plane of flipped inductor is significant. The resonance frequency for the flipped spiral inductor is lower than the wirebond spiral inductor due to the larger parasitics capacitance from 80 μm flip-chip height and dielectric constant of 3.8 underfill in the flip-chip structure. The *Q* of on-chip spiral inductors in different package is also affected by the associated package structure. The location of the ground plane impacts the RF current return path in flip-chip structure. The inductor RF current return path for flipped silicon substrate is associated with locations of ground substrate contacts that exist on the top surface of the chip. The changed RF current return path for flipped silicon substrate results in significant variations in current density and current distribution in the substrate. The changed current density and distribution cause variations in flipped inductor resistance and inductance at high frequencies. The measured *Q* of wirebond and flip-chip inductors are shown in Fig. 2(b). The *Q* of the flipped on-chip spiral inductor is lower than the wirebond on-chip spiral inductor due to lower effective inductance at low frequencies and higher parasitic capacitance at high frequencies as well as loss due to eddy current.

III. ON-STRIP MEASUREMENT TECHNIQUE

RF flip-chip characterization setup using on-strip measurement method is shown in Fig. 3. The chip was mounted onto a package substrate to measure the electric and magnetic characteristics of the flipped on-chip spiral inductor. The transition structures from on-wafer measurement probe pads to on-chip spiral inductor on chip were fabricated on a low-cost package substrate to measure the high-frequency response of RF flip-chip. In this setup, on-wafer measurement was used to obtain scattering parameters of package-mounted flipped on-chip spiral inductor.

A) Structure of on-strip measurement

Transitions between the ground-signal-ground (GSG) probe pads and the substrate vias are accomplished by using tapered coplanar waveguide (CPW) traces on the bottom of package substrate [12]. The entire structure is designed to maintain 50 Ω characteristic impedance using tapered CPW transmission

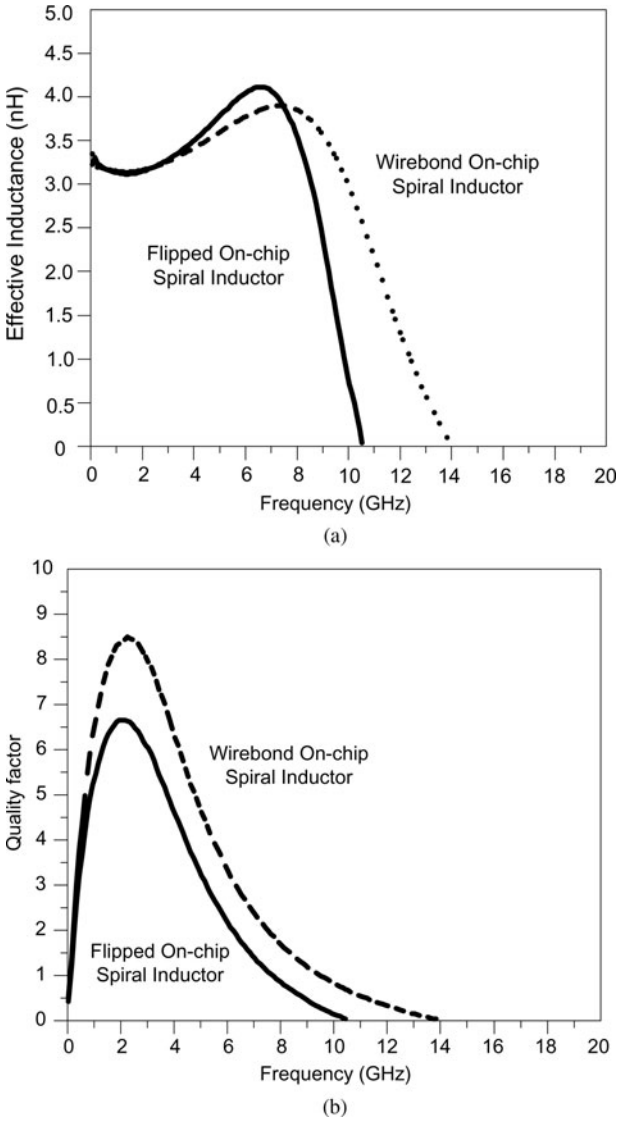

Fig. 2. Measured (a) inductance and (b) quality factor of wirebond and flip-chip inductor.

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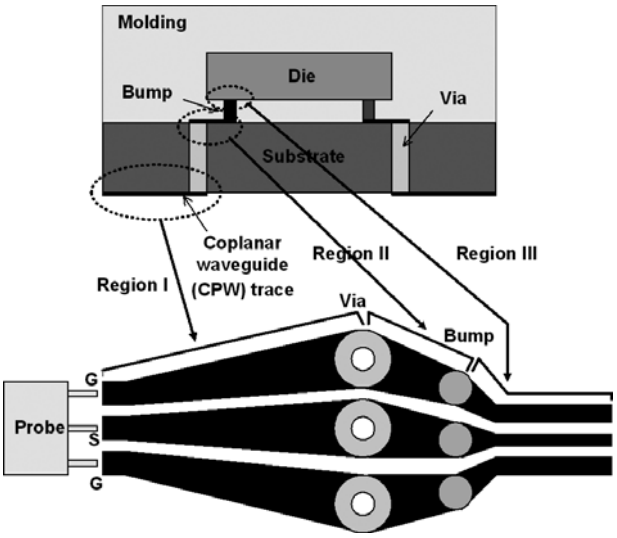

Fig. 3. On-strip measurement structure.

lines. Region I in Fig. 3 shows tapered transition structure between GSG probe pads and package vias. The designed GSG probe pads have the signal pad width of 120 μm and the space between signal and ground pads of 60 μm. GSG on-wafer pads structure satisfies the probe pitch of 150 μm. The metal space limitation comes from package process limitation at the time of design. The diameter of package vias is 300 μm. The minimum distance between vias is 75 μm. The CPW trace on the bottom of package substrate provides a transition between the pitch of the GSG probes used for on-wafer measurement (150 μm) and package vias. CPW traces between substrate vias and flip-chip bump are located on the package upper substrate and shown in Region II of Fig. 3. The test structure on chip is shown in Region III of Fig. 3. The total length of on-strip measurement structure is 6 mm. This transition structure was designed with tapered CPW transition to reduce discontinuity effects. The tapered CPW trace was optimized to reduce interconnection loss using electromagnetic simulator. A simplified flip-chip test structure shown in Fig. 4(a) was analyzed using a 3D electromagnetic simulator. Advanced design system was used to design and optimize the CPW probe pad. Via pads under and on package substrate were designed according to the manufacturing design rule. The bump pads on substrate and chip were designed to keep bump pitch of 225 μm. Figure 4(b) shows simulated insertion and return loss of chip-to-package transition structure up to 20 GHz.

B) Measurement results

Figure 5(a) shows a picture of fabricated bottom structure of package substrate. This structure includes input and output ports and tapered CPW structure between GSG probe pads and substrate vias. Measurements were carried out with Cascade on-wafer probe station with GSG pattern probes using a HP8510C vector network analyzer. Short-Open-Load-Thru (SOLT) [13] calibration was performed from 0.1 to 20 GHz, using calibration standard structures. Since the parasitics of on-chip open can be represented by *Y*-parameter equivalent lumped elements, which are in parallel to the passive and active circuits, the *S*-parameters of on-chip spiral inductor can be de-embedded from the measured *S*-parameters using a combination of cascaded and *Y*-parameter techniques. The same

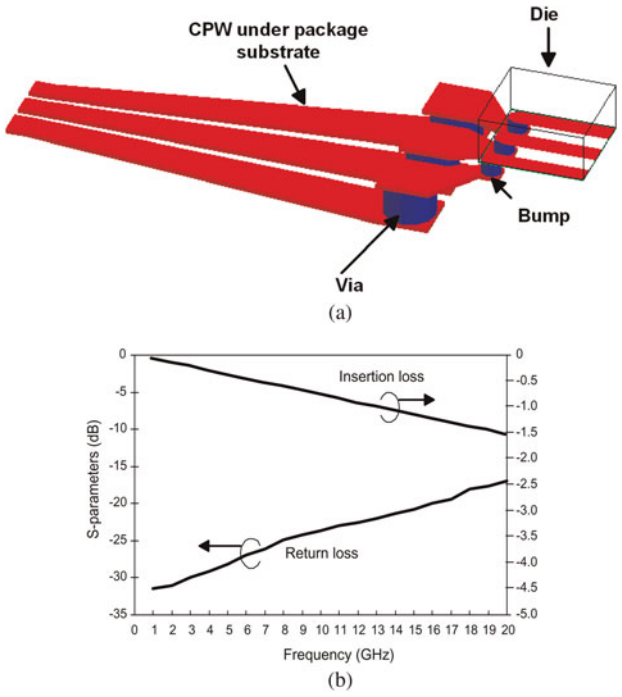

Fig. 4. (a) Simplified geometry and (b) simulated *S*-parameters of chip-to-package transition.

inductors were simulated by a full-wave electromagnetic simulator to compare measurement and simulation results. Figures 5(a) and 5(b) show pictures of on-strip measurement structure and on-chip spiral inductor, respectively. The white circles are vias in package substrate. The black circles are bumps between package substrate and die. The transition from vias to bump is located on upper substrate. This transition also uses tapered CPW structure to reduce discontinuity effects. The characteristics of the materials are as follows: the package substrate height of 200 μm, the package substrate dielectric constant of 4.2, substrate loss having tan $\delta = 0.023$ at $f =$ 2 GHz, bump height of 80 μm, under fill dielectric constant of 3.8 and molding layer height of 900 μm and dielectric constant of 4.3. The spiral inductor on flipped chip is as follows: outer dimension of 160 μm by 160 μm, metal width of 10.7 μm, and metal spacing of 2.1 μm. The metal traces are insulated from the silicon layers by a silicon oxide layer of 4.39 μm thickness and a dielectric constant of 4.2. The lossy silicon substrate has 271 μm thickness and 8 Ω-cm resistivity. X-ray machine was used to see other structures in the molding material, such as substrate vias and transition structure on package and flip-chip bump.

The measured *S*-parameters with on-strip measurement structure and de-embedded *S*-parameters are shown in Fig. 6. The flip-chip package parasitics, which include bumps, vias, and tapered CPW, are required in de-embedding process in order to characterize the on-chip device. De-embedding technique was used to extract package parasitics from measured *S*-parameters of the flip-chip structure.

The flip-chip package model can be simplified in circuit simulations to predict the electrical performance of the device in a RF flip-chip structure. The transmission line segments, including a tapered CPW trace on each side of the package substrate, are modeled using transmission line models in circuit simulator as shown in Fig. 7. Lumped LC circuits are used to model the bump interconnections and

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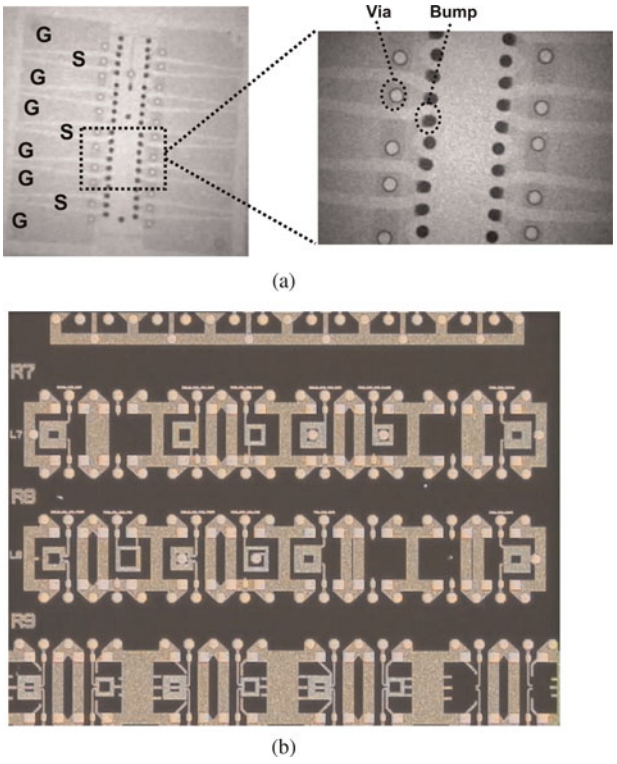

Fig. 5. Fabricated (a) chip-to-package transition and (b) on-chip spiral inductor.

via interconnections inside the package substrate [14]. An L-network is used to model via transition. In addition, π-network is used to model bump interconnections for flip-chip interconnections. In the LC circuits, the capacitance represents the effect of the overlapping metallization area between chip and package, while the inductance represents the self and mutual inductance of the bumps and vias. The equivalent circuit of on-strip measurement structure shown in Fig. 7 can be divided into four parts: (1) input port that includes chip/package transition structure; (2) output port that includes chip/package transition structure, (3) test fixture on chip that includes parasitic capacitances and inductances, and (4) passive or active device on chip.

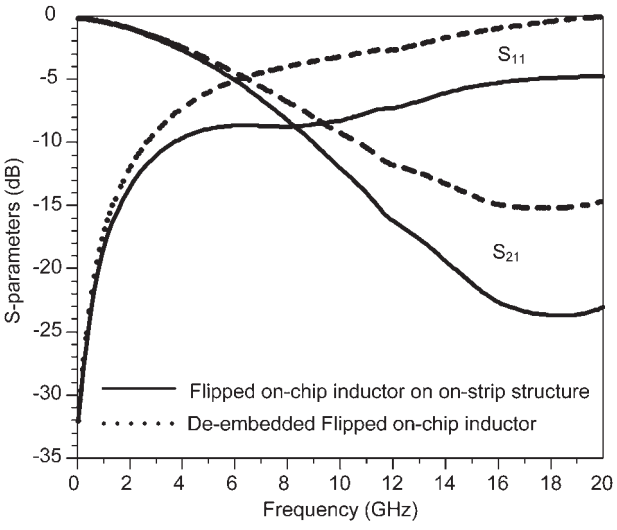

Fig. 6. Measured *S*-parameters of on-chip spiral inductor with on-strip measurement structure.

The input and output transitions are defined by the *S*-parameters, S_I and S_O, respectively. The *S*-parameters (S_{Device}) of the flipped device are obtained by applying the following *S*-parameter measurement methodology which is shown in Fig. 8.

(1) S_{Total} is obtained by measuring the two-port *S*-parameters with flipped die and input/output structure.
(2) S_I is obtained by measuring the two-port fixture *S* parameters with input structure only.
(3) S_O is obtained by measuring the two-port fixture *S* parameters with output structure only.

Determine the flipped device matrix S_{Device} from S_{Total} by applying the inverse chain scattering parameters or *T* parameter matrix multiplication techniques:

$$T_{Device} = T_I^{-1} T_{Total} T_O^{-1}, \tag{7}$$

where conversions between *S* and *T* parameters [15] are shown:

$$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{S_{21}} & -\frac{S_{22}}{S_{21}} \\ \frac{S_{11}}{S_{21}} & S_{12} - \frac{S_{11}S_{22}}{S_{21}} \end{bmatrix}$$

and (8)

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \frac{T_{21}}{T_{11}} & T_{22} - \frac{T_{21}T_{12}}{T_{11}} \\ \frac{1}{T_{11}} & -\frac{T_{12}}{T_{11}} \end{bmatrix}.$$

The complex propagation constant and characteristic impedance are computed from the de-embedded *S*-parameters by using the following equations:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \rightarrow \begin{bmatrix} A & B \\ C & D \end{bmatrix}, \tag{9}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh \gamma l & Z_0 \sinh \gamma l \\ Z_0^{-1} \sinh \gamma l & \cosh \gamma l \end{bmatrix}. \tag{10}$$

A three-step de-embedding method is followed to extract these package parasitics using simulated or measured *S*-parameters of the flip-chip device [16].

IV. EQUIVALENT CIRCUIT MODEL FOR FLIPPED ON-CHIP INDUCTOR

A small-signal equivalent circuit was extracted to understand the flip-chip effects of inductor parameters as shown in Fig. 9. In this circuit, R_s includes a frequency-dependent term that is related to skin effect of metal and other high-frequency effects. C_f models the parasitic capacitance that consists of the overlap capacitance between the spiral and the underpass, fringing capacitance between adjacent metal lines. C_1 and C_2 represent the

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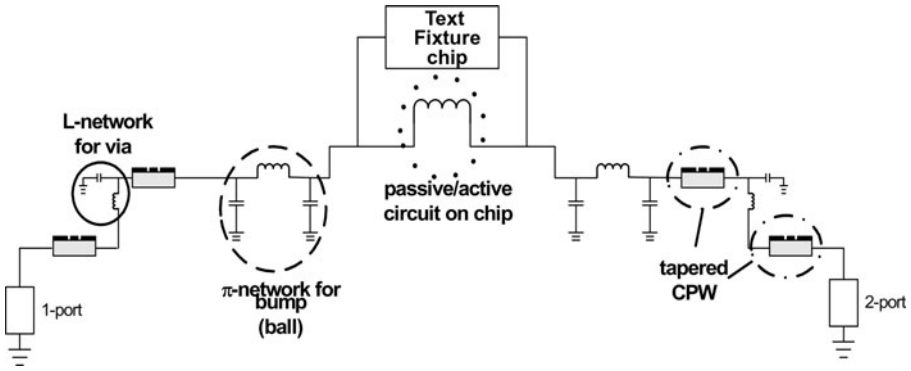

Fig. 7. Equivalent circuit for on-strip measurement structure.

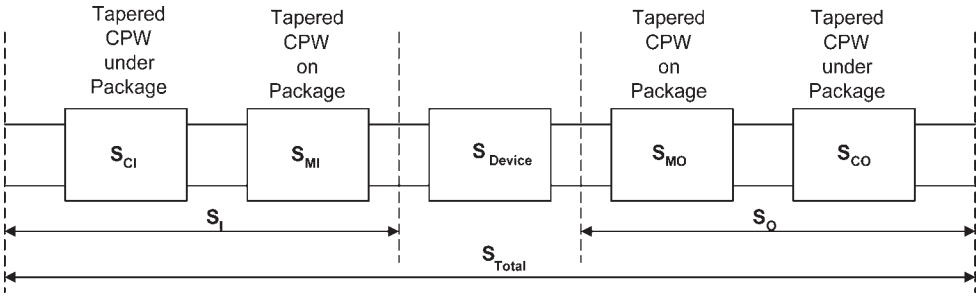

Fig. 8. Simplified chip-to-package transition for de-embedding application.

capacitance between the metal layer and the grounded substrate. The equivalent circuit model can be represented as a three separate blocks such that a simplified two-port network is created [17]. The model parameters are extracted by *Y*-parameters.

The equivalent circuit model can also be determined by extracting component values from the measured *Y*-parameters. Each block of this network is extracted from the measured *Y*-parameters such that

$$\begin{aligned} Y_s &= -Y_{12}, \\ Y_{in} &= Y_{11} + Y_{12}, \\ Y_{out} &= Y_{22} + Y_{12}. \end{aligned} \tag{11}$$

Corresponding equivalent parameters and self-resonance frequency are calculated using equations (7) that are shown in Table 1.

$$\begin{aligned} L_s &= -\frac{im(1/Y(1,2))}{2\pi f}, \\ C_1 &= \frac{im(Y(1,1)+Y(1,2))}{2\pi f}, \\ C_2 &= \frac{im(Y(2,1)+Y(2,2))}{2\pi f}, \\ R_s &= -real\left(\frac{1}{Y(1,2)}\right), \\ SRF &= \frac{1}{2\pi\sqrt{L_s C_1}}. \end{aligned} \tag{12}$$

The measured wirebond inductor has a outer dimension of 160 μm by 160 μm, a metal trace width of 10.7 μm, metal thickness of 3 μm, and metal spacing between traces of 2.1 μm. The measured flip-chip inductor uses the same geometrical characteristics of the wirebond inductor with the exception of the presence of the backside metal and bumps.

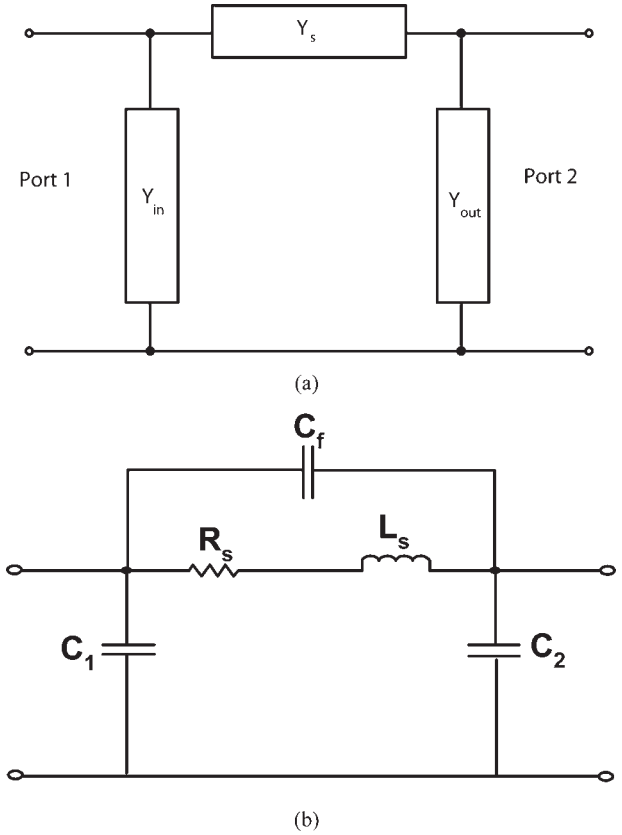

Fig. 9. (a) Simplified two-port network and (b) the equivalent circuit for inductor.

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Table 1. Comparison of inductor characteristics for different package environment at 2 GHz.

	L_s (nH)	C_1 (pF)	C_2 (pF)	C_f (pF)	R_s (Ohm)	Q	SRF (GHz)
Flipped	3.03	0.05	0.03	0.02	4.94	7.7	13.4
Wirebond	3.05	0.03	0.02	0.01	4.16	9.23	15.82

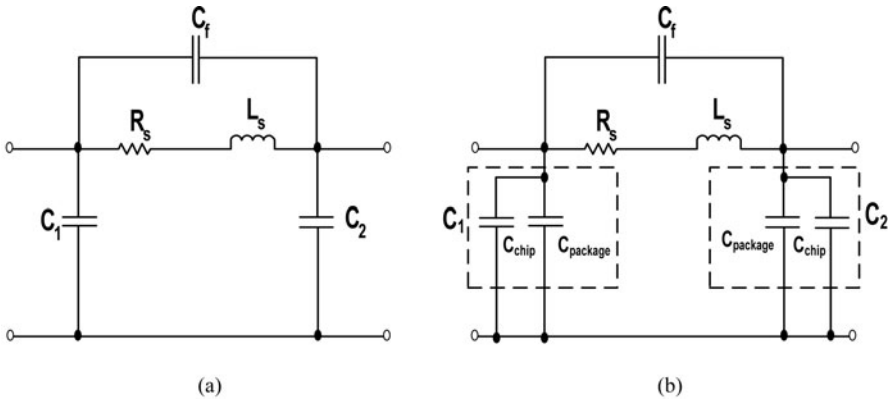

Fig. 10. Equivalent circuit models for spiral inductor on (a) wirebond and (b) flip-chip.

Theses results show the increase of C_1, C_2, and C_f in flip-chip environment. As a result, the self-resonance frequency is decreased with increased parasitic capacitance. This result can be understood because flipped on-chip spiral inductor faces package substrate and ground. In addition, the increase of R_s with flip-chip can be observed in Table 1. The location of the ground plane impacts the RF current return path since electric energy is coupled to the substrate through displacement current. The RF current return path is concentrated on the surface of silicon layer with floating ground because the backside of the die is no longer grounded. Figure 10 shows the equivalent circuit model for a conventional on-chip spiral inductor and a flipped on-chip spiral inductor on package substrate [18]. An equivalent model of flipped on-chip spiral is shown in Fig. 10(b). Parasitic capacitances (C_1 and C_2) of a flip-chip equivalent circuit are divided as C_{chip} and C_{package}. The C_{package} represents the parasitic capacitance between spiral inductor and package substrate. The C_{package} can be affected by different bump height or property of under-fill material. Accurate representation of the circuit is then obtained by minimizing the mean squared error between the Y-parameters and the admittance of each block over the entire frequency range of measured data. To assess the validity of the equivalent circuit models, S-parameter simulation and measurement were carried out as well. Two-port S-parameters were measured instead of a one-port parameter to allow extraction of parasitics from flipped structure. The equivalent circuit model of flipped spiral inductor consists of the equivalent circuit model of spiral inductor and the capacitance for flipped structure.

The measured S-parameters of spiral inductor are with the simulated S-parameters to demonstrate the validity of the model in Fig. 11. When the measured and modeled equivalent circuit S-parameters are compared, good agreements are shown for the cases of wirebond spiral inductor and flipped spiral inductor. Good conformity between the two sets of S-parameter data confirms the validity of our model for the accurate estimation of the flipped spiral inductor model.

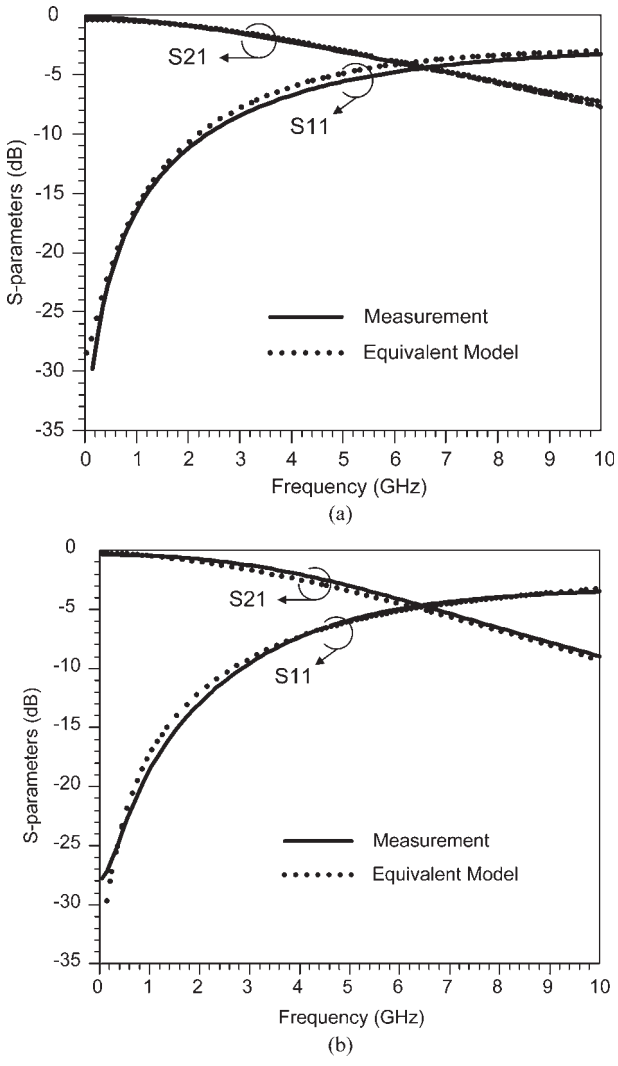

Fig. 11. Equivalent circuit models for spiral inductor on (a) wirebond and (b) flipped structure.

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V. BUMP PROXIMITY EFFECTS

The electrical performance of the complete flip-chip assembled structure cannot be derived by a simple combination of the individual characteristics of each element due to the electromagnetic coupling effect between each element and bump. Accurate estimation of the bump effect in the circuit is one of the main design objectives in flip-chip environment. One key circuit block of RFIC is the VCO blocks, which include an LC tank. To obtain low phase-noise performance, the existence of a high-quality LC resonator of the VCO is required. The Q of the resonator circuit is dominated by the quality factor of the on-chip inductor; hence, the design of such tank circuits is of major importance [19]. In LC tank circuits, the capacitance can be adjusted to tune the resonator frequency. However, the inductance and quality factor of flipped inductor are influenced by flip-chip structure. Figure 12(a) depicts the implementation of signal and ground bumps. The top

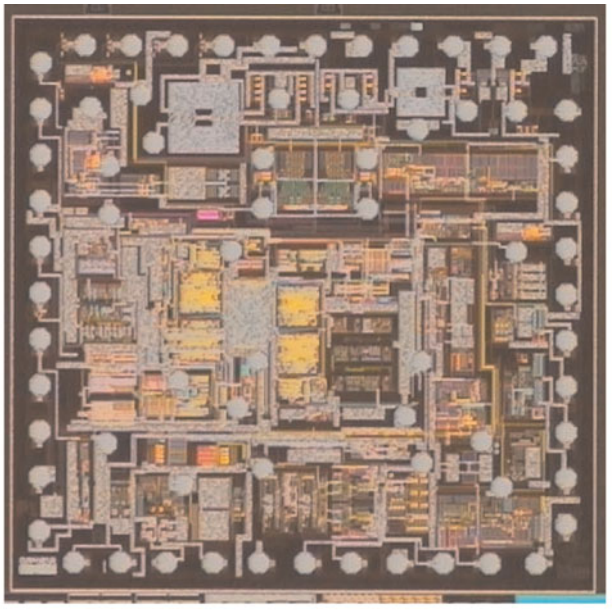

Fig. 12. Fabricated RFIC with (a) flip-chip and (b) wirebond technology.

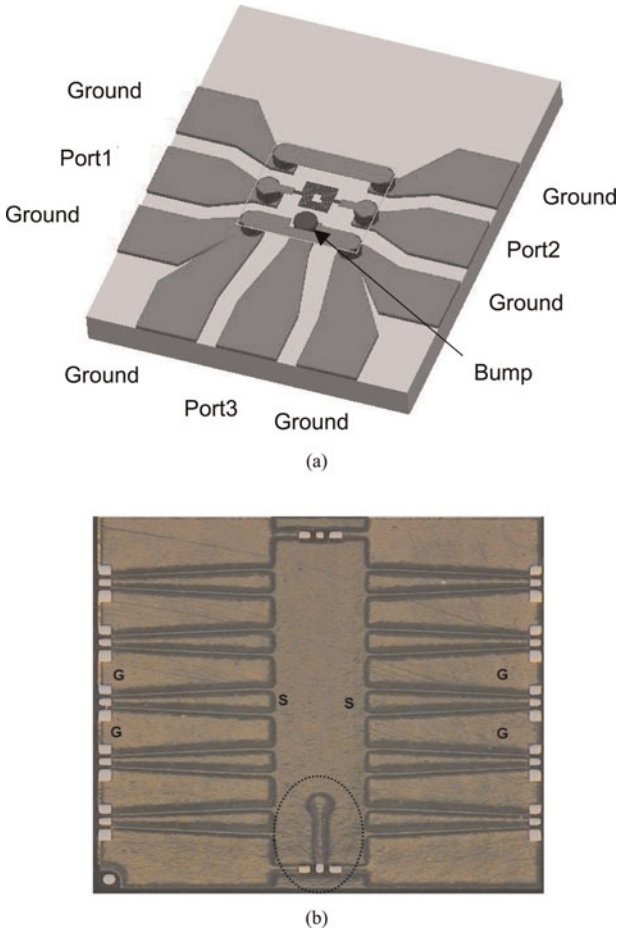

Fig. 13. Three-port structure for (a) electromagnetic simulation and (b) on-strip measurement.

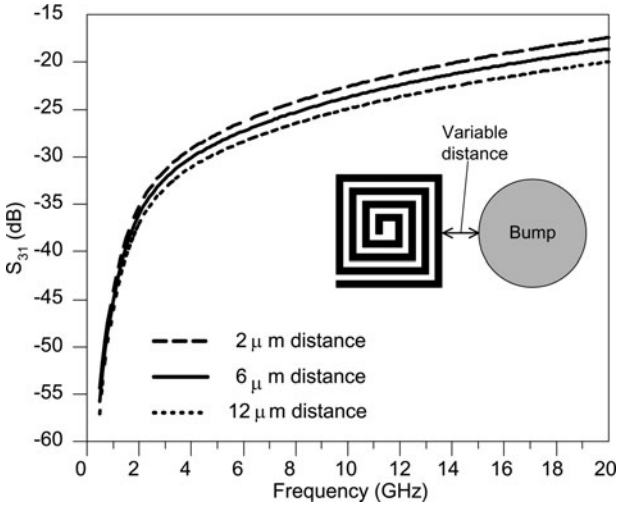

Fig. 14. Simulated S-parameters for bump proximity effects.

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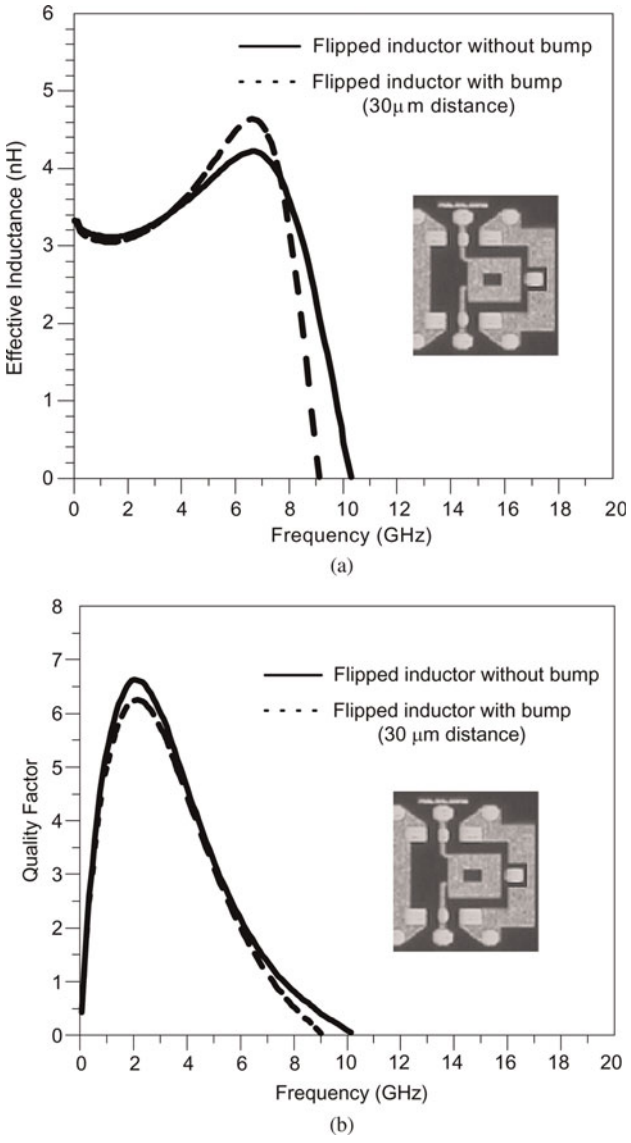


Fig. 15. Measured (a) inductance and (b) quality factor with bump proximity effect.

metal layer can be used for die bump pad, which provides the shortest path to ground in flip-chip environment. The bump proximity effects cannot be ignored in the high-frequency circuit design. Conventional wirebond technology use peripheral pads for wire bonding, which is shown in Fig. 12(b).

The proximity effects of physical separation between inductor and neighboring bump was simulated and measured to examine how the isolation between them varies as the distance between them changes. A 3-D field analysis was used to perform electromagnetic simulation. The structure in Fig. 13(a) was simulated up to 20 GHz. For proximity effects, an RF signal is applied to port 1, while port 2 was connected to 50 Ω to measure output signal and port 3 is sensed to measure the coupled signal. The circled structure of Fig. 13(b) shows the three-port measurement structure under package substrate.

Three pairs of identical spiral inductor and bumps were simulated to examine the isolation (S_{31}) between inductor and bumps. The results in Fig. 14 suggest that the isolation between spiral inductor and bump is improved by the increased gap distance between inductor and bump.

Figure 15 depicts the measured inductance and quality factor with bump proximity effects. At low frequencies, similar inductances are obtained regardless of the technology used. There is no difference in inductance of flipped inductors with and without bump proximity effect. However above 4 GHz, the effective inductance of the inductor with bump proximity is larger than that of the inductor without bump proximity. Since the inductor is orthogonal with bump, mutual inductance between inductor and bump is not significant. By considering the definition of effective inductance, which includes the parasitic capacitance term, it can be noticed that the capacitance contribution is getting significant as frequency approaches its self-resonance frequency. The self-resonance frequency of the inductor with bump proximity is lower than that of the inductor without bump proximity. The variation of self-resonance frequency is explained by the coupling capacitance effects between bump and on-chip inductor.

VI. CONCLUSION

Silicon-based inductors in flip-chip technology are analyzed using full-wave electromagnetic simulation and the laboratory measurement. The results show that the inductance of flipped on-chip spiral inductor is influenced by flip-chip environment. The changed RF current return path for flipped silicon substrate results in significant variations in current density and current distribution in substrate. The changed current density and distribution cause variations in flipped inductor resistance and inductance at high frequencies. The equivalent circuit model of the flipped inductor is verified with measured results over a wide frequency range. The RF flip-chip characterization technique using on-strip measurement method is presented. The transition structures of CPW probes are fabricated on a low-cost package substrate to measure the high-frequency response of RF flip-chip. The application of this method is demonstrated experimentally and theoretically up to 20 GHz. Based on these studies, the proper range of flip-chip parameters to obtain a maximum value of quality factor and self-resonance frequency for designing the optimal structure for RFIC's applications can be determined.

REFERENCES

[1] Lee, G.-A.; Lee, H.-Y.: Suppression of the CPW leakage in common millimeter-wave flip-chip structures. IEEE Microw. Guided Wave Lett., **8** (1998), 366–368.

[2] Niknejad, A.M.; Meyer, R.G.: Analysis, design, and optimization of spiral inductors and transformers for Si RF IC's. IEEE J. Solid-State Circuits, **33** (1998), 1470–1481.

[3] Nguyen, N.M.; Meyer, R.G.: Si IC compatible inductors and LC passive filters. IEEE J. Solid-State Circuits, **25** (1990), 1028–1031.

https://doi.org/10.1017/S1759078709990663 Published online by Cambridge University Press

[4] Burghartz, J.N.: Progress in RF inductors on silicon – understanding substrate losses, in IEEE Int. Electron Device Meeting, 1998, pp. 523–526.

[5] Davis, P. et al.: Silicon-on-silicon integration of a GSM transceiver with VCO resonator, in IEEE Int. Solid-State Circuits Conf., 1998, pp. 248–249.

[6] Kim, J.; Itoh, T.: A novel microstrip to coplanar waveguide transition for flip-chip interconnection using electromagnetic coupling, in 28th European Microwave Conf. Proc., October 1998, pp. 6–8.

[7] Lee, G.-A.; Megahed, M.; De Flaviis, F.: Analysis of PF flip-chip on-chip inductance with novel measurement technology, in Electronic Components and Technology Conf., May 2003, pp. 1253–1257.

[8] Koutsoyannopoulos, Y.K.; Papananos, Y.: Systematic analysis and modeling of integrated inductors and transformers in RF IC design. IEEE Trans. Circuits Systems-II: Analog Digital Signal Process., **47** (2000), 699–713.

[9] Zheng, J.; Tripathi, V.K.; Weisshaar, A.: Characterization and modeling of multiple coupled on-chip interconnects on silicon substrate. IEEE Trans. Microw. Theory Tech., **49** (2001), 1733–1739.

[10] Ramo, S.; Whinnery, J.R.; Van Duzer, T.: Fields and Waves in Communication Electronics, 3rd ed., Wiley, New York, 1994, pp. 324–330.

[11] Tegopoulos, J.A.; Kriezis, E.E.: Eddy Currents in Linear Conducting Media, Elsevier, Amsterdam, The Netherlands, 1985.

[12] Chun, C.; Pham, A.-V.; Laskar, J.; Hutchison, B.: Development of microwave package models utilizing on-wafer characterization techniques. IEEE Trans. Microw. Theory Tech., **45** (1997), 1948–1954.

[13] Imparato, M.; Weller, T.; Dunleavy, L.: On-wafer calibration using space-conservative (SOLT) standards, in IEEE MTT-S Int. Microwave Symp. Digest, June 1999, pp. 1643–1646.

[14] Arai, Y.; Sato, M.; Yamada, H.T.; Nagai, K.; Fujishiro, H.I.: 60-GHz flip-chip assembled MIC design considering chip-substrate effect. IEEE Trans. Microw. Theory Tech., **45** (1997), pp. 2261–2266.

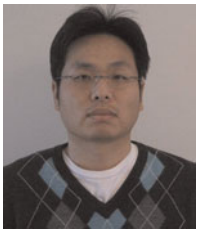
[15] Gonzalez, G.: Microwave Transistor Amplifiers, Prentice-Hall, Englewood Cliffs, NJ, 1997.

[16] Cho, H.; Burk, D.E.: A three-step method for the de-embedding of high-frequency S-parameter measurements. IEEE Trans. Electron Dev., **38** (1991), 1371–1375.

[17] Pozar, D.M.; Microwave Engineering, Addison-Wesley Publishing Company, Reading, MA, 1990.

[18] Patrick Yue, C.; Simon Wong, S.: On-chip spiral inductors with patterned ground shields for Si-based RF IC's. IEEE J. Solid-State Circuits, **33** (1998), 743–752.

[19] Burghartz, J.N.; Edelstein, D.C.; Soyuer, M.; Ainspan, H.A.; Jenkins, K.A.: RF circuits design aspects of spiral inductors on silicon. IEEE J. Solid-State Circuits, **33** (1998), 2028–2034.



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