

RESEARCH PAPER

Drain current transient and low-frequency dispersion characterizations in AlGaIn/GaN HEMTs

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This paper presents a detailed trap investigation based on combined pulsed I/V measurements, drain current transient (DCT) measurements and low-frequency dispersion measurements of transconductance (LF $Y_{2,1}$) and output conductance (LF $Y_{2,2}$). DCT characterization is carried out over a 7-decade time scale. LF $Y_{2,1}$ and $Y_{2,2}$ measurements are carried out over the frequency range from 100 Hz to 1 GHz. These combined measurements were performed at several temperatures for AlGaIn/GaN high electron mobility transistors under class AB bias condition and allowed the extraction of the activation energy (E_a) and the capture cross section (σ_c) of the identified traps. Extensive measurements of these characteristics as a function of device bias are reported in this work to understand the dynamic trap behavior. This paper demonstrated a correlation between LF small-signal (LF $Y_{2,1}$ and $Y_{2,2}$) and large-signal voltage steps (DCT) results. These measurements allow identifying the same 0.64 eV deep level, attributed to a native defect of GaN, possibly located in the buffer layer.

Keywords: Deep level transient spectroscopy (DLTS), Transconductance frequency dispersion, Output conductance frequency dispersion, Defects, Gallium nitride, High electron mobility transistor (HEMT), Trap levels

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1. INTRODUCTION

High electron mobility transistors (HEMTs) based on AlGaIn/GaN heterostructures have shown impressive performances, in terms of high-electron mobility, high-power density, high cut-off frequency and high-thermal conductivity. As a consequence, they represent the most promising candidates for future power switching and microwave applications. However, GaN technology suffers from an important lack of knowledge and poor control of trapping effects such as current collapse (CC) and knee walkout. These trapping effects combined with thermal effects lead to a limitation of their performances [1, 2] under modulated large-signal dynamic excitations. In order to get insight into working mode of trapping effects, several techniques have been proposed:

- (1) Pulsed I/V measurements, carried out at several quiescent bias points to quantify the CC [3], to obtain a preliminary characterization and to understand which trapping mechanisms may affect the transistor performance [4];

- (2) Current deep-level transient spectroscopy (I-DLTS) analysis [5, 6] through stretched multiexponential fitting of the drain current transient (DCT) measurements [7] can provide information on the E_a and σ_c of the trap levels involved in CC;
- (3) Output conductance frequency dispersion [8, 9] and transconductance frequency dispersion [10] based on low-frequency (LF) 2-port S-parameters measurements can provide information on the trap characteristics (E_a and σ_c) promoted by small-signal excitation at fixed bias point.

The aim of this paper is to contribute to better understand trapping phenomena from DC to radio-frequency (RF) range with the combination of these three characterization techniques. The frequency dispersion of electrical characteristics is important, for microwave circuit design, in the way that the trapping phenomena reduce significantly the transconductance and output conductance. Therefore, it is of prime importance to introduce those LF small-signal parasitic effects and I-DLTS in CAD models, in order to be able to predict more accurately the RF dispersion when the transistor is driven by pulsed-RF large-signal excitations [11, 12]. In the following section, the pulsed I/V characteristics are presented, and associated with a specific procedure allowing the identification of traps. Section III is dedicated to DCT measurements, with emphasis on activation energies and capture cross sections of three main traps. Section IV describes the transconductance and output-conductance

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frequency dispersion technique; in particular, the new way to determine the E_a and σ_c , and to identify the traps from the LF dispersion of the transconductance is presented. Finally, Section V presents the comparison of the extracted trap characteristics using the different measurement techniques. It also discusses and compares the Arrhenius plot results found by DCT and transconductance and output-conductance frequency dispersion techniques with previous papers on defects in GaN.

II. PULSED CHARACTERIZATION

The devices used for this study are 2 mm ($8 \times 250 \mu\text{m}$), $0.5 \mu\text{m}$ gate length AlGaIn/GaN GH50 HEMTs (from UMS foundry), grown on SiC substrate, with a SiN passivation layer. The devices were submitted to a complete pulsed I/V characterization aimed at identifying the presence of traps and quantifying CC. Pulsed I/V characterization was carried out by means of a commercial 250 V/10A pulsed I/V BILT AMCAD system [13]. Figure 1(a) reports the results of pulsed I_D - V_D characterization and Fig. 1(b) shows the g_m variation (extracted from I_D - V_G measurements) for different quiescent bias points:

- Q_1 : (V_{GQ}, V_{DQ}) = (0 V, 0 V), which corresponds to negligible electron trapping;
- Q_2 : (V_{GQ}, V_{DQ}) = (-5 V, 0 V), which may favor the trapping of electrons under the gate region (gate-lag);
- Q_3 : (V_{GQ}, V_{DQ}) = (-5 V, 40 V), which may favor the trapping of electrons under the gate-drain region (drain-lag);
- Q_4 : (V_{GQ}, V_{DQ}) = (-1.9 V, 40 V), which is representative of electron trapping under class AB bias condition ($I_{DS} = 50 \text{ mA}$ at $V_{DQ} = 40 \text{ V}$).

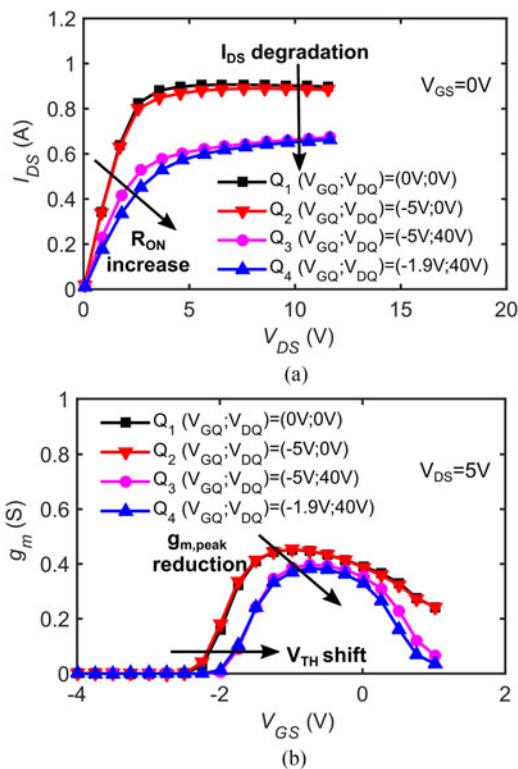


Fig. 1. (a) I_D - V_D and (b) g_m (derived from I_D - V_G) pulsed characterizations for different quiescent bias points.

The results of pulsed I_D - V_D measurements indicate that the device is less sensitive to gate-lag than to drain-lag: the gate filling pulse V_{GQ} has a negligible effect on device characteristics, while the application of V_{DQ} induces a strong CC and degrades the R_{ON} value. By comparing the OFF-state quiescent bias point (-5 V, 40 V) with SEMI-ON state, class AB bias condition (same V_{DQ} but $V_{GQ} = -1.9 \text{ V}$), it can be noticed that the CC is relatively unchanged but the R_{ON} degradation is enhanced.

Transconductance (g_m) measurements, shown in Fig. 1(b), show that drain-lag (point Q_3) induces both a positive threshold voltage shift and a g_m reduction (-15% at peak and more pronounced at higher V_{GS}). The Q_4 quiescent point presents the same threshold voltage shift and a slightly more pronounced g_m decrease with respect to Q_3 . These results suggest that CC is related with negative charge trapping both under the gate and in the access regions.

III. DCT MEASUREMENTS

The properties of the traps, responsible for CC, were investigated by DCT measurements. The experimental set-up used for DCT measurements is shown in Fig. 2.

In this set-up, the DCT is determined by measuring the differential voltage on a resistive load ($R_{SENSE} = 10 \Omega$) connected between the drain of transistor and the drain pulser. The drain pulse signal is linearly amplified to reach the required values of drain current and voltage. The scope is then triggered with a synchronous pulsed signal generated by the drain pulser. The delay introduced by the linear DC power amplifier (PA) has a negligible effect on the synchronized biasing and DC measurement of transistor. The transistor is first biased by applying a 100s filling pulse (V_{GF}, V_{DF}), thus inducing a specific trapping state. Subsequently, the device is switched to a different bias point in the saturation region (V_{GM}, V_{DM}) = (-1.7 V, 5 V); the recovery of drain current related to charge detrapping is measured over 7 time decades (from $10 \mu\text{s}$ to 100 s) by means of a digital sampling oscilloscope. For the extraction of the time constants the DCT data were fitted by a stretched multiexponential function [7]:

$$I_{DS,fitting}(t) = \sum_i^N A_i e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} + I_{DS,final}, \quad (1)$$

where A_i , τ_i , and β_i are fitting parameters corresponding respectively, to trap amplitude, time constant and the

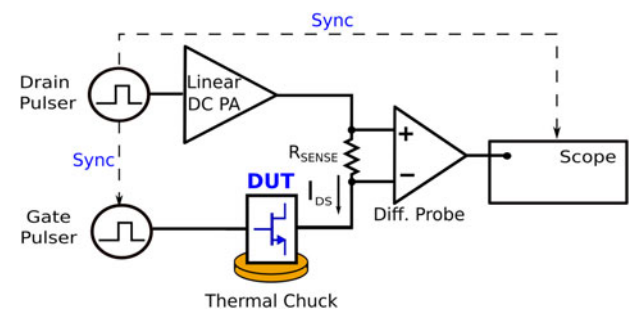


Fig. 2. Block diagram of thermal DCT measurement set-up.

stretching parameter ($0 < \beta < 1$) of N detected charge trapping. In trapping (detrapping) behavior, $A > 0$ ($A < 0$) corresponds to emission and $A < 0$ ($A > 0$) corresponds to capture process. Therefore, the extracted time constants with applied temperature correction [14] allow us to determine the apparent activation energy E_a and the capture cross section σ_c by using the Arrhenius' equation written as

$$e_n(T) = \gamma T^2 \sigma_c \exp\left(-\frac{E_a}{kT}\right), \quad (2)$$

with $e_n = 1/\tau_n$ and $\gamma = 2\sqrt{3}(2\pi)^{(3/2)}k^2m \times h^{-2}z$, where τ_n is the time constant, e_n is the emission rate, T is the temperature, m^* is the effective electron mass, h is the Planck constant and k is the Boltzmann constant.

To achieve complementary information about CC, DCT measurements were carried out, starting from three different filling bias conditions (V_{GF}, V_{DF}) (corresponding to the quiescent bias points used in the previously described pulsed I/V measurements). The results are shown in Fig. 3. The OFF-state condition defined by (V_{GF}, V_{DF}) = (-5 V, 10 V) induces negligible trapping. The emission process "E4" shows a high drain voltage dependence and clearly appears for the two following conditions: OFF state is defined by (V_{GF}, V_{DF}) = (-5 V, 40 V) and SEMI-ON state is defined by (V_{GF}, V_{DF}) = (-1.9 V, 40 V). Furthermore, the emission process "E2" and the capture process "E3" are mostly induced by the (V_{GF}, V_{DF}) = (-1.9 V, 40 V) bias condition. In order to investigate the properties of traps for the SEMI-ON state, the DCT measurements were carried out at different temperatures. The time spectrum analysis and Arrhenius plot are reported, respectively, in Figs 4(b) and 4(c). The analysis for the SEMI-ON state is very interesting because it gives information on which traps will affect class AB operation mode of the transistor in a PA. It can be

noticed that all emission and capture processes "E2", "E3", and "E4" will take place in this class AB operation mode.

IV. LF DISPERSION MEASUREMENTS

Output-conductance and transconductance of GaN HEMTs have been observed to change significantly at LF (100 KHz–100 MHz) [10]. So, in order to gather complementary information on trapping effects under class AB operation mode, the LF Y -parameters dispersion are investigated through small-signal S -parameters measurements in the 100 Hz–1 GHz frequency range. These S -parameters measurements were carried out at several temperatures using a LF–HF Vector Network Analyzer (VNA; Agilent E5061b) to determine $g_d(f)$ and $g_m(f)$ dispersion. As illustrated in Fig. 5, the V_{GS} is applied to LF home-made bias tee [15] with DC port connected to power supply and the RF port connected to port 2 of VNA. The drain terminal is connected to internal bias system (port 1) to the network analyzer. On-wafer SOLT calibration is performed at each individual temperature.

So, the Y -parameters are calculated from the measured S -parameters [16]. Empirically, the effect of carrier trapping

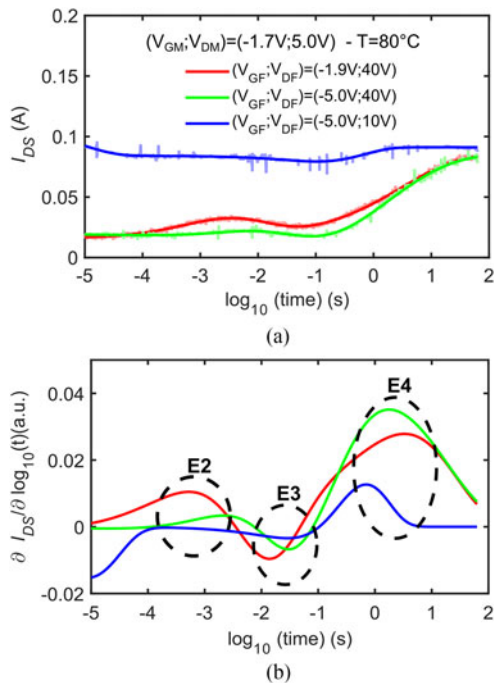


Fig. 3. (a) DCT recorded and fitting for three different trapping conditions at 80 °C (b) related time spectrum analysis.

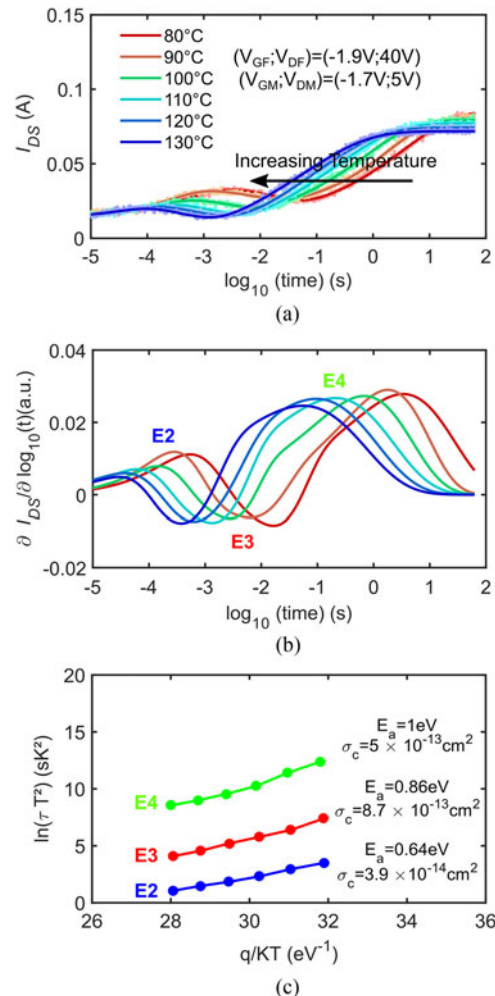


Fig. 4. (a) DCT recorded and fitting in SEMI-ON state condition for 80–140 °C temperature range, (b) related time spectrum analysis and (c) related Arrhenius plot.

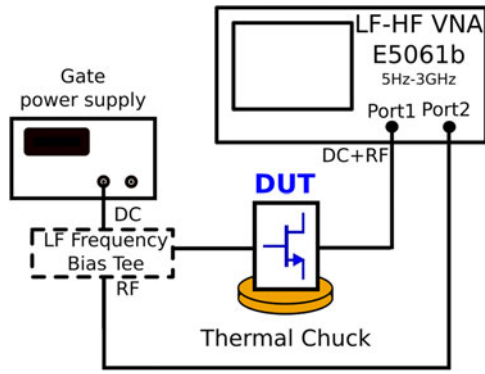


Fig. 5. Block diagram of the LF Y-parameters measurement set-up in 2-port configuration for the characterization of $g_d(f)$ and $g_m(f)$.

on frequency dispersion of output-conductance and transconductance can be modeled as reported in [17]. The dispersion effects are taken into account with an additional voltage dependent current source (that represents the injection mechanism in trap state) in a RC circuit as shown in Fig. 6.

According to this small-signal model at LF, $g_m(f)$ and $g_d(f)$ can be deduced from the Y-parameters of the Device Under Test, respectively, Y_{21} and Y_{22} parameters by the following equations:

$$Y_{21}(\omega) = \left(g_m - \frac{g_{mn}(\omega\tau_n)^2}{1 + (\omega\tau_n)^2} \right) - j \frac{g_{mn}(\omega\tau_n)}{1 + (\omega\tau_n)^2}, \quad (3)$$

$$Y_{22}(\omega) = \left(g_d + \frac{(g_{mn} + g_n)(\omega\tau_n)^2}{1 + (\omega\tau_n)^2} \right) + j \frac{(g_{mn} + g_n)(\omega\tau_n)}{1 + (\omega\tau_n)^2}, \quad (4)$$

$\tau_n = C_n/g_n$ corresponds to the time constant of trapping process. For the extraction of time constants, the derivative forms of imaginary part of Y_{21} and Y_{22} are used. In this way, the emission constants due to $g_m(f)$ dispersion can be extracted either from peak values of Y_{21} imaginary part ($f_{imag}(Y_{21}) = 1/2\pi\tau_n$) and the emission constants due to $g_d(f)$ dispersion can be extracted either from peak values of Y_{22} imaginary part ($f_{imag}(Y_{22}) = 1/2\pi\tau_n$). The number of traps of $g_m(f)$ ($g_d(f)$) is defined by the number of peaks of the Y_{22} imaginary part (Y_{21} imaginary part) or by the number of inflexion points of the Y_{22} real part (Y_{21} real part) [9]. As it is demonstrated, the peak values of Y_{21} and Y_{22} imaginary parts at several temperatures allow extracting the E_a and σ_c (associated respectively, to $g_m(f)$ and $g_d(f)$ dispersion) using the Arrhenius formula (2) and

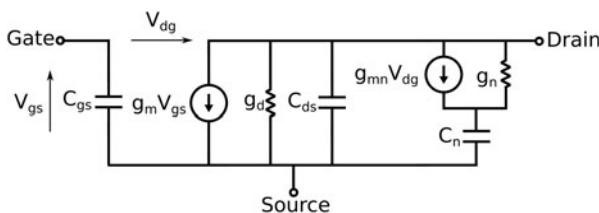


Fig. 6. Empirically equivalent circuit model for output-conductance and transconductance dispersions.

substituting the emission rate with the reciprocal of time constant ($e_n = 1/\tau_n$). A temperature correction [14] is applied to determine E_a and σ_c . LF Y-parameters measurements for the SEMI-ON state ($V_{GS}, V_{DS}) = (-1.9 \text{ V}, 40 \text{ V})$ were carried out at different temperatures to obtain the Arrhenius plot, as shown in Figs 7 and 8. This analysis is focused only on Y_{21} and Y_{22} because the experimental data of Y_{11} and Y_{12} do not show any dispersion. The Y-parameters, depicted in Figs 7 and 8, show that above the 100 MHz frequency, the contribution of intrinsic capacitors of small signal model is not negligible.

The Y_{21} -measurement shows two distinct transition frequencies in $\text{Real}(Y_{21})$ and two distinct peaks in $\text{Imag}(Y_{21})$, proving that $g_m(f)$ dispersion presents two trapping phenomena. The peak of Y_{21} imaginary part corresponds to the transitions in the transconductance (Y_{21} real part). The Fig. 7(a) shows a significant decrease of the transconductance ($\text{Real}(Y_{21})$) amplitude with the increase of the temperature due to thermal effects. On the one hand, the first transition appears at LF (approximately 5–10 KHz for 80 °C). On the other hand the $\text{Real}(Y_{21})$ increases when the frequency decreases. The conclusion of these two last observations is

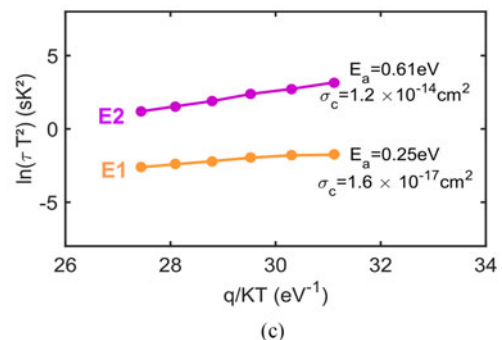
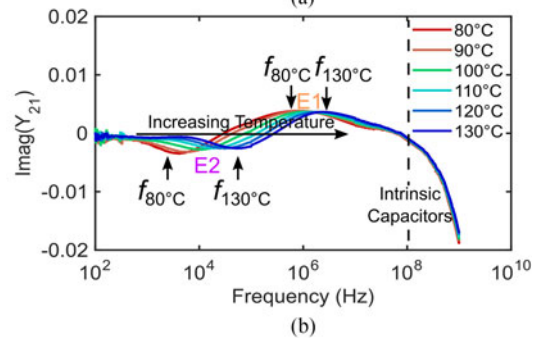
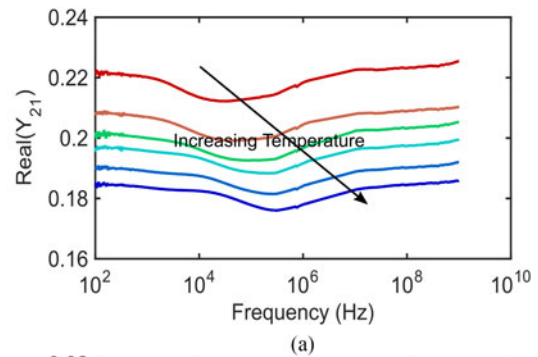


Fig. 7. (a) Y_{21} real part versus frequency for 80–130 °C temperature range, (b) Y_{21} imaginary part versus frequency for 80–130 °C temperature range and (c) related Arrhenius plot.

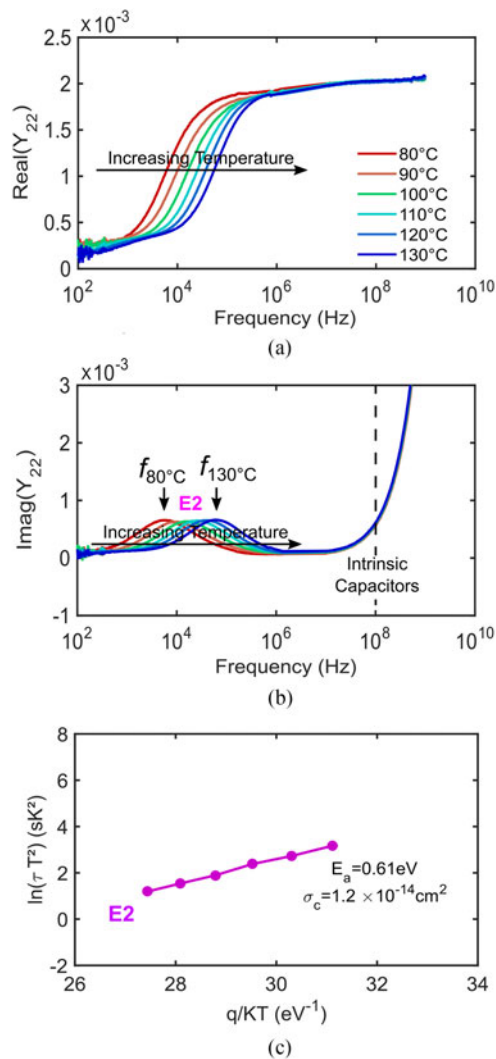


Fig. 8. (a) Y_{22} real part versus frequency for 80–130 °C temperature range, (b) Y_{22} imaginary part versus frequency for 80–130 °C temperature range and (c) related Arrhenius plot.

that the trap (label “E2”) can be associated with an emission process. Considering that $\text{Real}(Y_{21})$ decreases when the frequency decreases and considering that the time constant of trap “E1” is approximately 1 μs (range of capture time constant), the trap “E1” can be associated with a capture process. Output conductance dispersion for the same device is presented in Fig. 8. The Y_{22} real part ($\text{Real}(Y_{22})$) corresponding, in a first approximation, to the output conductance g_d (or the reciprocal of output resistance) shows one inflexion point. So $g_d(f)$ dispersion presents one trap that corresponds to trap “E2” found by $g_m(f)$ dispersion according to [18]. Moreover, for the process “E2” we found the same time constants by $g_d(f)$ and $g_m(f)$ dispersions. Thus, the traps “E1” and “E2” are promoted by two mechanisms: the first one appears only when the small-signal is applied to gate port, this suggests that the trap is located under the gate. The second trapping mechanism is due to hot electrons as explained in the next Section. The transconductance and output conductance frequency dispersions promoted by the process “E2” can be explained in this way: if the detrapping time constant is much higher than the signal period, traps cannot respond as quickly as the applied voltage. On the

other hand, when the detrapping time constant is of the same order of the signal period, the trapped electrons due to the injection of highly energetic (hot) electrons are emitted and they participate to the RF current-carrying process giving rise to frequency dispersion in the device.

V. IDENTIFICATION OF THE DEEP LEVELS

A) Trap signatures

The overall Arrhenius plot provided by I-DLTS, transconductance and output-conductance frequency dispersion measurements is shown in Fig. 9.

To obtain more detailed information of trap properties, the deep levels observed in Fig. 9 are compared with deep levels previously reported in literature [5, 7, 19–50].

From Fig. 9, the emission process “E2” obtained from DCTs measurements is characterized by $E_a = 0.64$ eV and $\sigma_c = 3.9 \times 10^{-14}$ cm². The emission trap process obtained from transconductance and output-conductance frequency dispersion measurements is characterized by $E_a = 0.61$ eV and $\sigma_c = 1.2 \times 10^{-14}$ cm². For the first time, to our knowledge, the correspondence of the trap characteristics allows concluding that the same trap level “E2” is extracted from the two different measurements. Moreover, the Y_{21} imaginary part and the Y_{22} imaginary part in Figs 7 and 8 shows a rightward shift of the peaks when the temperature increases. This frequency shift, from 5 kHz (at 80 °C) to 65 kHz (at 130 °C), converted in the time domain corresponds to a same time constant shift observed in I-DLTS measurements (Fig 4(a)) when the temperature increases. This level “E2” is supposed to be due to a native defect of GaN, based on the comparison with previous reports [7, 49, 50].

The level “E3” ($E_a = 0.86$ eV; $\sigma_c = 8.7 \times 10^{-13}$ cm²) obtained from DCTs measurements, reveals similar signature to deep levels already associated with nitrogen-related defects [19, 35] present in the GaN layer.

The level “E4” ($E_a = 1$ eV; $\sigma_c = 5.0 \times 10^{-13}$ cm²) characterized by DCTs measurements, shows a correspondence with the signature of deep levels associated with extended defects in GaN [7, 27].

Finally, the level “E1” ($E_a = 0.25$ eV; $\sigma_c = 1.6 \times 10^{-17}$ cm²) characterized by LF Y_{21} measurements, shows again a correspondence with the signature of deep levels associated with nitrogen-related defect [30, 31].

B) Filling time dependence

To obtain more information on the trap dynamic behavior, the evolution of the “E2”, “E3”, and “E4” time spectrum results is reported versus the duration of filling pulse in Fig. 10(a). For this investigation, the trapping phenomena were induced by applying $(V_{GF}, V_{DF}) = (-1.9$ V, 40 V) at constant temperature (100 °C). The width of filling time varies from 100 μs to 100 s. As described in Fig. 10, the “E4” amplitude increases with time and saturates for long pulse width. This behavior can be explained by two possible hypotheses. The first one is related to the presence of linear line defects, possibly due to dangling bonds along dislocation core sites. As described in [51], the concentration of the

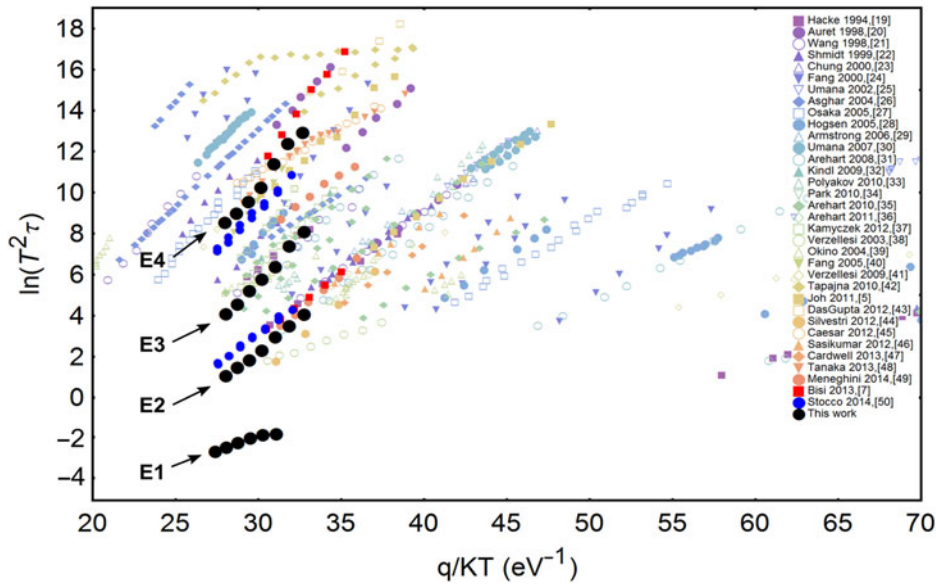


Fig. 9. Arrhenius plot of deep levels “E1”, “E2”, “E3” and “E4” detected within this paper. Presentation of trap states reported in previous papers for comparison (data taken from [7] and references therein).

ionized defects has a logarithmic dependency on duration of filling pulse (t_p) according to the following formula:

$$n_T(t_p) = c_n \cdot \tau \cdot N_T \cdot \ln\left(1 + \frac{t_p}{\tau}\right), \quad (5)$$

where c_n , τ , and N_T , respectively, represent the capture probability, the characteristic time for the capture barrier build-up and the total concentration of the defects. Before the saturation of trap occupancy, the charge filling time may

produce a capture rate reduction due to repulsive interaction between the free electrons and the increased negatively charged traps. The second one is related to the presence of acceptor-like traps, where the filling time is associated with the emission of holes to the valence band [52]. Simultaneously, the “E2” amplitude decreases when the pulse width increases up to a value, which corresponds to the saturation of ionized “E4” traps. The evolution of “E4” and “E2” amplitudes with the filling time suggests that there may exist an equilibrium between the ionization of the two trap states.

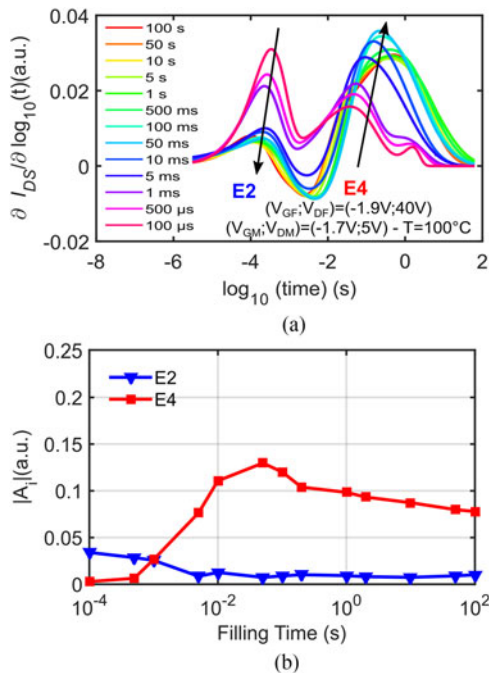


Fig. 10. (a) E2 and E4 time spectrum analysis and (b) related amplitude processes dependency with the filling pulse duration.

C) Capture mechanism: dependence on gate bias and temperatures

To further investigate on the trapping behavior due to the RF working conditions, a complete analysis of CC dependence with the gate quiescent bias point (swept from -5 to -1.5 V) was performed. It allows emulating the RF sweep condition (that corresponds to a constant DC value of V_{DS} and an increase DC value of I_{DS} with the increase of input power). The results of this CC analysis (evaluated at $V_{GS} = 0$ V and $V_{DS} = 10$ V) are summarized in Fig. 11. It shows that for OFF state ($V_{GS} < -2.4$ V) the CC is constant and for ON state ($V_{GS} > -2.4$ V) the CC increases significantly with the drain current I_{DS} . These variations cannot be due to the temperature increase when the drain current increases because Fig. 11 proves that the CC does not depend on the temperature of the device.

The CC increase for ON state can rather be attributed to the injection of hot electrons towards traps located in the buffer, in this case trap “E2” and/or trap “E4”. This hypothesis is also reported in [49], which associates this phenomenon to trap “E2” and shows an increase of amplitude’s process with increase of gate quiescent bias point. It is then demonstrated that the CC is strongly correlated to the value of gate quiescent bias conditions in the ON state.

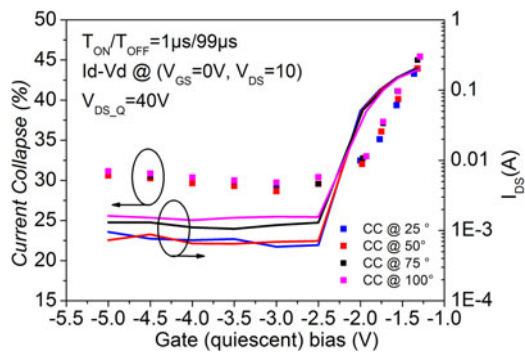


Fig. 11. Thermal dependence of CC and I_{DS} versus gate quiescent bias point for a 40 V drain quiescent bias point.

VI. CONCLUSION

In this work, a detailed investigation of the trapping processes in AlGaIn/GaN HEMTs under class AB bias condition is described. It is based on combined pulsed I/V measurements (which provide an identification of the possible trap position), I-DLTS investigation (which provide data on the large-signal voltage steps detrapping transient, suitable for deep-level analysis) and LF transconductance and output-conductance measurements (which provide small-signal trap analysis). The pulsed I/V measurements under class AB bias condition detected a shift in the threshold voltage, a significant increase in the resistivity of the gate–drain access region, and a decrease in the transconductance peak. Moreover, pulsed I/V characterization carried out at several temperatures shows that the CC increases when the gate quiescent bias point increases (due to hot electrons). This phenomenon can impact seriously the dynamic performances of the transistor. The properties of the trap responsible for CC are investigated with I-DLTS. This technique has evidenced three traps with the following activation energies: $E_4 = 1$ eV, $E_3 = 0.86$ eV, and $E_2 = 0.64$ eV. For the first time, the level “E2” has been found to have a good matching with the trap level identified by the transconductance and output-conductance frequency technique, which is supposed to be due to a native defect GaN. The features of the pulsed I/V measurement suggest that these defects are located in the GaN buffer layer. The DCT technique is very powerful because of drain current sensitivity to trap parameter analysis. The time constants and amplitude of the traps are extracted by a stretched multiexponential function for trapping or detrapping phenomena. Real-time trapping behaviors are observed thanks to accurate records over a 7-decade time scale allowing investigation of slow and fast trapping phenomena. The transconductance and output-conductance frequency dispersion technique can provide trap information (E_a and σ_c) using small-signal excitations close to real continuous wave RF operation mode. This trapping extraction method (LF Y_{21} and LF Y_{22}) is based on the 2-port S -parameters measurement that directly provides information of the current corresponding to g_m and g_d (in a first approximation). The advantage of this method lies in the g_m and g_d sensibility to the drain-lag trapping effects. LF Y -parameters characterization is very accurate because it is based on the use of VNA measurements. This method provides a fast characterization of trapping phenomena but suffers from the lack of a quantitative determination of trap density.

The complexity of the LF dispersion characterization and the scarcity of its analysis makes difficult to determine at the moment a detailed theoretical model of trap “E1”. But, the extraction technique of activation energies and capture cross sections for detected traps, based on temperature-dependent measurements of the imaginary part of Y_{22} and Y_{21} , is demonstrated.

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