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RESEARCH PAPER

Performance study of an inverse class E power amplifier with series tunable parallel resonant tank

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An analysis of operation of a modified inverse class E power amplifier is presented. The proposed amplifier that has a series tunable parallel resonant tank is similar to a hybrid of class F and inverse class E. The principles and design equations required to determine the optimum operation of the amplifier are analyzed in detail. The practical circuit using LDMOS MRF21010 is shown to be able to deliver 40.02 dBm outpout power at 155 MHz. The amplifier achieves power-added efficiency (PAE) of 78.18% and drain efficiency of 78.42%, and exhibits 25.02 dB power gain when operates from a 21 V supply voltage. Comparisons of simulated and measured results are given with good agreement between them being achieved.

Keywords: Inverse class E amplifier, class F, zero current switching, high efficiency

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I. INTRODUCTION

As the demand for wireless communications continues to grow, the requirement of high-efficiency, high-frequency power amplifiers has never been greater. The operating and deployment costs of wireless base stations and the mobility of user terminals can be significantly optimized by increasing the efficiency of the power amplifiers in the final output stage.

Unfortunately, there is often a trade-off between amplifier efficiency and amplifier linearity. To fulfill the stringent linearity requirements of wireless communication standards while achieving high efficiency, designers propose some advanced transmitter architectures, such as linear amplification using non-linear components (LINC) [1], envelope elimination and restoration [2], and polar amplifiers [3]. It is generally believed that switching-mode power amplifiers that can offer unity theoretical efficiency are the most promising solution in these transmitter architectures.

Class E [4–6] and class F [7] are two well-known switching-mode power amplifier topologies that have demonstrated high performance at radio and microwave frequencies, whereas there are some limitations when designing them. Class E amplifier's high drain voltage is very dangerous to the transistor's safety, and class F amplifier needs complex tuned circuits to supply open and short circuits to the alternating harmonics. To address these limitations, some new designs that unify class E and class F or class 1/F [8, 9] into a single framework were proposed [10–14]. It is a pity that these literatures have not introduced exact design equations or simple design process of the class FE and class E/F power amplifier topologies. In 2005, a new topology for the class E amplifier has been reported by T. Mury. Termed as the inverse class E amplifier it has several advantages over the classical class E configuration [15–18]. For example, when compared with the classic class E topology the inverse class E amplifier offers (i) lower inductance values, which is more attractive for lumped MMIC implementation, (ii) better harmonic suppression when operated into a distributed load network, and (iii) lower peak switching voltages, which reduces the possibility of the device failure owing to transistor breakdown mechanisms [17, 18]. However, the inverse class E amplifier does not further the power output capability and has higher drain current when compared with the class E mode. A modified class E amplifier with tunable serial–parallel resonator network that replaces the single parallel capacitor of the classic class E mode was proposed in [6]. The results have shown that the modified topology is able to improve the power output capability, whereas the proposed circuit also has high drain voltage.

In this paper, we have introduced a tunable parallel resonant tank into the load network of the inverse class E amplifier. The new configuration is similar to a hybrid combining features of inverse class E and class F or class1/F, and demonstrates varying degrees of trade-off between the peak drain voltage and current when the added parallel resonant is tuned to the different frequency. The proposed amplifier not only maintains the zero power loss switching operation, but also brings in some improvements, such as higher output power, power output capability, and further relaxes design requirements. This paper is organized as follows: In Section II, the theoretical

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analysis and the design equations for the new topology operating under ideal switching conditions are given in detail. Section III will present amplifier's performance supported by numerical results when the added parallel resonant tank tuned to the different frequencies. In Section IV, circuit harmonic balance simulations and experiments are carried out to validate the theories. And Section V presents the conclusion.

II. FUNDAMENTAL THEORY

Figure 1 depicts the circuit schematic diagram of the amplifier proposed in this paper. The transistor operates cyclically as an ideal switch at the fundamental frequency (ω); the load network is similar to the inverse class E amplifier, but it has a more parallel resonant tank $C_n//L_n$, the resonance frequency of this parallel resonant circuit is $n\omega$, where n is a design parameter and it can be set to any value. When n is an integer, the impedance of the parallel-tuned circuit $C_n//L_n$ is infinite at the frequency $n\omega$ and zero otherwise. Especially this new configuration open circuits the second harmonic which is similar to the inverse class F amplifier when $n = 2$, and open circuits the third harmonic that is similar to the class F amplifier when $n = 3$. Thus, the modified class E amplifier proposed in this paper exhibits different performance with design parameter n varies.

The analysis of the circuit is based on the following assumptions that are proposed by the previous literature [15]: (i) The transistor is modeled as an ideal switch; the switching action of the transistor is instantaneous and lossless. (ii) The switch duty cycle is 50%. (iii) The RF choke (RFC) has an infinite inductance; The DC block has an infinite capacitance. (iv) The factor Q_L of the parallel LC resonator is high enough so that the output voltage is essentially sinusoidal at the carrier frequency.

A) Switch current and voltage steady-state waveforms

According to the assumptions above, the output voltage and the output current are sinusoidal and are defined as

$$v_o(\theta) = V_{DC} a \sin(\theta + \varphi), \tag{1}$$

$$i_o(\theta) = V_{DC} a \sin(\theta + \varphi)/R_L, \tag{2}$$

where $\theta = \omega t$, $\omega = 2\pi f_o$ (f_o is the fundamental frequency), the switch is closed when $0 \le \theta < \pi$; and the switch is opened when $\pi \le \theta \le 2\pi$. V_{DC} is a DC input voltage, φ is the phase angle of the output signal, and R_L is the load resistance. Parameters a and φ are to be determined. From Fig. 1, according to the KVL law $v_1(\theta)$ can be expressed as

$$v_1(\theta) = V_{DC} - v_o(\theta) - v_2(\theta), \quad 0 \le \theta \le 2\pi. \tag{3}$$

And then, the steady-state switch current and voltage waveforms can be expressed as

$$i_s(\theta) = \begin{cases} \dfrac{1}{\omega L}\displaystyle\int_0^\theta v_1(\theta)\, d\theta, & 0 \le \theta < \pi, \\ 0, & \pi \le \theta \le 2\pi, \end{cases} \tag{4}$$

$$v_s(\theta) = \begin{cases} 0, & 0 \le \theta < \pi, \\ v_1(\theta), & \pi \le \theta \le 2\pi. \end{cases} \tag{5}$$

According to the KCL law, the current through switch $i_s(\theta)$ can be rewritten as

$$i_s(\theta) = I_{DC} + i_2(\theta), \quad 0 \le \theta \le 2\pi \tag{6}$$

and the current $i_2(\theta)$ flowing through the parallel resonant tank $C_n//L_n$ can be expressed as

$$i_2(\theta) = \frac{1}{\omega L_n}\int_0^\theta v_2(\theta)\, d\theta + C_n \omega \frac{dv_2(\theta)}{d\theta}. \tag{7}$$

Hence, when the switch is ON ($0 \le \theta < \pi$), from (4), (6) and (7), we obtain

$$I_{DC} + \frac{1}{\omega L_n}\int_0^\theta v_2(\theta)\, d\theta + C_n \omega \frac{dv_2(\theta)}{d\theta} = \frac{1}{\omega L}\int_0^\theta v_1(\theta)\, d\theta. \tag{8}$$

Equation (8) can be represented in the form of the second-order differential equation given by

$$\omega C_n v_2''(\theta) + \frac{1}{\omega L_n} v_2(\theta) = \frac{1}{\omega L} v_1(\theta). \tag{9}$$

Substituting (3) into (9), results in

$$v_1''(\theta) + \left(n^2 + \frac{1}{\omega^2 L C_n}\right) v_1(\theta) = n^2 V_{DC} - (n^2 - 1) v_o(\theta), \tag{10}$$

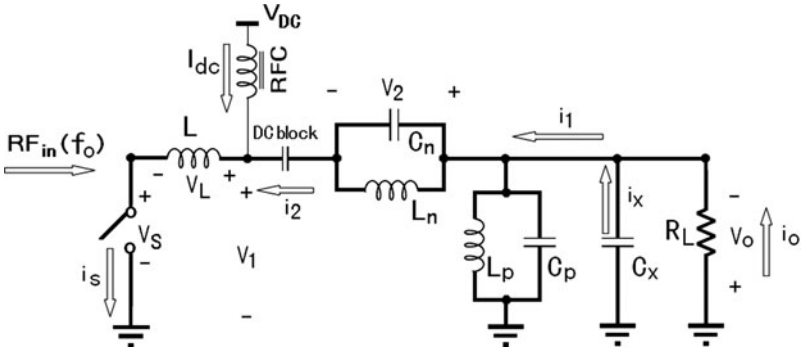

Fig. 1. The circuit schematic diagram of the proposed inverse class E amplifier with series tunable parallel resonant tank.

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the general solution of which can be obtained by

$$v_1(\theta) = A_1 \cos(\beta\theta) + A_2 \sin(\beta\theta) + n^2 V_{DC}/\beta^2 - aV_{DC}(n^2-1)\sin(\theta+\varphi)/(\beta^2-1), \quad (11)$$

where $0 \le \theta < \pi$, $\beta = \sqrt{n^2 + (1/\omega^2 LC_n)}$, and coefficients A_1, A_2 are yet to be determined.

Under the initial condition $i_s(0) = 0$, substituting (11) into (4), the steady-state switch current waveform is then given by

$$i_s(\theta) = \begin{cases} \frac{1}{\omega L}\left[A_1\frac{\sin(\beta\theta)}{\beta} - A_2\frac{\cos(\beta\theta)-1}{\beta} + \frac{n^2 V_{DC}\theta}{\beta^2} + \frac{aV_{DC}(\cos(\theta+\varphi)-\cos\varphi)(n^2-1)}{\beta^2-1}\right], & 0 \le \theta < \pi, \\ 0, & \pi \le \theta \le 2\pi. \end{cases} \quad (12)$$

When the switch is OFF ($\pi \le \theta \le 2\pi$), according to the KCL law $i_2(\theta) + I_{DC} = 0$, we obtain

$$I_{DC} + \frac{1}{\omega L_n}\int_{\pi}^{\theta} v_2(\theta)\, d\theta + C_n\omega\frac{dv_2(\theta)}{d\theta} = 0. \quad (13)$$

Equation (13) can be represented in the form of the second-order differential equation given by

$$\omega C_n v_2''(\theta) + \frac{1}{\omega L_n} v_2(\theta) = 0. \quad (14)$$

Substituting (3) into (14), results in

$$v_1''(\theta) + n^2 v_1(\theta) = n^2 V_{DC} - a(n^2-1)V_{DC}\sin(\theta+\varphi), \quad (15)$$

which general solution can be obtained by

$$v_1(\theta) = A_1' \cos(n\theta) + A_2' \sin(n\theta) + V_{DC} - aV_{DC}\sin(\theta+\varphi), \quad (16)$$

where $\pi \le \theta \le 2\pi$, and coefficients A_1', A_2' are yet to be determined. Substituting (16) into (5), the steady-state switch voltage waveform is then given by

$$v_s(\theta) = \begin{cases} 0, & 0 \le \theta < \pi, \\ A_1' \cos(n\theta) + A_2' \sin(n\theta) + V_{DC} - aV_{DC}\sin(\theta+\varphi), & \pi \le \theta \le 2\pi. \end{cases} \quad (17)$$

In summary, the switch current and voltage steady-state waveforms can be obtained from (12) and (17), respectively. And all the unknown parameters in these expressions will be calculated in the following analysis.

B) ZCS conditions of inverse class E power amplifier

For the lossless operation mode, it is necessary to provide optimum conditions to eliminate power losses of the transistor. The zero-current switching and zero-current slope switching conditions ($i_s(\pi) = 0$; $i_s'(\pi) = 0$) should be fulfilled. As a result, we obtain two equations:

$$A_1 \sin(\beta\pi) - A_2[\cos(\beta\pi) - 1] + \frac{n^2 V_{DC}\pi}{\beta} - \frac{2a\beta V_{DC}(n^2-1)\cos\varphi}{(\beta^2-1)} = 0, \quad (18)$$

$$A_1 \cos(\beta\pi) + A_2 \sin(\beta\pi) + \frac{n^2 V_{DC}}{\beta^2} + \frac{aV_{DC}(n^2-1)\sin\varphi}{(\beta^2-1)} = 0. \quad (19)$$

Combining (18) and (19), A_1 and A_2 can be expressed as two equations with three unknown parameters (a, β, φ):

$$A_2 = \frac{n^2 V_{DC}[\sin(\beta\pi) - \pi\beta\cos(\beta\pi)]}{\beta^2[\cos(\beta\pi) - 1]} + \frac{aV_{DC}(n^2-1)[\sin\varphi\sin(\beta\pi) + 2\beta\cos\varphi\cos(\beta\pi)]}{(\beta^2-1)[\cos(\beta\pi) - 1]}, \quad (20)$$

$$A_1 = \frac{A_2[\cos(\beta\pi) - 1]}{\sin(\beta\pi)} - \frac{n^2 V_{DC}\pi}{\beta\sin(\beta\pi)} + \frac{2a\beta V_{DC}(n^2-1)\cos\varphi}{(\beta^2-1)\sin(\beta\pi)}. \quad (21)$$

C) The continuity of the capacitance voltage and inductance current

The energy stored in capacitance or inductance cannot change instantly, and hence the voltage across the C_n or the current through the L_n is continuous. According to the continuity of the capacitance voltage and inductance current, we obtain some other boundary conditions besides the ZCS conditions.

Since the voltage $v_2(\theta)$ across the C_n is continuous, $v_1(\theta)$ is also continuous. From zero-current slope switching condition ($i_s'(\pi) = 0$) and the continuity of $v_1(\theta)$, we obtain $v_1(\pi) = 0$, then combine it and (16), results in

$$A_1' \cos(n\pi) + A_2' \sin(n\pi) + V_{DC} + aV_{DC}\sin\varphi = 0. \quad (22)$$

When $\theta = \pi$, equation (13) can be written as $\omega C_n v_2'(\pi) + I_{DC} = 0$, then substituting (3) and (17) into it, we obtain

$$A_1' \sin(n\pi) - A_2' \cos(n\pi) = -I_{DC}/(n\omega C_n). \quad (23)$$

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From (22) and (23), A_1' and A_2' can be expressed as two equations with three unknown parameters (a, β, φ):

$$A_1' = \frac{-I_{DC}\sin(n\pi)}{n\omega C_n} - V_{DC}(1 + a\sin\varphi)\cos(n\pi), \tag{24}$$

$$A_2' = \frac{I_{DC}\cos(n\pi)}{n\omega C_n} - V_{DC}(1 + a\sin\varphi)\sin(n\pi). \tag{25}$$

There is another equation $v_1(0) = v_1(2\pi)$ since the voltage $v_2(\theta)$ across the C_n is continuous. Combine it and (16), results in

$$\begin{aligned} A_1 + \frac{n^2 V_{DC}}{\beta^2} - \frac{aV_{DC}(n^2-1)\sin\varphi}{\beta^2 - 1} &= \frac{I_{DC}\sin(n\pi)}{n\omega C_n} \\ - V_{DC}(1 + a\sin\varphi)\cos(n\pi) &+ V_{DC}(1 - a\sin\varphi). \end{aligned} \tag{26}$$

In addition, it is necessary to consider the continuity of current $i_{Ln}(\theta)$ through the L_n to determine all the unknown parameters. The expression of $i_{Ln}(\theta)$ during a whole cycle ($0 \le \theta \le 2\pi$) is given by

$$i_{L_n}(\theta) = \begin{cases} \dfrac{1}{\omega L_n}\displaystyle\int_0^{\theta} \begin{bmatrix} -A_1\cos(\beta\theta) - A_2\sin(\beta\theta) \\ +\dfrac{(\beta^2 - n^2)V_{DC}}{\beta^2} \\ +\dfrac{aV_{dc}(n^2-\beta^2)\sin(\theta+\varphi)}{(\beta^2-1)} \end{bmatrix} d\theta, & 0 \le \theta < \pi, \\ \dfrac{1}{\omega L_n}\displaystyle\int_{\pi}^{\theta} \begin{bmatrix} -A_1'\cos(n\theta) \\ -A_2'\sin(n\theta) \end{bmatrix} d\theta, & \pi \le \theta \le 2\pi. \end{cases} \tag{27}$$

According to the circuit initial condition and the continuity of current $i_{Ln}(\theta)$, we obtain $i_{Ln}(2\pi) = i_{Ln}(0) = 0$, and then (27) can be rewritten as

$$i_{L_n}(\theta) = \begin{cases} \dfrac{1}{\omega L_n}\left\{ \begin{array}{l} -A_1\dfrac{\sin(\beta\theta)}{\beta} + A_2\dfrac{\cos(\beta\theta)-1}{\beta} \\ +\dfrac{(\beta^2-n^2)V_{DC}\theta}{\beta^2} \\ +\dfrac{aV_{dc}(\beta^2-n^2)[\cos(\theta+\varphi)-\cos\varphi]}{(\beta^2-1)} \end{array} \right\}, & 0 \le \theta < \pi, \\ \dfrac{1}{\omega L_n}\begin{bmatrix} A_1'\dfrac{\sin(2n\pi)-\sin(n\theta)}{n} \\ +A_2'\dfrac{\cos(n\theta)-\cos(2n\pi)}{n} \end{bmatrix}, & \pi \le \theta \le 2\pi. \end{cases} \tag{28}$$

Considering that the current $i_{Ln}(\theta)$ is continuous when $\theta = \pi$, and then combining (24), (25), and (28), we obtain

$$\begin{aligned} &-A_1\frac{\sin(\beta\pi)}{\beta} + A_2\frac{\cos(\beta\pi)-1}{\beta} + \frac{(\beta^2-n^2)V_{DC}\pi}{\beta^2} \\ &-\frac{2aV_{dc}(\beta^2-n^2)\cos\varphi}{(\beta^2-1)} \\ &= \frac{I_{DC}(1-\cos(n\pi))}{\omega n^2 C_n} - \frac{V_{DC}(1+a\sin\varphi)\sin(n\pi)}{n}. \end{aligned} \tag{29}$$

D) Fourier series of switch current $i_s(\theta)$

In the time domain the switch current $i_s(\theta)$ can be expressed in the form of a Fourier series as follows:

$$i_s(\theta) = I_{DC} + \sum_{n=1}^{\infty}\{a_{in}[\cos(n\theta+\varphi)] + b_{in}[\sin(n\theta+\varphi)]\}. \tag{30}$$

The DC current I_{DC} can be expressed as

$$I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i_s(\theta)\,d\theta = \frac{1}{2\pi}\int_0^{\pi} i_s(\theta)\,d\theta = \frac{V_{DC}}{2\pi\omega L}U, \tag{31}$$

where U is the expression consists of five unknown parameters a, β, φ, A_1, A_2. The fundamental frequency current $i_1(\theta)$ flowing through the switch consists of two components

$$i_1(\theta) = a_{i1}\cos(\theta+\varphi) + b_{i1}\sin(\theta+\varphi), \tag{32}$$

where a_{i1} and b_{i1} are defined as

$$a_{i1} = \frac{1}{\pi}\int_0^{\pi} i_s(\theta)\cos(\theta+\varphi)\,d\theta = \frac{V_{DC}}{\pi\omega L}E, \tag{33}$$

$$b_{i1} = \frac{1}{\pi}\int_0^{\pi} i_s(\theta)\sin(\theta+\varphi)\,d\theta = \frac{V_{DC}}{\pi\omega L}F, \tag{34}$$

where E, F are also the expressions consist of five unknown parameters a, β, φ, A_1, A_2. According the KCL law, we can write

$$\begin{aligned} i_1(\theta) = i_x(\theta) + i_o(\theta) &= \omega C_x a V_{DC}\cos(\theta+\varphi) \\ &+ aV_{DC}\sin(\theta+\varphi)/R_L, \end{aligned} \tag{35}$$

then from (32)–(35) we obtain

$$a_{i1} = EV_{DC}/(\pi\omega L) = \omega C_x a V_{DC}, \tag{36}$$

$$b_{i1} = FV_{DC}/(\pi\omega L) = aV_{DC}/R_L. \tag{37}$$

The drain efficiency of an ideal inverse class E power amplifier is 100%, hence $V_{DC}I_{DC} = a^2V_{DC}^2/(2R_L)$, then we write R_L as follows:

$$R_L = a^2 V_{DC}/(2I_{DC}). \tag{38}$$

From the analysis proposed above, we obtain enough equations to solve all the unknown parameters.

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E) Design equations of circuit components

By combining (20), (21), (26), and (31), the first equation can be simply written as follows: $\phi_1(a, \beta, \varphi) = 0$, where $\phi_1(a, \beta, \varphi)$ can be expressed as

$$\begin{aligned}\phi_1(a,\beta,\varphi) = {} & aV_{DC}\sin\varphi\frac{n^2-1}{\beta^2-1} - \frac{n^2V_{DC}}{\beta^2} \\ & - \frac{V_{DC}U(\beta^2-n^2)}{2\pi n}\sin(n\pi) \\ & - V_{DC}(1+a\sin\varphi)\cos(n\pi) \\ & + V_{DC}(1-a\sin\varphi) - A_1.\end{aligned} \tag{39}$$

By combining (20), (21), (29), and (31), the second equation can be written as $\phi_2(a, \beta, \varphi) = 0$, where $\phi_2(a, \beta, \varphi)$ can be expressed as

$$\begin{aligned}\phi_2(a,\beta,\varphi) = {} & -A_1\frac{\sin(\beta\pi)}{\beta} + A_2\frac{\cos(\beta\pi)-1}{\beta} \\ & + \frac{(\beta^2-n^2)V_{DC}\pi}{\beta^2} - \frac{2aV_{DC}(\beta^2-n^2)\cos\varphi}{(\beta^2-1)} \\ & - \frac{\beta^2-n^2}{2\pi n^2}V_{DC}U(1-\cos(n\pi)) \\ & + \frac{V_{DC}(1+a\sin\varphi)\sin(n\pi)}{n}.\end{aligned} \tag{40}$$

From (20), (21), (31), (37), and (38), we obtain the third equation $\phi_3(a, \beta, \varphi) = 0$, where $\phi_3(a, \beta, \varphi)$ can be expressed as

$$\phi_3(a,\beta,\varphi) = U - aF. \tag{41}$$

Table 1. The numeric results of important parameters for calculate components values.

	$n=2$	$n=3$	$n=4$	$n=5$
a	1.61294	1.96954	1.69386	1.90201
β	2.45412	3.36359	5.12841	5.29696
φ (rad)	−0.22909	−0.71363	−0.38354	−0.63446
E	1.00952	1.22692	0.45903	1.22129
F	1.90675	1.01546	0.47438	1.05152
U	2.62054	2	0.80353	2

The three unknown parameters a, β, and φ can be determined by solving these three equations, and then the expressions E, U, F consisting of parameters a, β, φ can be calculated. Whereas the final expressions of the three parameters are very complicated, it is not convenient to get the explicit expressions. The values of these parameters will be given in the following analysis through numerical calculation.

When designing a power amplifier we require a specific output power P_o, for a given DC voltage V_{DC} at a specified operating frequency f_o. The optimum component values for the specified output power and DC voltage can be calculated from these equations as follows:

$$R_L = a^2V_{DC}^2/(2P_o), \tag{42}$$

$$L = UV_{DC}^2/(2\pi\omega P_o), \tag{43}$$

$$C = 1/(\omega^2\beta^2 L), \tag{44}$$

$$C_x = 2EP_o/(aU\omega V_{DC}^2). \tag{45}$$

The values of L_p and C_p of the parallel resonant circuit depending on the chosen in advance loaded quality factor

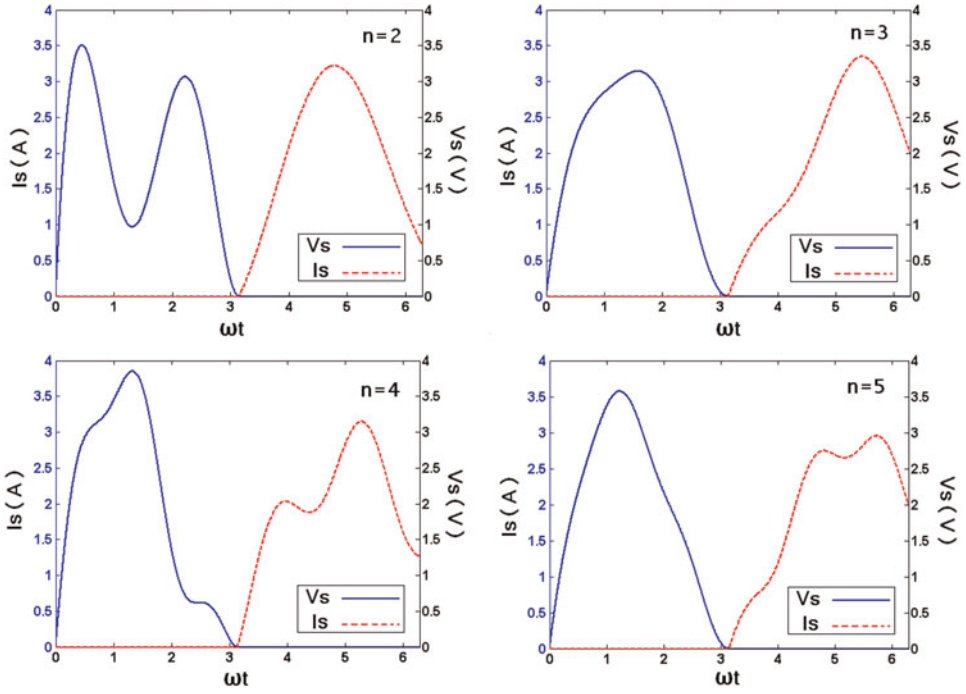

Fig. 2. The ideal drain voltage and current waveforms of the amplifier with n varies.

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Table 2. Peak drain voltage and current, power output capability of the amplifier with n varies.

	n=2	n = 3	n = 4	n = 5
v_{smax}	$3.214V_{DC}$	$3.348V_{DC}$	$3.153V_{DC}$	$2.954V_{DC}$
i_{smax}	$3.510I_{DC}$	$3.142I_{DC}$	$3.841I_{DC}$	$3.574I_{DC}$
C_{Pout}	0.089	0.095	0.083	0.095

Q_L, whose value should be as high as possible, are calculated by

$$C_p = Q_L/(\omega R_L), \tag{46}$$

$$L_p = 1/(\omega^2 C_p). \tag{47}$$

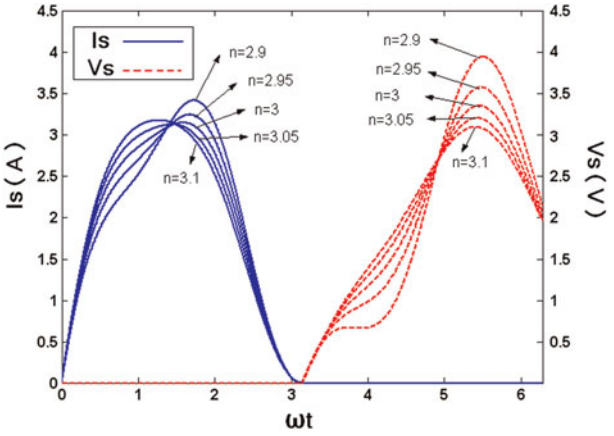

Fig. 3. Ideal drain voltage and current waveforms of the amplifier when n is swept from 2.9 to 3.1.

III. AMPLIFIER PERFORMANCE STUDY WITH PARAMETER N VARIATIONS

The resonance frequency of the parallel resonant tank $C_n//L_n$ is $n\omega$, where n is a design parameter as mentioned above. The amplifier demonstrates varying peak drain voltage and current waveforms and different power output capability when the parallel resonant is tuned to a different frequency.

According to the analysis proposed in Section II, all the values of load network circuit components and performance of the modified class E amplifier can be obtained through numeric simulations. Table 1 shows the numeric results of important parameters for calculated circuit components with different n values. The ideal drain voltage and current waveforms of the amplifier with n varies are presented in Fig. 2, the amplifier performance such as the peak drain voltage and current, power output capability are shown in Table 2.

Obviously, the power output capability decreases and the drain voltage and current waveforms distort when the parameter n is even, and so it is not a good choice to construct a hybrid combining features of inverse class E and inverse class F. The reason is that theoretic inverse class F amplifier presents discontinuous drain current at the switching events which is incompatible with the ZCS conditions. Whereas incorporating traits of inverse class E and class F is a reasonable scheme. Table 2 shows that when n is odd the power output capability of the modified amplifier is slightly less than the classical class E and inverse class E mode. Especially when $n = 3$, the amplifier can be regarded as a realization of class F_3/E mode, which is a hybrid of third-harmonic peaking class F [19] and inverse class E. It displays lower peak drain voltage comparing to the classical class E and lower peak drain current comparing to the classical inverse class E.

Further analysis shows that the amplifier obtains some improvement when n is a non-integer near 3. The ideal drain voltage and current waveforms of the amplifier when n is swept from 2.9 to 3.1 are presented in Fig. 3. It demonstrates varying degrees of trade-off between the peak drain voltage and current when parameter n is set to different value. Figure 4 shows the power output capability of the amplifier versus parameter n. The maximum value of power output capability is 0.1022, which is obtained when $n = 3.11$. Finally, we let $n = 3.1$ and carry out an experiment based on the theoretical analysis above. Table 3 shows comparison of the proposed amplifier and class E and inverse class E.

The proposed amplifier not only maintains the zero power loss switching operation, but also brings in some improvements as follows:

First, when DC supply voltage and load resistance are fixed, the modified amplifier obtains the highest output voltage V_o and output power P_o.

Second, the power output capability C_{Pout} of the new configuration gets an increase of 4.1% comparing to the standard class E or inverse class E amplifier.

In addition, the new topology achieves more desirable drain voltage and current waveforms. The peak drain voltage for nominal class E operation is $3.562V_{DC}$, whereas for inverse class E amplifier the value is $2.862V_{DC}$. As a dual of class E topology, inverse class E amplifier has lower peak drain voltage; nevertheless, it brings high peak drain current whose value is $3.562I_{DC}$. When the parallel resonant tank is introduced to the invrese class E topology, the peak drain current decreases to $3.170I_{DC}$, and the peak drain voltage is $3.090V_{DC}$ that is also much lower than the peak drain voltage vlaue of classical class E amplifier. This relaxes the

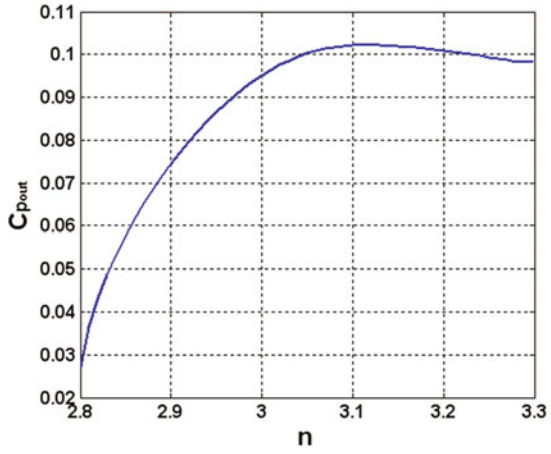

Fig. 4. The power output capability of the amplifier versus parameter n.

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Table 3. Comparison of the proposed amplifier and class E and inverse class E.

	This work (n=3.1)	Inverse class E	Class E
R_L	$1.795V_{DC}^2/P_o$	$1.734V_{DC}^2/P_o$	$0.577V_{DC}^2/P_o$
L	$0.305V_{DC}^2/(\omega P_o)$	$0.318V_{DC}^2/(\omega P_o)$	$0.665V_{DC}^2/(\omega P_o)$
C_x	$0.636P_o/(\omega V_{DC}^2)$	$0.665P_o/(\omega V_{DC}^2)$	$0.318P_o/(\omega V_{DC}^2)$
L_n	$0.170L$	/	/
C_n	$0.104/\omega^2 L_n$	/	/
C_p	$Q_L/\omega R_L$	$Q_L/\omega R_L$	$Q_L/\omega R_L$
L_p	$1/\omega^2 C_p$	$1/\omega^2 C_p$	$1/\omega^2 C_p$
V_o	$1.895V_{DC}$	$1.862V_{DC}$	$1.074V_{DC}$
I_o	$1.055I_{DC}$	$1.074I_{DC}$	$1.862I_{DC}$
P_o	$1.795V_{DC}^2/R_L$	$1.734V_{DC}^2/R_L$	$0.577V_{DC}^2/R_L$
φ	-0.634(rad)	-0.567(rad)	-0.567(rad)
v_{smax}	$3.090V_{DC}$	$2.862V_{DC}$	$3.562V_{DC}$
i_{smax}	$3.170I_{DC}$	$3.562I_{DC}$	$2.862I_{DC}$
C_{Pout}	0.102	0.098	0.098

design requirement on the transistor and is greatly beneficial to the device safety.

IV. SIMULATIONS AND EXPERIMENTS

To confirm the theoretical analysis and synthesis explained in Sections II and III, harmonic balance simulations have been carried out within Agilent Advanced Design Systems (ADS) suite. In these experiments, let $n = 3.1$ and then all the values of load network components can be calculated as introduced in Section III. Here the transistor used is MRF21010 manufactured by Freescale Corporation, whose physics-based Root model is available in the ADS library. Although the transistor MRF21010 is able to operate at 2GHz, its switching action deteriorates heavily because of the effects of parasitic components. In order to verify the practical performance of the proposed circuits, the power amplifier is built in low frequency (155 MHz), and then the device can be modeled as a switch approximately. From the above analysis the load network circuits can be fixed and then using the source-pull method we can obtain the optimal source impedance which is suitable for design input matching circuit.

Figure 5 shows the simulated drain voltage/current waveforms of the class E power amplifier proposed in this paper.

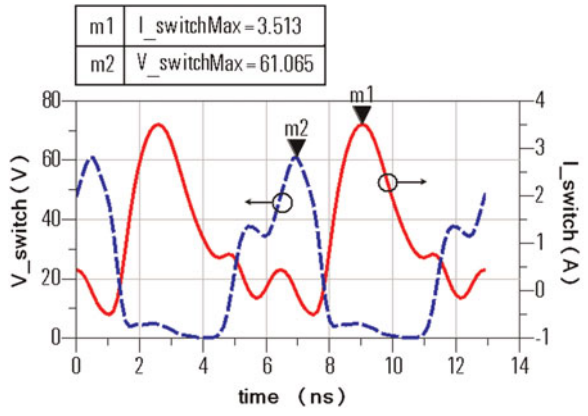

Fig. 5. The simulated drain voltage/current waveforms (DC voltage is 21 V, output power is 10 W, and work frequency is 155 MHz).

The amplifier obtaining an output power 40 dBm at 155 MHz (DC voltage is 21 V and DC current is 1.12 A). It can be observed that the peak drain voltage and current are about 61 V and 3.5A, respectively. These values show the agreement with theoretical analysis. The waveforms in Fig. 5 are distorted lightly when compared to the idealized waveforms in Fig. 3. This is mainly due to the effects of some internal transistor parasitics and non-ideal switching action. There exist many factors that can degrade the amplifier performance. For example, the on resistance of a transistor can cause notable efficiency degradation because it consumes

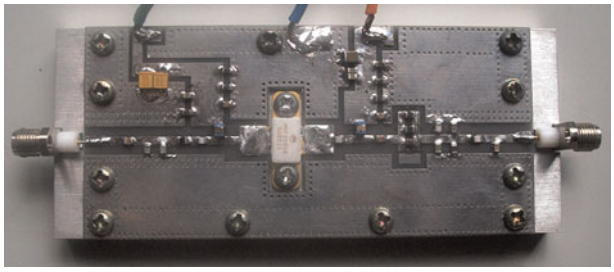

Fig. 6. The schematic and photo of the test board.

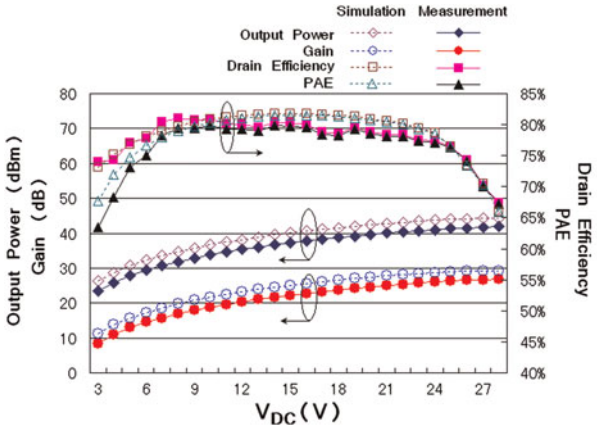

Fig. 7. The output power, gain, drain efficiency, and PAE of the simulations and the measurements versus DC supply voltage ($P_{in} = 15$ dBm, $f =$ 155 MHz, $V_{GS} = 4.2$ V).

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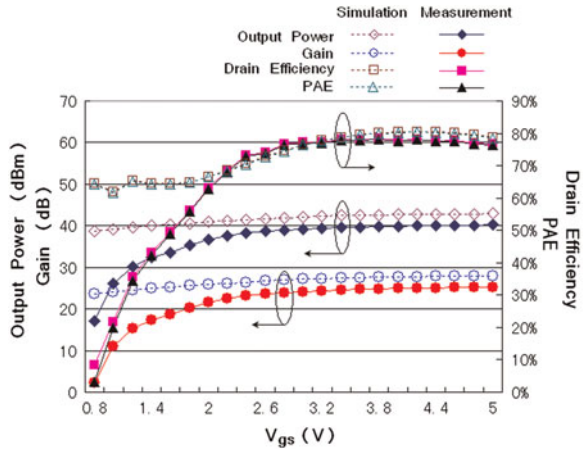

Fig. 8. The output power, gain, drain efficiency, and PAE of the simulations and the measurements versus gate–source voltage ($P_{in} = 15$ dBm, $f =$ 155 MHz, $V_{DC} = 21$ V).

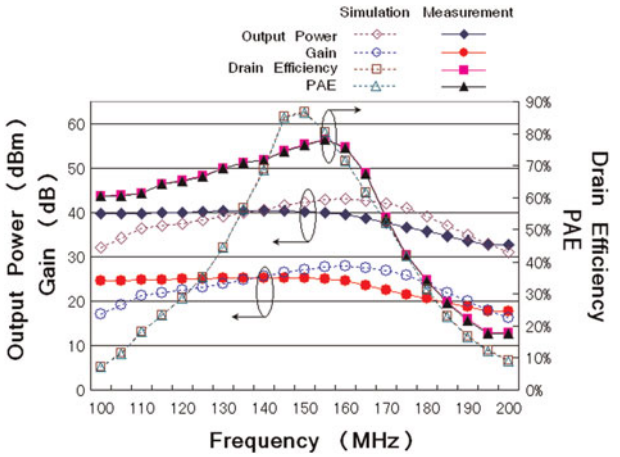

Fig. 10. The output power, gain, drain efficiency, and PAE of the simulations and the measurements versus operating frequency ($V_{GS} = 4.2$ V, $V_{DC} = 21$ V, $P_{in} = 15$ dBm).

power during the on state. Whereas, at the microwave band, the effects of parasitic components such as output capacitance and lead inductance become notable. The distorted drain voltage/current waveforms which caused by parasitics will degrade the perormance and security of the PA. As a result, excellent switching device (such as GaN HEMT) should be utilizing when design frequency moves toward microwave operation. The schematic and photo of the experiment circuits are shown in Fig. 6. The simulation and measurement results are presented as follows.

Figure 7 depicts the output power, gain, drain efficiency, and power-added efficiency (PAE) of the simulations and the measurements versus DC supply voltage. It can be seen from Fig. 7 that the maximum simulated drain efficiency and PAE are 81.74 and 81.51%, and the maximum measured drain efficiency and PAE are 81.04 and 79.82%. Here, drain efficiency >75% for DC supply voltage ranges from 5 to 25 V is obtained. Obviously, the measured results agree well with the simulation. This implies that the output power can be well-controlled through direct variation of the DC supply voltage without unduly impairing efficiency.

Figure 8 shows the plot of output power, gain, drain efficiency, and PAE of the simulations and the measurements versus gate–source voltage. Because the used device Root model is not exactly the same with the practical transistor especially in the modeling of gate–source characteristics, the measured output power and drain efficiency are much lower than the simulated results when the gate–source bias voltage <2 V.

The output power, gain, drain efficiency, and PAE of the simulations and the measurements versus input power are illustrated in Fig. 9. Comparing measured results with simulated results, the excellent agreement was obtained. The output power rises with the increasing input power, and it goes into saturation area when the input power is high enough. Thus, the amplifier needs proper level of the input power to obtain the optimal performance.

The amplifier performance as a function of operating frequency is presented in Fig. 10. It can be seen that when the operating frequency is swept from 135 to165 MHz, the output power ranges from 39.58 to 40.31 dBm and the drain efficiency ranges from 71.03 to 78.24%. This amplifier can maintain its high efficiency and output power in the relative bandwidth about 20% (i.e. 30 MHz).

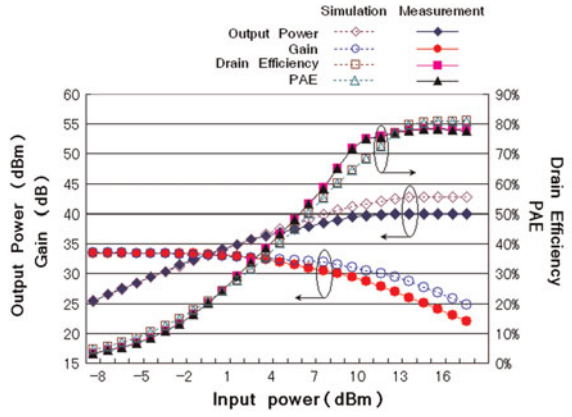

Fig. 9. The output power, gain, drain efficiency, and PAE of the simulations and the measurements versus input power ($V_{GS} = 4.2$ V, $V_{DC} = 21$ V, $f =$ 155 MHz).

V. CONCLUSIONS

A modified inverse class E power amplifier with series tunable parallel resonant tank has been analyzed in this paper. The theoretical principles and design equations required to calculate the optimum circuit component values were given in detail. The proposed amplifier not only maintains 100% efficiency theoretically, but also brings in some improvements such as higher output power, power output capability, and further relaxes design requirements. The practical circuit implemented delivers 40.02 dBm output power at 155 MHz, and achieved PAE of 78.18%, drain efficiency of 78.42%, and 25.02 dB power gain when operated from a 21 V supply voltage. Experimental results show excellent agreement with simulations, which verifies the theoretical analysis. And the manufacture of this mode power amplifier with transmission-line load network at C-band will be the next work in future.

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