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RESEARCH PAPER

# A 120 GHz FMCW radar frontend demonstrator based on a SiGe chipset

MARTIN JAHN AND ANDREAS STELZER

*This paper presents a frequency-modulated continuous-wave (FMCW) radar operating at 120 GHz, which features silicon–germanium (SiGe) chips that employ HBTs with 320 GHz $f_{max}$. The chipset comprises a fundamental-wave signal-generation chip with a voltage-controlled oscillator (VCO) that provides frequencies between 114 and 130 GHz and a corresponding dual–transceiver (TRX) chip that supports monostatic and quasi-monostatic radar configurations. The cascode amplifiers used in the TRX chip were characterized in separate test chips and yielded peak small-signal gains of approximately 15 dB. Finally, a quasi-monostatic two-channel FMCW radar frontend with on-board differential microstrip antennas was built on an RF substrate. FMCW radar measurements with frequency chirps from 116 to 123 GHz verified the functionality of the designed radar sensor.*

**Keywords:** Circuit design and application, Radar application, Frequency-modulated continuous wave

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## I. INTRODUCTION

In both science and industry, a clear trend toward higher operating frequencies in silicon-based technologies can be noticed (e. g., [1]). Millimeter-wave circuits for applications such as wireless data transmission at 60 GHz and radar sensors operating at 77 GHz have become state–of–the–art and integrated circuits for frequency bands above 100 GHz have already been presented [2–6]. Distinct advantages of silicon technologies such as high integration density, low cost, and packaging capability make them appealing candidates for future millimeter-wave consumer market products. Nevertheless, the performance progress made – especially in SiGe technology, where unity gain transition frequencies $f_T$ around 300 GHz and a maximum oscillation frequency $f_{max}$ of 500 GHz have recently been demonstrated [7] – can pave the way for applications operating within reasonable design margins above 100 GHz. One of the next bands of interest is located at 122 GHz, where an industrial, scientific, and medical (ISM) radio band with 1 GHz bandwidth has been allocated.

In this paper, we present a frequency-modulated continuous-wave (FMCW) radar sensor with two channels built on a circuit board and employs customized silicon–germanium (SiGe) based monolithic microwave–integrated circuits. The final demonstrator produces chirps from 116 to 123 GHz in the measurement setup.

Johannes Kepler University Linz, Altenberger Str. 69, 4040 Linz, Austria. Phone: +43 732 2468
**Corresponding author:**
M. Jahn
Email: m.jahn@nthfs.jku.at

## II. CIRCUIT DESIGN

The 120 GHz chipset comprises a signal-generation chip and a dual–transceiver (TRX) chip. The signal-generation chip includes a voltage-controlled oscillator (VCO) with fine-and coarse-tuning capability, an output buffer, and a prescaler with a total division ratio of eight. A similar topology can be found in [2]. The block diagram of the TRX die is depicted in Fig. 1. It includes two TRX cells: the first cell features a single TRX port and favors the monostatic radar configuration which uses a single antenna for transmit (TX) and receive(RX); therefore, a duplexer (Rat-race coupler) was introduced to separate signals into TX and RX. The second TRX cell deploys separate TX and RX channels, and favors a radar architecture with separate TX and RX antennas. If the distance between the antennas is of the order of the wavelength the setup is said to be quasi-monostatic. If the TX and RX antennas are located at different positions and the distance in between is very large compared to the wavelength, the configuration is referred to as bistatic (used, e. g., in military applications and weather radar). Obviously, there is no need for a duplexer in the quasi-monostatic approach, since the TX and RX signals are separated by different antennas. For this reason, higher output power, improved RX gain, and lower RX noise figure (NF) can be observed compared to the monostatic approach, where the duplexer leads to a degradation of the aforementioned figures (≈4.5 dB, cf. [2]). Furthermore, the quasi-monostatic approach can mitigatethe dc-offset problem in zero-IF receivers, which originates from TX leakage, strong reflections of mismatched interfaces such as bond–wire transitions, and antenna mismatch [8].

All circuits are fully differential and run on a 3.3 V power supply. The SiGe technology employed for chip fabrication features HBTs with an $f_T$, an $f_{max}$, and a ring-oscillator gate

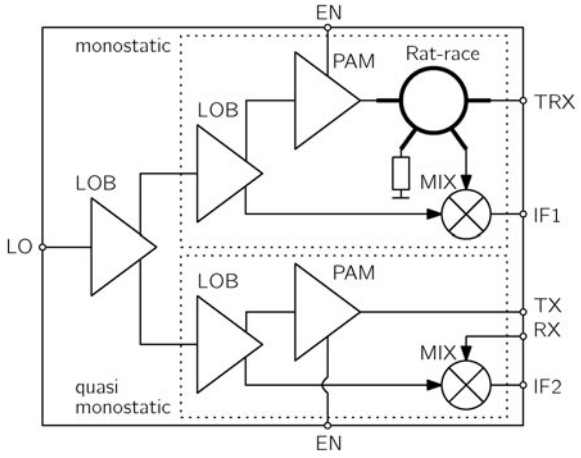



**Fig. 1.** Block diagram of the integrated dual TRX chip. It comprises two slightly different TRX cells that favor monostatic and quasi-monostatic radar configurations, respectively. The building blocks are indicated by abbreviations, where LOB, PAM, and MIX denote the LO buffer, power amplifier, and mixer, respectively.

delay $\tau_D$ of approximately 225 GHz, 320 GHz, and 2.7 ps, respectively. Fig. 2 shows microphotographs of the signal-generation chip and the dual–TRX chip with labeled building blocks. The die sizes are $728 \times 728\ \mu m^2$ and $1028 \times 1128\ \mu m^2$, respectively.

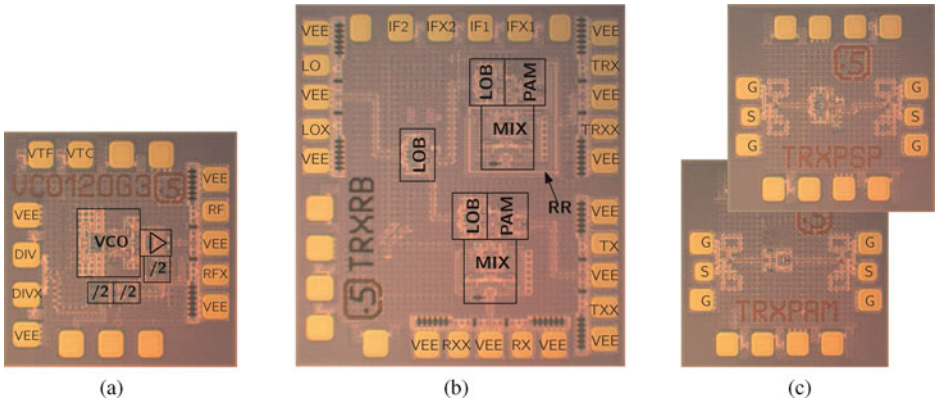
## A) Signal-generation chip

A detailed description of the employed signal-generation chip can be found in [9]. The fundamental-wave VCO is based on a negative resistance topology and uses an additional capacitive cross-coupling. It covers a frequency span of 16 GHz at a center frequency of 122 GHz, and the tuning voltage ranges from 1.5 to 9 V (fine- and coarse-tuning tied together). The chip exhibits an average phase noise of −95 dBc/Hz at 1 MHz offset frequency over the whole tuning range. The output power measured at the buffer was around 0 dBm. In order to minimize load pulling effects, an output buffer was connected to the output of the VCO. A cascode topology was favored over an emitter follower stage because the latter is prone to becoming instable. Moreover, a cascode stage provides better isolation, which is desired. The buffer is matched to a differential input impedance of 50 Ω and to 70 Ω at the output. The three-stage prescaler consists of two regenerative dividers in the first stages and a third static divider in the last stage. Regenerative dividers were chosen as first stages, because they achieve higher operating frequencies compared to static dividers.

## B) Dual-transceiver chip

The LO buffer in the TRX chip (cf. Figs 1 and 2) is based on the circuit shown in [10] and draws 25 mA. It was matched to a differential impedance of 70 Ω at the input and to 35 Ω at the output in order to allow connection of two 70 Ω transmission lines in parallel. The first LO buffer in the TRX circuitry compensates for losses due to interconnections, such as bond–wire transitions and tracks, and distributes the LO signal to the downstream TRX cells, where the LO buffers operate already in compression, that is, they work as limiters in order to supply the mixers with a constant LO drive. Fig. 3 (a) shows the measured single-ended S-parameters of the LO buffer test chip, which is shown in Fig. 2 (c). It uses LC-baluns at the input and output ports to perform the single-ended to differential conversion. Additionally, one branch of the buffer output was terminated by a resistor in order to employ the same baluns at the input and output. The desired center frequency of 125 GHz was achieved. Of course, the behavior of the buffer in this case was also influenced by the applied baluns used. Nevertheless, good matching in the target frequency range can be assumed. The peak small-signal gain was measured to be 12.7 dB, and the 3 dB bandwidth was 7.5 GHz. The insertion loss of the LC-baluns was 3 dB, measured using a back-to-back configuration. Considering this value, the de-embedded small-signal gain can be estimated to be 15.7 dB. The simulated saturated output power of the bare LO buffer is approximately 5 dBm.

The downstream power amplifier in the TX path boosts the signal. It draws 32 mA and is based on a cascode topology. Designing a separate test chip by employing the above-mentioned LC-baluns was again required to allow characterization in a single-ended measurement environment (cf. Fig. 2 (c)). Fig. 3 (b) shows the measured S-parameters. The circuitry




(a) (b) (c)

**Fig. 2.** (a) Microphotograph of the signal-generation chip. Size: $728 \times 728\ \mu m^2$. (b) Microphotograph of the dual–TRX chip. The Rat-race (RR) coupler is indicated by an arrow. It surrounds the mixer and also connects the power amplifier. Size: $1028 \times 1128\ \mu m^2$. (c) LOB (above) and PAM test chips with auxiliary baluns for single-ended characterization.

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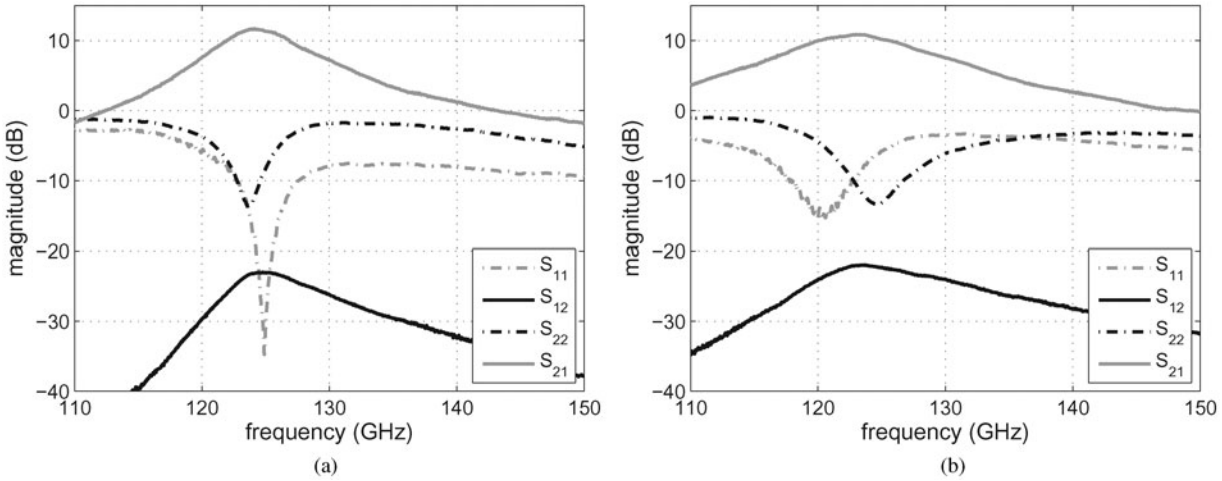


**Fig. 3.** Measured S-parameters of (a) the LO buffer test chip and (b) the power amplifier test chip. Both results are not de-embedded from the input and output LC-baluns.

exhibits a well-matched behavior over the target frequency span, although the minimum return loss is a little off-center. A peak small-signal gain of 11.7 dB, which equals 14.7 dB when the losses of the baluns are taken into account, and a 3 dB bandwidth of 12.5 GHz were measured. The saturated output power was measured to be higher than 7 dBm. However, the value was obtained with a W-band power meter, which is not calibrated above 110 GHz, but its operation has been verified.

A Gilbert cell topology was employed in making the double-balanced mixer. The circuit as implemented makes use neither of resistive emitter degeneration nor of a tail current source. Thus, the circuit is very sensitive to variations in the biasing point of the differential pair. The biasing network uses a diode-connected transistor to set the bias voltage at the RF input transistors. However, the emitter length of the diode-connected transistor in the biasing network was chosen to be smaller than that in the differential pair. Since these two devices show different forward voltages, the biasing point changes and consequently the tail current increases significantly, which degrades the performance of the mixer in terms of gain and noise figure. Nevertheless, a gain of approximately 10 dB at 125 GHz was measured.

## III. 122 GHZ FRONTEND

Fig. 4 (a) shows a block diagram of the radar sensor. The direct-digital synthesizer (DDS), phase-frequency discriminator (PFD), and loop filter (LF) are not located at the frontend, instead they are incorporated in the baseband board. Fig. 4 (b) depicts the radar demonstrator frontend in chip-on-board technology, which was built on a printed circuit board with a layer stack according to [11]. The design required low-loss interconnections because of the high operating frequency. Hence, bond–wire transitions and tracks for RF signals were kept as short as possible. To this end, the bare dies were attached in cavities in order to minimize the length of the bond–wires. Additionally, a differential off-chip bond–wire matching structure in conjunction with a differential single-patch antenna was designed for the TX and RX ports. The layout is shown in Fig. 4 (c) together with the chip arrangement. It uses a multisection transformer with two sections of transmission lines with lengths of approximately a quarter wavelength ($\lambda/4$) to overcome the high–impedance difference between the bond–wires and the antenna. The simulated insertion loss of the bond-wire transition including matching structure is 2.5 dB and the simulated differential single-patch microstrip antenna has a gain of approximately 6 dBi, a center frequency of 121 GHz, and a relative 10 dB return loss bandwidth of 7%.

The radar frontend (Figs. 4 (a) and (b)) uses a 17 GHz down-converter, a signal-generation chip, and two cascaded TRX chips forming a two-channel frontend. Obviously, each TRX uses the quasi-monostatic cells with separate TX and RX antennas. The output signal of the monostatic cell, however, was used for LO distribution, that is, it was connected to the LO input port of the downstream TRX chip. The perpendicular alignment of the TX and RX antennas allows TRX chips with different planes of polarization to be paired, thus forming a polarimetric radar. In this context, RX1/TX2 and TX1/RX2 can be combined. Other combinations allow measurement of the cross-polarization response of targets.

The signal-generation chip and the first TRX chip are collocated in a common cavity. Thus, the LO connection by means of chip-to-chip bonding was accomplished at the minimum distance. The LO connection between the TRX chips required distribution via tracks. However, the high gain of the LO buffer mitigates this constraint and ensures a proper LO level at the downstream TRX.

The 17 GHz SiGe down-converter chip is similar to that presented in [12]. It allows conversion of the prescaler output, which is around 15 GHz, down to a frequency that can be processed by the phase-locked loop (PLL) synthesizer located on the baseband board. This configuration leads to an offset-loop configuration for VCO stabilization [13]. Since the prescaler frequency is lower than the down-converter frequency, the tuning behavior is inverted and the control deviation decreases as the output frequency increases (reverse frequency position). Consequently, the polarity of the charge-pump current must be inverted for proper operation. For baseband signal generation and data acquisition, a fully customized base-band board similar to that described in [14] was employed.

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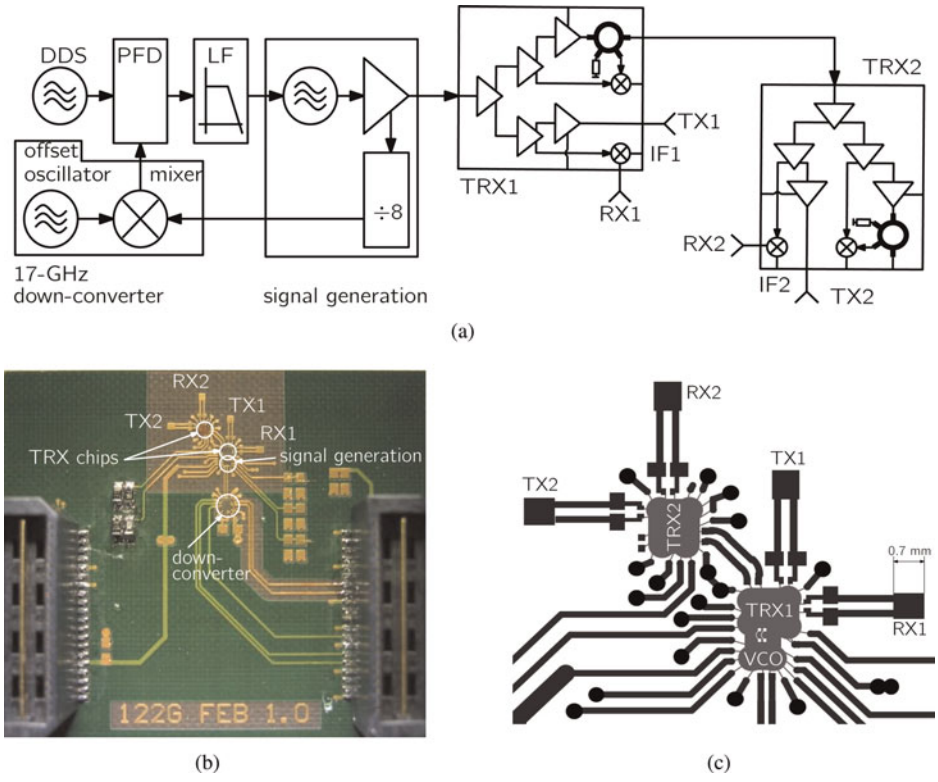


**Fig. 4.** (a) Block diagram of the radar sensor. It features an offset-loop PLL and two cascaded TRX chips. The DDS, PFD, and LF are located at the baseband board. (b) 120 GHz quasi-monostatic radar frontend with two channels perpendicularly arranged similar to a polarimetric radar. Size: 4 × 3.5 cm². (c) Breakout of the PCB layout showing the chip arrangement with the multisection transformer bond–wire matching structures and the differential single-patch microstrip antennas.

## IV. EXPERIMENTAL SETUP AND RESULTS

For the subsequent measurements, the PLL was equipped with a passive loop filter that does not allow generating tuning voltages exceeding the charge-pump supply voltage of 5 V. Hence, the maximum operating frequency in this setup was limited to approximately 123 GHz. The frequency sweep was accomplished by means of a DDS connected at the reference input of the 120 GHz PLL synthesizer. All measurement results presented are based on a single chirp measurement evaluated by applying a Von-Hann window function and subsequent Fourier transformation.

The first experimental setup is depicted in Fig. 5 (a). A small corner-cube (CC) reflector with a length of 39 mm at the shortest edge with a corresponding radar cross-section (RCS) of 1.9 dBsm served as target in the far field. The CC was attached on a wooden pole, which was again mounted on a linear rail in order to move the target back and forth. The FMCW sensor performed down chirps from $f_{\text{start}} =$ 122 GHz to $f_{\text{stop}} = 117$ GHz within $T_{\text{sweep}} = 2$ ms, and $N =$ 2500 data points were sampled per measurement cycle and channel. The measured amplitudes over distances from 1 to 4.5 m are shown in Fig. 5 (b). The figure also includes the predicted received signal amplitude. To this end, a link budget based on the basic radar equation (e. g., [15]) for point targets was calculated. Note that 5 dB IF amplifier gain were also incorporated.

Both results are in close agreement and the graphs nearly cover each other. However, the simulated values had to be shifted by −3 dB to consider the performance loss of the TRX due to the thermal warming of the chips. The outlier at 4 m stems from an interference of the metallic body of the linear rail. The link budget calculation furthermore confirmed the 2.5 dB insertion loss of the bond–wire transition (cold TRX).

The second experimental setup is shown in Fig. 6 (a). Two static CCs, $CC_1 = 9.4$ dBsm and $CC_2 = 12.1$ dBsm, were placed at different distances and angles. The FMCW parameters for this measurement setup were set to $f_{\text{start}} =$ 123 GHz, $f_{\text{stop}} = 116$ GHz, $T_{\text{sweep}} = 3$ ms, and $N = 3750$, that is, a sweep bandwidth of 7 GHz. Fig. 6 (b) depicts the resulting spectrum with two dominant peaks at 3.4 m ($CC_1$) and 4.0 m ($CC_2$). Another small peak at 4.5 m origins from the corner of the anechoic chamber.

To further evaluate the quality of the measurement results, 500 individual measurements were taken and statistically evaluated. Fig. 7 depicts the 500 measurement results for the position of $CC_1$ and shows the corresponding histogram with a binwidth of 45 μm. A Gaussian distribution of identical mean and variance was inserted additionally. The evaluation for the CC positions yielded means and standard deviations of $\mu_{CC_1} = 3432.598$ mm, $\sigma_{CC_1} = 115$ μm and $\mu_{CC_2} =$ 4061.003 mm, $\sigma_{CC_2} = 133$ μm, respectively. The standard deviation at $CC_2$ is greater than that at $CC_1$ since the signal-to-noise ratio is slightly worse due to reflections of the metallic tripod and multipath effects in the vicinity to the corner. The Cramér–Rao bound states a limit below which the variance of an unbiased estimator can not fall [16]. The results above attained this theoretical limit, which is also an indicator for a well–designed system.

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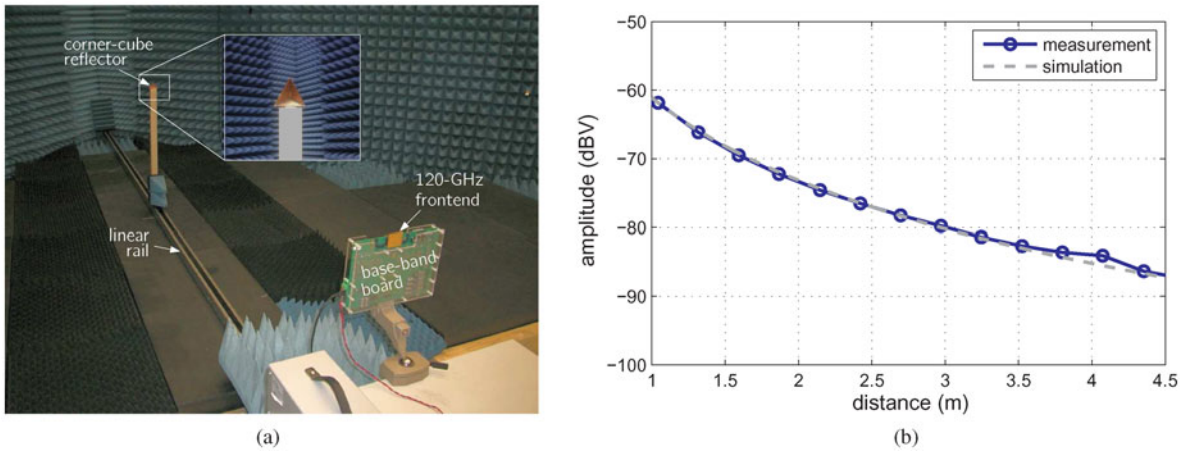


**Fig. 5.** (a) First experimental setup with a small CC (1.9 dBsm) mounted on a linear rail. (b) Measured amplitude over target distance compared to the theoretical values according to the basic radar equation.

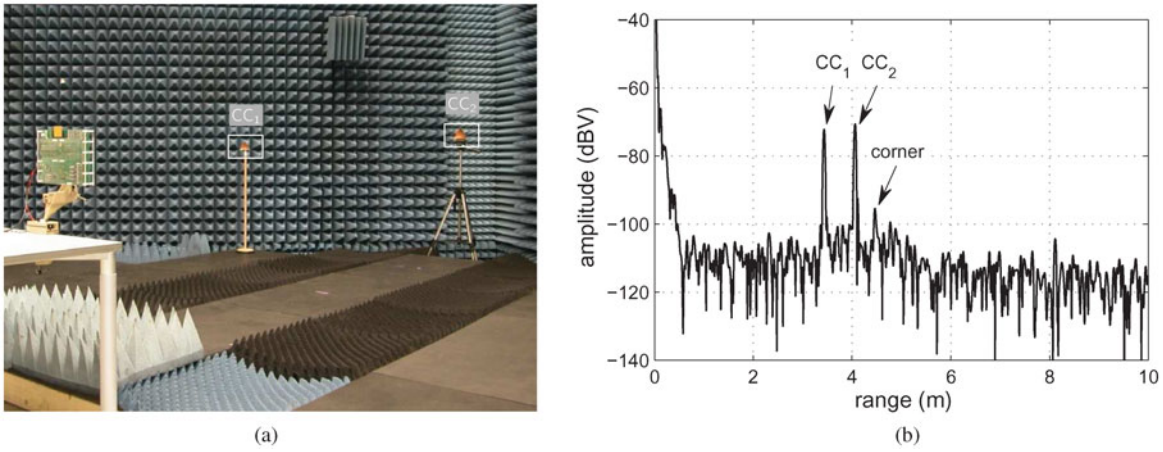


**Fig. 6.** (a) Second experimental setup with two static CCs. (b) Measured amplitude spectrum. FMWC parameters: $f_{start} = 123$ GHz, $f_{stop} = 116$ GHz, and $T_{sweep} = 3$ ms.

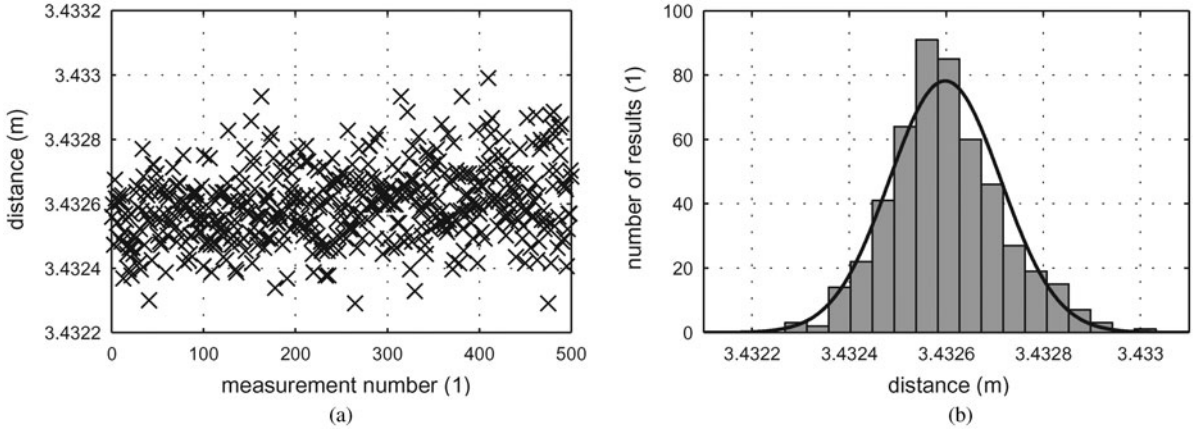


**Fig. 7.** (a) 500 individual measurement results for position of $CC_1$. (b) Histogram of the 500 individual measurements (binwidth 45 μm) and Gaussian distribution with identical mean and variance.

As a final inspection, the corresponding windowing function (Von-Hann window) was plotted over the target peaks as can be seen in Fig. 8 (a). The close-up view for the peak of $CC_1$ is shown in Fig. 8 (b). The main lobes match very well and only a minor broadening can be examined in the measurement data. Thus, one can conclude that a proper linear frequency ramp with 7 GHz bandwidth can be provided by the PLL. Also chips, matching structure, and antenna

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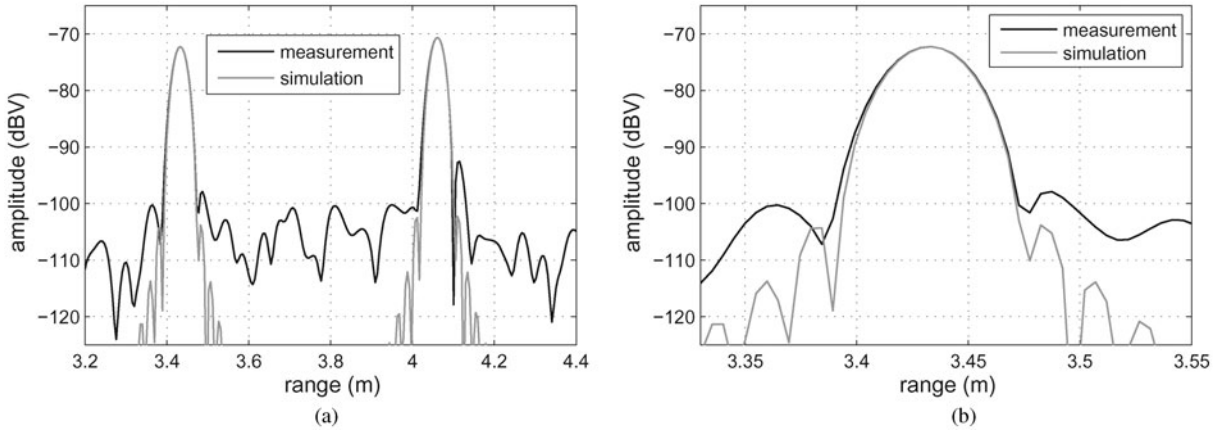


**Fig. 8.** (a) Comparison of the resulting measurement peaks with the simulated Von-Hann windowing function. (b) Close-up of peak $CC_1$. Only a minor minor broadening of the main lobe can be identified.

provide sufficient bandwidth, because any inferior behavior would inevitably broaden the main lobe and hence affect the variance of the estimation results.

## V. CONCLUSION

This paper presented a two-channel 120 GHz quasi-monostatic FMCW radar demonstrator using a fundamental-wave SiGe signal-generation chip and two cascaded SiGe TRX chips. The radar sensor was built on RF substrate in chip-on-board technology with off-chip differential microstrip antennas in conjunction with matching structures for the bond–wire transition. The designed chips were tested successfully in a radar sensor application, and measurements verified the capability of 7 GHz frequency sweeps.

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**M. Jahn** received a Dipl.-Ing. (M.Sc.) degree in mechatronics from the Johannes Kepler University, Linz, Austria, in 2007. Since 2007, he has been with the Institute for Communications Engineering and RF-Systems at the University of Linz, Austria, and since 2008 he has been working toward the Ph.D. degree as a Research Assistant. His research interests include RF and millimeter-wave–integrated circuits with emphasis on system design for millimeter-wave radar sensors operating above 100 GHz.

**Andreas Stelzer** received a Diploma Engineer degree from the Technical University of Vienna, Vienna, Austria, in 1994, and the Dr. techn. degree (Ph.D.) from the Johannes Kepler University, Linz, Austria, in 2000. In 2003, he became Associate Professor at Johannes Kepler University. Since 2007, he has been Head of the Christian Doppler Laboratory for Integrated Radar Sensors, and since 2011 he has been a full Professor at Johannes Kepler University, heading the department for RF-Systems. He has authored or coauthored over 245 journal and conference papers. His research is focused on microwave sensor systems for industrial and automotive applications, RF and microwave subsystems, surface acoustic wave sensor systems, as well as digital signal processing for sensor signal evaluation. Dr. Stelzer received several awards including the EEEfCOM Innovation Award and the European Microwave Association (EuMA) Radar Prize in 2003. He was also the recipient of the 2011 German Microwave Conference (GeMiC) Best Paper Award as well as the 2008 IEEE Microwave Theory and Techniques Society (IEEE MTT-S) Outstanding Young Engineer Award and the 2011 IEEE Microwave Prize.

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