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Research on digital predistortion based on adaptive algorithms†

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In wireless broadband communication systems, the inherent non-linearity of power amplifiers creates spectral growth beyond the signal bandwidth, which interferes with adjacent channels. It also causes distortions within the signal bandwidth. In this paper, we study five digital predistortion algorithms for linearising two different non-linear memory power amplifier models. The simulation results show that the proposed digital predistorter using different algorithms can improve the in-band distortion and out of band spreading in different ways. In particular, the DLMS algorithm with fast convergence can significantly suppress spectral regrowth (by 60dB), effectively compensating for the non-linearity of the power amplifier.

1. Introduction

Power amplifiers are an indispensable component of wireless communication systems. However, power amplifiers also generate spectral regrowth because of their inherent non-linearity, which leads to adjacent channel interference and in-band distortion (He and Chen 2010; Ding 2004). Thus, linearisation techniques are required to obtain power amplifiers with a high efficiency and good linearity. Digital predistortion technology is becoming the major linearisation technology for RF power amplifiers in future communication systems due to its great adaptability, simple structure and low cost characteristics (Du 2010; Zhang *et al.* 2008).

Adaptive technology has the ability to track the time-varying signals in an unknown environment, and this has become an important tool for signal processing. Therefore, adaptive predistortion technology can not only automatically correct the input signals to make the amplifier output have a linear characteristic, but also compensate for the changes in the amplifier characteristics due to device ageing and temperature drift (Zhang *et al.* 1981; Wang 2009; Wu 2009).

In the current paper, we propose a digital predistortion technology for multi-carrier broadband communication systems. In particular, we have applied it to a WCDMA system. By analysing the theory of the traditional least mean squares (LSM) algorithm

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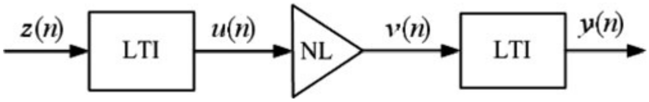

Fig. 1. The Wiener–Hammerstein model

and its variable step-size variants, we then present an indirect learning architecture to construct a predistorter based on different algorithms for two types of power amplifier.

2. Modelling power amplifiers

In broadband communication system, such as WCDMA, the memory effects of the power amplifier cannot be ignored as the input signal bandwidth becomes wider. In the current paper, we concentrate on two types of memory amplifier model: the Wiener–Hammerstein model and the polynomial model (Mahfuz and Wang 2007; Zhao 2011).

2.1. *The Wiener–Hammerstein model*

The Wiener–Hammerstein model is composed of an LTI system, followed by a memoryless non-linearity, which in turn is followed by another LTI system – see Figure 1. This configuration is commonly used for satellite communication channels. The subsystems in this model are described as follows:

$$u(n) = \sum_{l=0}^{L-1} a_l z(n-l)$$

$$v(n) = \sum_{\substack{k=1 \\ odd}}^{K} b_k u(n)|u(n)|^{k-1}$$

$$y(n) = \sum_{l=0}^{L-1} c_l v(n-l)$$

where a_l and c_l are the impulse response values of the LTI systems, respectively, before and after the memoryless non-linear block and the b_k are the coefficients of the non-linear block.

2.2. *The memory polynomial model*

The most commonly adopted memory polynomial model uses the diagonal kernels of the Volterra series, which is described by

$$y_k(n) = \sum_{q_1=0}^{Q-1} \cdots \sum_{q_2=0}^{Q-1} h_k(q_1, q_2, \cdots, q_k) \prod_{l=1}^{k} x(n-q_1)$$

where

$$y(n) = \sum_{k=0}^{k^2} c_l \sum_{q=0}^{Q-1} h_{k,q} x(n-l)|x(n-l)|^{k-1}.$$

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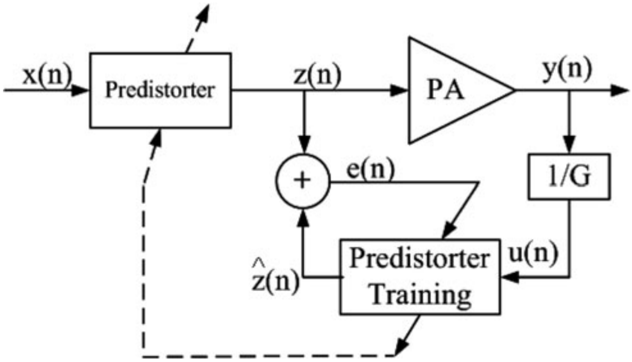

Fig. 2. The indirect learning architecture for the predistorter

In these equations, h_k is the k-order kernel of the Volterra series, Q is the memory depth and k is the non-linear order of the Volterra series. In the actual system, all off-diagonal kernels of the Volterra series are defined to be zero, thus the power amplifier model can be rewritten as

$$y(n) = \sum_{k=0}^{K} c_l \sum_{q=0}^{Q-1} h_{k,q} x(n-l)|x(n-l)|^{k-1}.$$

This equation is just the memory polynomial model, which can accurately characterise the properties of an actual power amplifier.

3. Architecture of the predistorter

The most popular designs for digital predistorters use either direct or indirect learning approaches. The former first identifies the power amplifier and then finds its inverse. The latter designs the predistorter directly, and is the approach adopted in this paper. The advantage of this structure is that it eliminates the need for assumptions about the model and parameter estimation for the power amplifier. A block diagram of the indirect learning structure is shown in Figure 2, where the feedback path labelled 'Predistorter Training' has $y(n)/G$ as its input, where G is the intended power amplifier gain, and $\hat{z}(n)$ as its output. The actual predistorter is an exact copy of the feedback path, which has $x(n)$ as its input and $z(n)$ as its output. Ideally, we would like $y(n) = G * x(n)$, which makes $z(n) = \hat{z}(n)$ and the error term $e(n) = 0$. Given $y(n)$ and $z(n)$, this structure enables us to find the predistorter parameters directly. The algorithm converges when the error energy $\|x\|^2$ is minimised.

4. Principle of the adaptive algorithm

The identification system is the key to the linearisation techniques based on an adaptive predistorter, which can constantly update the coefficients by tracking the variations of the power amplifier. It is obvious that the performance of the digital predistortion system is directly influenced by the adaptive identification algorithms. For this reason, the

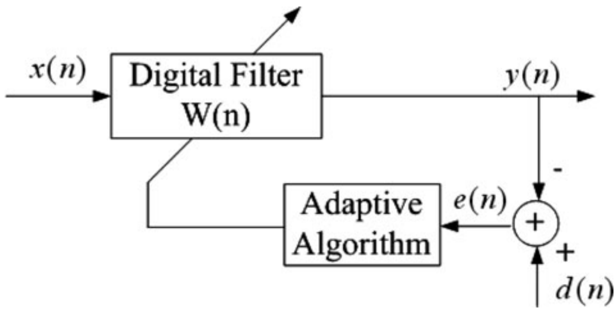

Fig. 3. Block diagram for an adaptive filter

algorithms in the field of linearising filters have been deeply researched for application to non-linear predistorters.

The basic LMS algorithm and its variable step-size variants are all linear adaptive filtering algorithms, and are composed of a digital filter whose parameters are adjustable and an adaptive algorithm. The operation principle is shown in Figure 3. The error estimate signal is described by the equations

$$e(n) = d(n) - y(n).$$

If we define

$$x_L(n) = [x(n), x(n-1), \cdots, x(n-L+1)]^T,$$

where x(n) and y(n) are the the input and output signals, respectively, we obtain

$$y(n) = \sum_{i=1}^{L} w_i x(n-i+1) = X_L^T(n) W_L$$

where

$$W_L = [w_1, w_2, \ldots, w_L]^T$$

is the coefficient of the adaptive filter.

4.1. *The LMS algorithm*

The LMS algorithm is based on the mean square error (MSE), with the stochastic gradient descent method used to minimise the MSE. Specifically, in order to achieve the optimal weights and the adaptive filter in the sense of the least mean squares, in each iteration, the weight vectors upgrade the steps by a certain percentage along the negative direction of the calculated gradient of the error performance surface. The iterative equation for the filter is

$$W(n) = W(n-1) + 2\mu e(n) x(n)$$

where μ is the step-size factor of the adaptive filter.

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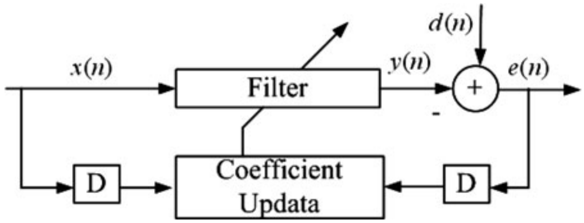

Fig. 4. Block diagram for the DLMS algorithm

4.2. *The RLS algorithm*

The recursive least squares (RLS) algorithm is based on the least squares criterion, where the sum of the squares of the difference between the reference signals and the filter's output signal is to be minimised. The iterative equation for the filter is

$$W(n) = W(n-1) + \frac{1}{\lambda} R^{-1}(n-1)e(n)x(n)$$

where $0 < \lambda \leqslant 1$ is the genetic factor and

$$R(n-1) = E[x(n-1)x^T(n-1)]$$

is the autocorrelation matrix of the input signals at time n-1.

4.3. *The NLMS algorithm*

The normalised least mean squares (NLMS) algorithm is based on the LMS algorithm. It is a variable step-size algorithm, which accelerates the convergence by changing the step factor indirectly. The iterative equation for the filter is

$$W(n) = W(n-1) + \frac{\eta}{x^H(n)x(n) + \psi} e(n)x(n)$$

where ψ and η are both constants, with $0 < \eta < 1$ used to guarantee the imbalance coefficients of the LMS algorithm have a fixed value.

4.4. *The DLMS algorithm*

Because of the slow convergence process caused by the conflict between the step factor and convergence rate, Long and Herzberg proposed the delay LMS (DLMS) algorithm as a variant of the traditional LMS algorithm – see Figure 4. Compared with the LMS algorithm, the delayed cycle number d is used to update the coefficients of the DLMS algorithm at the next clock cycle. Thus, the throughput of the DLMS algorithm data is twice that of the LMS, and it is thus more suitable for high-speed signal processing. The iterative equation for the filter is

$$W(n) = W(n-1) + 2\mu e(n-d)x(n-d)$$

where the parameter d is the delayed cycle number, which is introduced when the weight coefficients are updated.

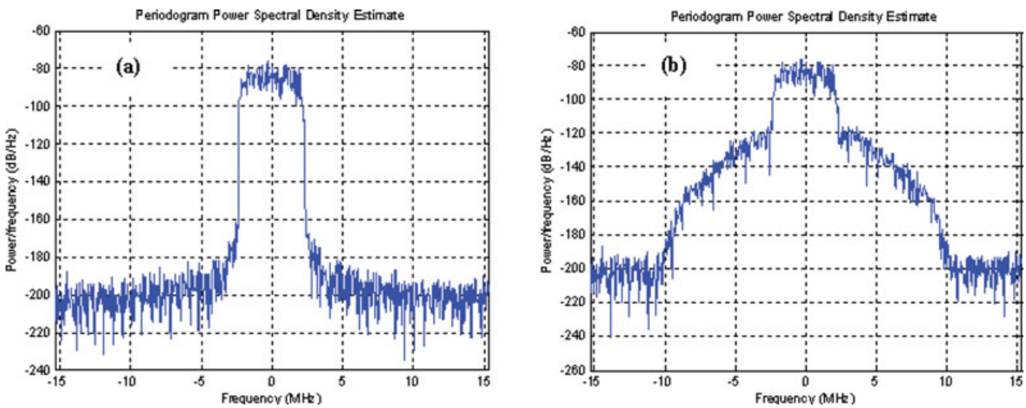

Fig. 5. (Colour online) Power spectrum of input (a) and output (b) signals without the predistorter (Wiener–Hammerstein model)

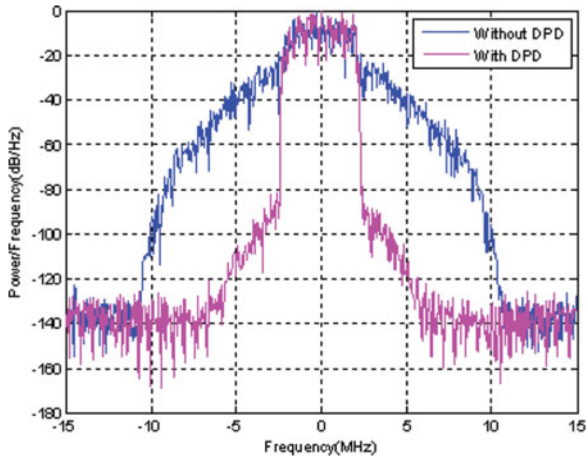

Fig. 6. (Colour online) Performance of the predistorter with the LMS algorithm (Wiener–Hammerstein model)

4.5. *The sign LMS algorithm*

The stochastic gradient descent method is also used in the sign LMS algorithm to obtain the optimal solution, though this method only gives the optimal solution and not the size of the gradient. The iterative equation for the filter is

$$W(n) = W(n-1) + 2\mu \ \mathrm{sign}[e(n)]x(n)$$
$$W(n) = W(n-1) + 2\mu e(n) \ \mathrm{sign}[x(n)]$$

where sign is the sign function, and the first equation is the sign LMS algorithm for the error signals and the second is for the input signals.

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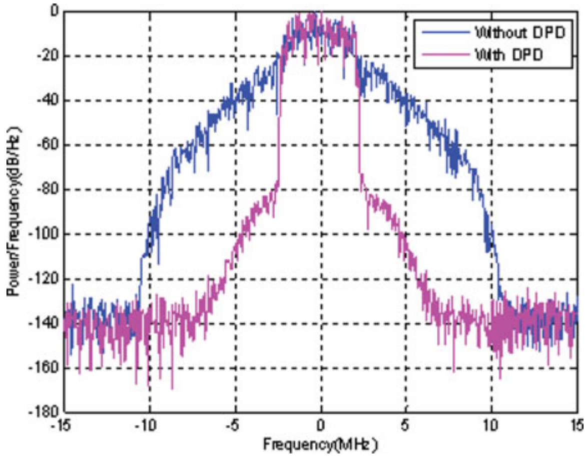

Fig. 7. (Colour online) Performance of the predistorter with the RLS algorithm (Wiener–Hammerstein model)

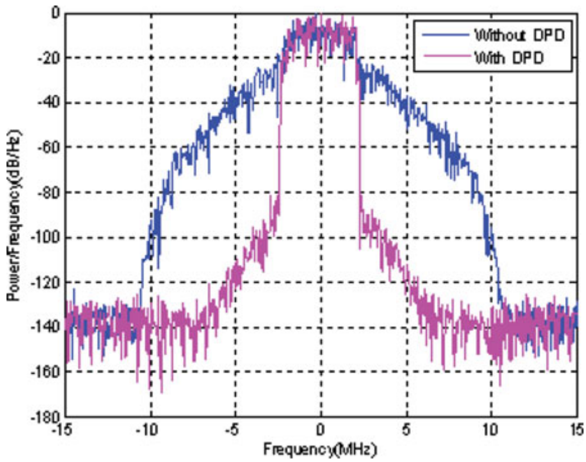

Fig. 8. (Colour online) Performance of the predistorter with the NLMS algorithm (Wiener–Hammerstein model)

5. Simulation of adaptive digital predistortion

In order to verify the validity and feasibility of the proposed adaptive digital predistorter, a source generation and simulation test platform was set up using MATLAB software. Specifically, following one of the 3GPP25.141 protocol test patterns, we generated two frame business source with 78848 dates. We then simulated single and dual carrier signals for a WCMDA system on the test platform using the two different power amplifier models under consideration.

5.1. *Simulation with the Wiener–Hammerstein model*

When the power amplifier is modelled as a Wiener–Hammerstein model, the coefficients for the case where there is no linearisation process using the predistorter, which were

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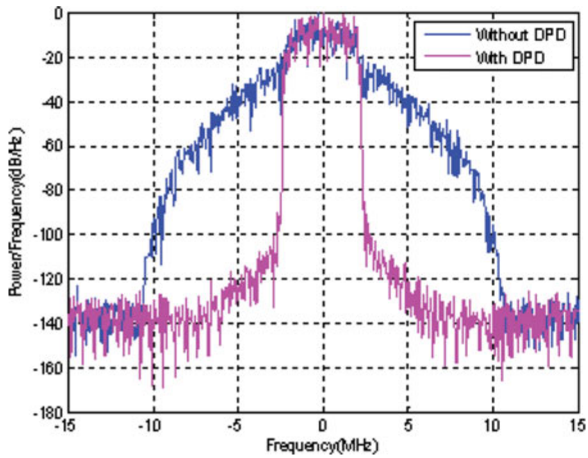

Fig. 9. (Colour online) Performance of the predistorter with the DLMS algorithm (Wiener–Hammerstein model)

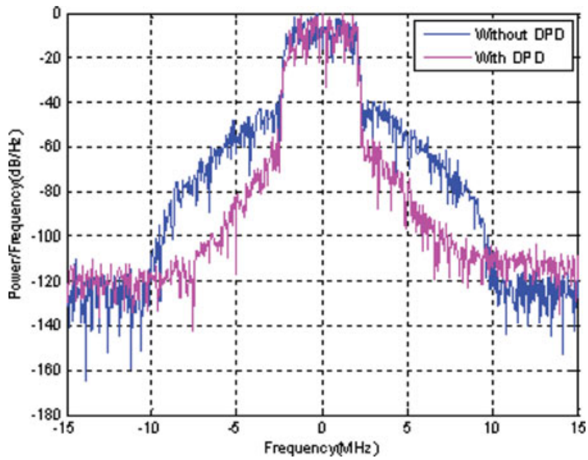

Fig. 10. (Colour online) Performance of the predistorter with the sign LMS algorithm (Wiener–Hammerstein model)

extracted from the actual Class AB power amplifier, are

$$c_1 = +1.0108 + 0.0858j$$
$$c_3 = +0.0879 - 0.1583j$$
$$c_5 = -1.0992 - 0.8891j.$$

The WCDMA system's single carrier signal was adopted as the baseband input signals. The power spectrum of the input and output signals without the predistorter is shown in Figure 5.

We then analysed the memory polynomial predistorter with memory length 3 and 5th odd-order non-linearity, with the predistorter coefficients constantly updated using the algorithms described earlier in the paper.

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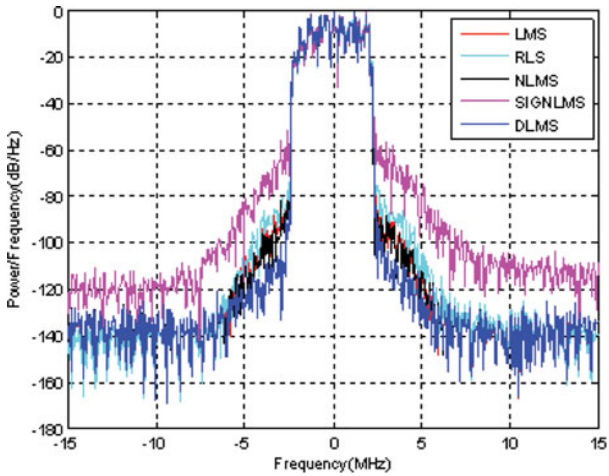

Fig. 11. (Colour online) Performance comparison of the predistorter using the different algorithms (Wiener–Hammerstein model)

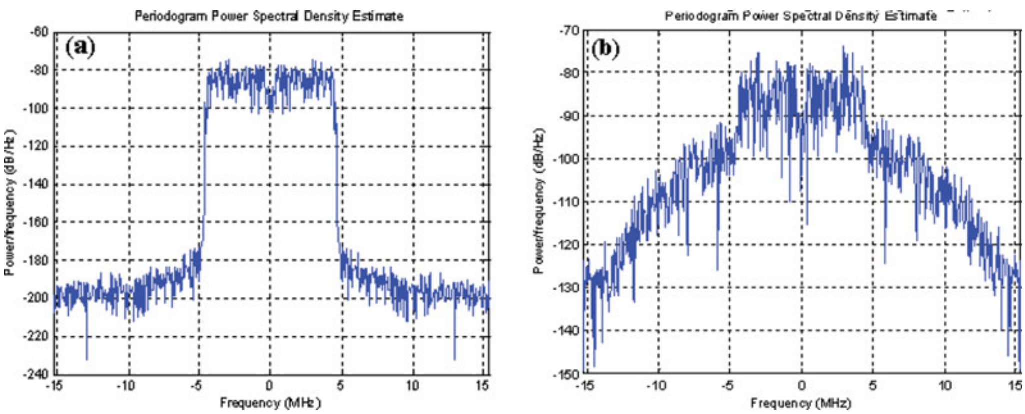

Fig. 12. (Colour online) Power spectrum of input (a) and output (b) signals without the predistorter (polynomial model)

In iterating the LMS and RLS algorithms, we used a step factor of $\mu = 0.005$ and genetic factor $\lambda = 0.095$. The output signal with and without the memory polynomial predistorter is shown for the LMS and RLS algorithms in Figures 6 and 7, respectively.

In iterating the NLMS and DLMS algorithms, we used the values $\psi = 0.02$, $\eta = 0.095$, the step factor $\mu = 0.005$ and the delay number in the weight updating $d = 5$. The performance of the predistorter using the NLMS and DLMS algorithms is shown in Figures 8 and 9, respectively.

Using the two iterative formulas given in Section 4.5 for the sign LMS algorithm, the error signals were simulated to determine the performance of the predistorter – see Figure 10.

Figure 11 compares the performance of the predistorter using each of the five adaptive algorithms.

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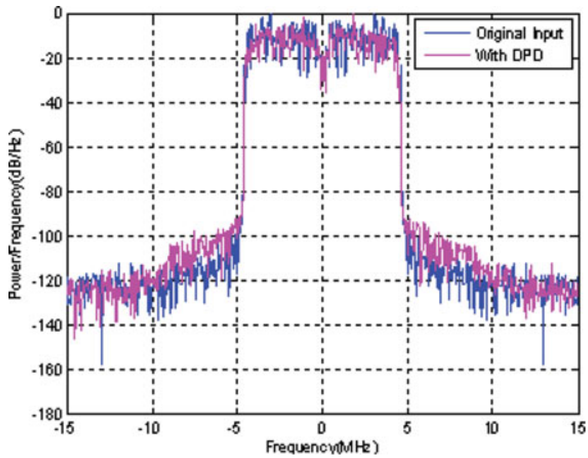

Fig. 13. (Colour online) Performance of the predistorter with the LMS algorithm (polynomial model)

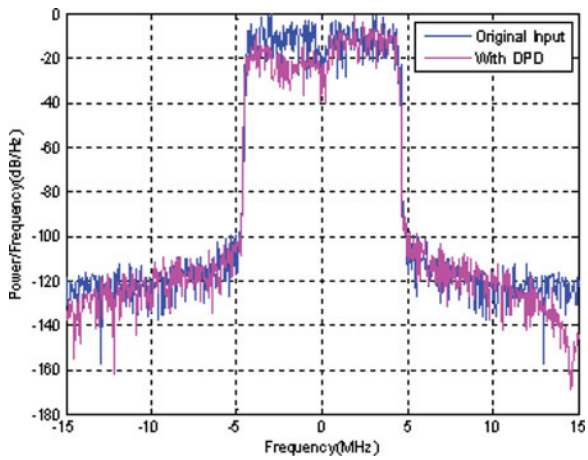

Fig. 14. (Colour online) Performance of the predistorter with the RLS algorithm (polynomial model)

When the Wiener–Hammerstein model was adopted as the model for the predistorter and amplifier, the above simulation characteristics show that when the sign LMS algorithm is used, there is only limited improvement of the outband distortions by about 20dB. However, in comparison with the other algorithms, the DLMS and NLMS algorithms can significantly suppress spectral regrowth by about 60dB.

5.2. *Simulation with a polynomial model*

When the power amplifier was constructed with a polynomial model, the coefficients, which were extracted from an actual Class AB power amplifier, were

$$b_{10} = +1.0513 + 0.0904j$$
$$b_{30} = -0.0542 - 0.2900j$$

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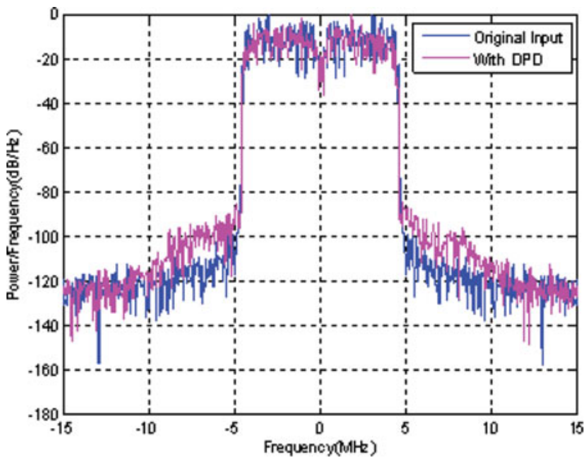

Fig. 15. (Colour online) Performance of the predistorter with the NLMS algorithm (polynomial model)

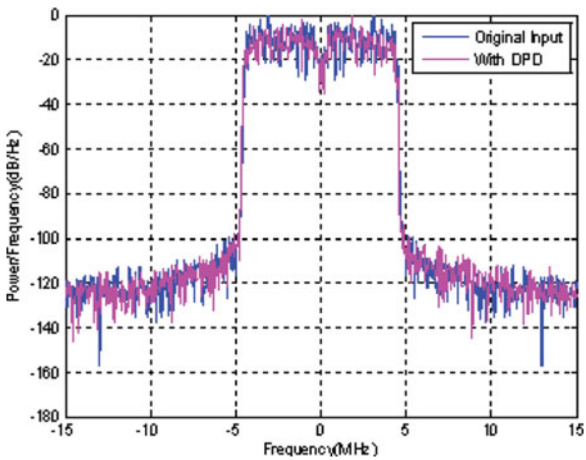

Fig. 16. (Colour online) The performance of predistorter with DLMS algorithm (polynomial model)

$$b_{50} = -0.9657 - 0.7028j$$
$$b_{11} = -0.0680 - 0.0023j$$
$$b_{31} = +0.2234 + 0.2317j$$
$$b_{51} = -0.2451 - 0.3735j$$
$$b_{12} = +0.0289 - 0.0054j$$
$$b_{32} = -0.0621 - 0.0932j$$
$$b_{52} = +0.1229 + 0.1508j.$$

In this case, we adopted the dual carrier signal of the WCDMA system as the baseband input signals. Figure 12 shows the power spectrum of the input and output signals without the predistorter.

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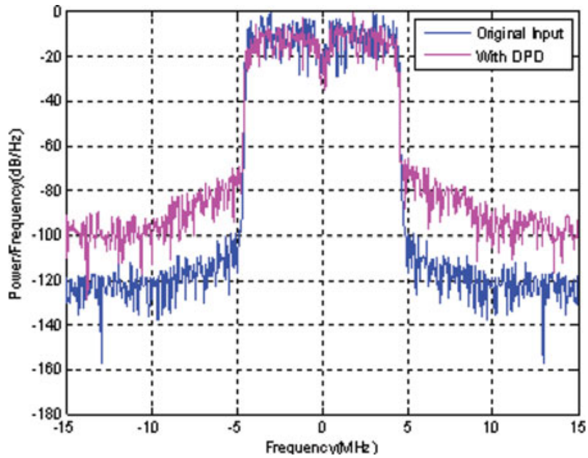

Fig. 17. (Colour online) Performance of the predistorter with the sign LMS algorithm (polynomial model)

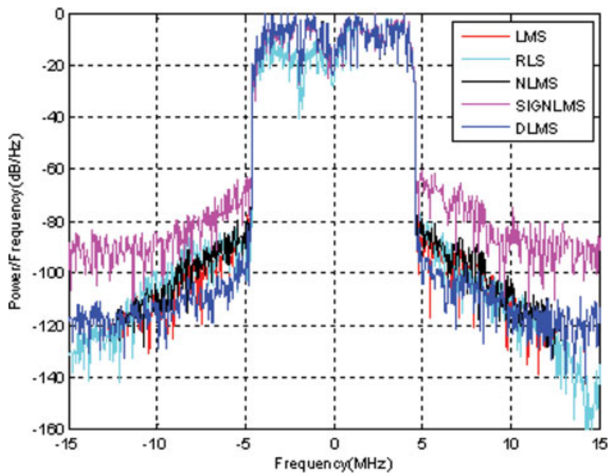

Fig. 18. (Colour online) Performance comparison of the predistorter with the different algorithms (polynomial model)

We again analysed the memory polynomial predistorter with memory length 3 and 5th odd-order non-linearity.

In iterating the LMS and RLS algorithms, we used a step factor of $\mu = 0.005$ and genetic factor $\lambda = 0.095$. The output signal with and without the predistorter is shown for the LMS and RLS algorithms in Figures 13 and 14, respectively.

In iterating the NLMS and DLMS algorithms, we used the values $\psi = 0.02$, $\eta = 0.095$, the step factor $\mu = 0.001$ and the delay number in the weight updating $d = 2$. The performance of the predistorter using the NLMS and DLMS algorithms is shown in Figures 15 and 16, respectively.

The error signals were also simulated for the sign LMS algorithm – see Figure 17.

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Figure 18 compares the performance of the predistorter using each of the five adaptive algorithms.

It is obvious from the above simulation characteristics for the adaptive algorithms when the polynomial model was adopted as the model for the predistorter and amplifier that all the algorithms apart from the sign LMS algorithm can dramatically suppress the adjacent interference. In particular, the original input and output signals almost coincide when the DLSM algorithm was adopted to update the predistorter coefficients.

6. Conclusions

In this paper, we have proposed memory polynomial predistortion constructed with an indirect learning architecture to counteract non-linear distortion and memory effects arising from the power amplifier. In the process of linearising two types of power amplifier, we used the LMS algorithm and its variable step-size variants to carry out a performance analysis. The different algorithms may have different performance characteristics for different power amplifier designs, but the DLMS algorithm seems to be superior because of its fast convergence and high-speed processing characteristics.

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