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A 60 GHz 14 dBm power amplifier with a transformer-based power combiner in 65 nm CMOS

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A 52–61 GHz power amplifier (PA) is implemented in 65 nm bulk complementary metal oxide semiconductor (CMOS) technology. The proposed PA employs a transformer-based power combiner to sum the output power from two unit PAs. Each unit PA uses transformer-coupled two-stage differential cascode topology. The differential cascode PA is able to increase the output power and ensure stability. The transformer-based passives enable a compact layout with the PA core area of only 0.3 mm^2. The PA achieves a peak power gain of 10.2 dB with 3-dB bandwidth of 9 GHz. The measured saturated output power is 14.8 dBm with a peak power-added efficiency (PAE) of 7.2%. The reverse isolation is smaller than −33 dB from 25 to 65 GHz. The PA consumes a quiescent current of 143 mA from a 1.6 V supply.

Keywords: power amplifiers, cascode stage, differential signalling, transformer, power combiner, CMOS, 60 GHz

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I. INTRODUCTION

The demand for gigabit-per-second short-range wireless communication systems is increasing daily while the opening up of the 57–64 GHz unlicensed band presents new opportunities. IEEE standard 802.15.3c [1] defines the specifications for wireless personal area network (WPAN) in a 60 GHz band, which enables applications such as uncompressed video streaming, office desktop data transfer, and kiosk file downloading. IEEE 802.11ad [2] is tasked to amend the existing 802.11 WLAN standard to enable a maximum throughput of at least 1 Gbps, which is comparable to the existing wired LAN products. Furthermore, the wireless gigabit alliance has proposed and launched the technology to drive the industry convergence to a single radio in the unlicensed 60 GHz spectrum [3].

The millimeter-wave (mm-wave) power amplifier (PA) design has been one of the most significant challenges to a full integration of a complete wireless communication system on a single chip in the 60 GHz band. To set up a communication range of 1 m, an output power of 10 dBm is required while a bandwidth of 7 GHz is preferred to cover the whole frequency band and enable channel bonding. Although mm-wave PAs have traditionally been implemented in III–V compound semiconductors such as GaAs and InP, CMOS technologies are now capable of operating at mm-wave frequencies [4–10]. CMOS technologies can offer the advantages of integration density on a single chip and the potential for reducing cost with increasing production volume. However, the low operation voltage of an MOS transistor, limited by the low breakdown voltage, and lossy passive components restrict the performance of CMOS PAs in 60 GHz band. One potential solution is to use the power combining technique [11], which combines the output power of several unit PAs to achieve a higher output power. Increasing the number of unit PAs may improve the output power whereas it complicates the floor plan of the PA. Wilkinson or hybrid power combiners have been utilized that require quarter-wave transmission lines (TLs) and thus consumes relatively large silicon area [12].

This paper presents a 60 GHz wideband PA [13] using a transformer-based power combining technique to improve the output power and save chip area. It is fabricated in a 65 nm low-power bulk CMOS technology. The paper is organized as follows. Section II addresses the mm-wave PA design strategies and explains the advantages of using differential cascode amplifier topology and power combining technique. Section III details the PA design. Experimental results and conclusions are presented in Sections IV and V, respectively.

II. DESIGN STRATEGIES FOR MM-WAVE PA

At mm-wave frequencies, new challenges are posed on the PA designs. As the operating frequencies approach a fraction of the transistor's cut-off frequency, the decreasing active power gain of the transistor and high-loss passives limit the gain and efficiency of PAs, which increase the system power consumption and potentially cause thermal dissipation issues. Besides, the sizes of components are comparable with wavelength and thus microwave theory applies. Device and interconnect parasitics represent a large portion of the total impedance or admittance at a node, and so the layout

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optimization and parasitic extraction are crucial. In this section, our treatments will be focused on cascode amplifier stage and power combining technique to improve the output power, and the differential signaling to ensure signal integrity.

A) Cascode amplifier stage

Scaling of CMOS technologies leads to reduced channel length and gate oxide thickness. Although mm-wave circuits benefit from this scaling trend, its direct negative impact on PA design is the lowered breakdown voltage. The breakdown mechanisms of MOS transistors can be categorized as gate oxide breakdown, drain-bulk breakdown, punch-through, and hot carrier degradation while the last one is the limiting factor [14]. Hot carrier degradation occurs when the carriers in the channel are accelerated by the large drain-to-source voltage. In 40 nm CMOS technology, the maximum DC and RF drain-to-source voltages have to be smaller than 1.25 and 1.4 V, respectively, when the gate bias voltage is 0.7 V, to ensure a 10-year lifetime [15]. In the proposed PA, cascode stage is used to extend the output voltage swing. Figure 1 shows the cascode and common-source (CS) stages with output matching network. The voltage waveforms at different nodes of the cascode stage are studied. As shown in Fig. 2, since the drain and source voltages of the transistor M_2 are in phase, the actual voltage across the transistor V_{ds} is reduced by 30%. Compared to the CS stage with the same breakdown voltage, cascode stage has 1.5 dB improvement in output power when the optimum load impedance is adjusted.

Apart from the capability to deliver more output power, the cascode stage alleviates the miller effect and therefore presents wide bandwidth and better stability. The improved reverse isolation also eases the design procedure. Compared with the CS stage, simulation results show that the cascode amplifier has more than 3 dB in maximum power gain (G_{max}), exceeds15 dB in S_{12}, and is unconditional stable at 60 GHz, as shown in Fig. 3.

B) Power combining technique

The power combining technique provides another solution to improve the output power. As discussed in the previous section, the low breakdown voltages limit the voltage swing at PA's output to approximately ± 0.5 V for a CS stage and ± 0.7 V for a cascode stage, respectively, in 65 nm CMOS. An impedance transformation network is usually inserted between the output stage and the transmit antenna to achieve the required output power. A large transformation ratio and lossy passive components significantly degrade the efficiency of the PA at mm-wave frequencies. Power combining technique combines the output power of several unit PAs, which can achieve relatively high efficiency. When all the unit PAs have the same output impedance, the total output power delivered to the load equals [11]

$$P_o = N^2 m^2 \frac{V_{PA}^2}{R_L}, \quad (1)$$

where N is the number of the unit PAs, m the transformer turn ratio, V_{PA} the output voltage swing of the unit PA, and R_L the load of the complete PA. It can be seen that the impedance transformation ratio can be traded off with the number of unit PAs. An output matching network with low transformation ration leads to higher efficiency and broader bandwidth [16]. Therefore, a transformer-based power combiner was adopted in this design, as shown in Fig. 4. The power combiner was implemented in an overlay configuration with top two metals, achieving a coupling factor of 0.7. Instead of placing the primary and secondary coils on top of each other, an offset was introduced between the two coils to improve the matching between the load and the output impedance of the PA. The metal width of the two coils was optimized to minimize the insertion loss (1 dB) and extend the self-resonance frequency (100 GHz) of the power combiner.

C) Differential signaling

To ensure the signal integrity at mm-wave frequencies is another challenge. It is not easy to make a low-impedance ground plane in the mm-wave frequency range. For instance, at 60 GHz, a 10 pH inductance in the ground plane adds 4 Ω reactance to the AC ground of a single-ended amplifier stage. This degeneration inductance reduces power gain and efficiency of the PA and it has to be modeled well. The virtual ground nature of the differential pair provides a local AC ground, which avoids this unwanted effect from the ground inductance, and high-frequency performance can be restored. Although the differential circuit consumes twice as much power as the single-ended circuit, it provides 3 dB extra output power.

For a multistage amplifier, unwanted coupling of signals between stages may cause instability [17]. One of the primary undesired couplings is through on-chip supply or ground lines. The differential amplifier is not immune to

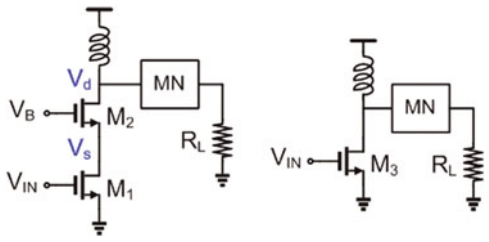

Fig. 1. Cascode and CS stages with output matching networks.

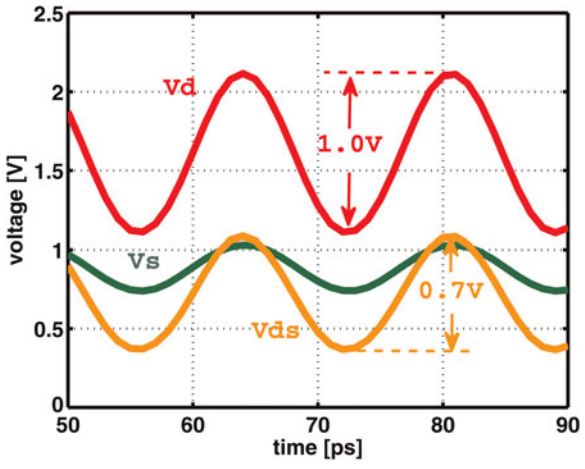

Fig. 2. Transient voltage waveforms of the cascode stage (Fig. 1) with a matched output.

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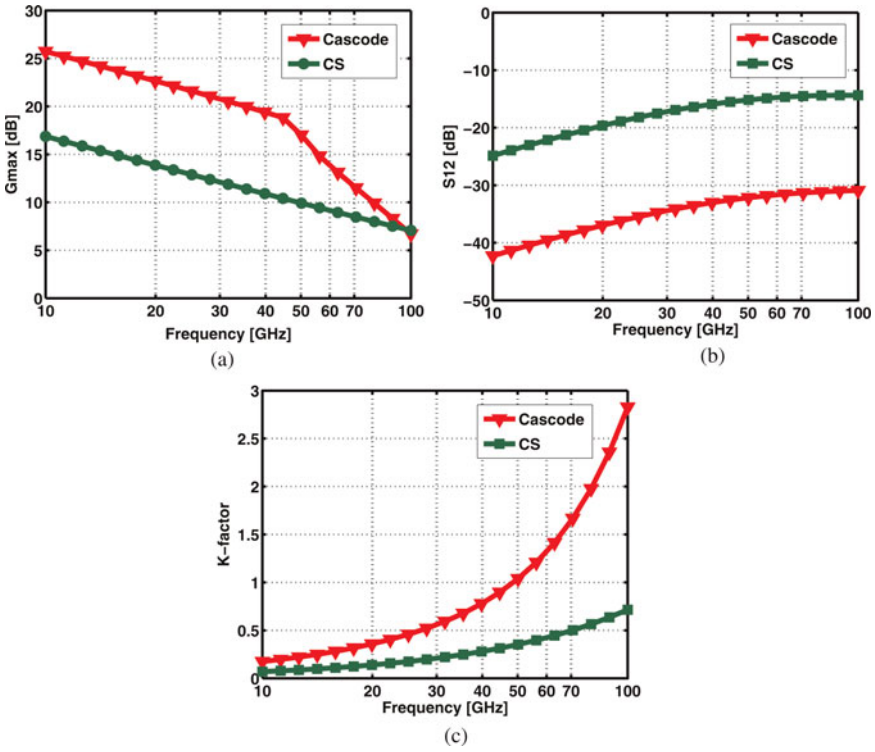

Fig. 3. Simulated performance comparison between cascode and CS stages in (a) G_{max}, (b) S_{12}, and (c) k-factor. The size of the back-annotated transistor is 40 μm with 1 μm finger width.

this problem especially when the PA produces highly nonlinear outputs or it is integrated in a system. Illustrated in Fig. 5, the supply line and signal path close the unintended loop that does not affect differential operations. However, common-mode positive feedback can occur between the two gain stages at certain frequency. Similarly, the ground bounce also affects the stability of a multistage amplifier. Therefore, the supplies and grounds of the driver stage and the output stage were separated in the design to improve the stability of the PA. Note that supply and ground separations between stages are only feasible in differential circuits for differential signaling provides a specified signal current return path.

III. CIRCUIT DESIGN

This section details the 60 GHz PA design. The design was implemented in 65 nm bulk CMOS technology with f_T/f_{MAX} of 170/230 GHz. The transistor used in the design is biased at 0.2 mA/μm to maximize the power gain. The schematic of the amplifier is shown in Fig. 6. It consists of two unit PAs and each unit PA has a driver stage and an output stage. The pseudo-differential cascode amplifier is used to extend output voltage swing and improve the stability. The common-gate stage is laid out in close proximity to create a virtual ground at the gate and relax the need for decoupling capacitor. Load-pull simulations are performed for both output and driver stages. The optimum load impedances are then determined to maximize the output power. Even for the differential circuit, the inductance in the ground plane is still problematic when the transistor size goes large as every unit transistor sees different local ground. A 10 pH source degeneration inductance implemented with wide metals is applied to mitigate this problem, as shown in Fig. 7. The source degeneration inductor can be well modeled in the output stage and included in the circuit simulations. Although it reduces the power gain of the amplifier, the source degeneration inductor increases the input impedance of the output stage to ease the interstage matching and reduce the insertion loss of the matching network. The inductor is shielded from the signal path by floating metal strips.

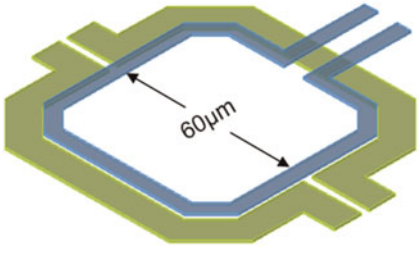

Fig. 4. Overlay transformer-based power combiner.

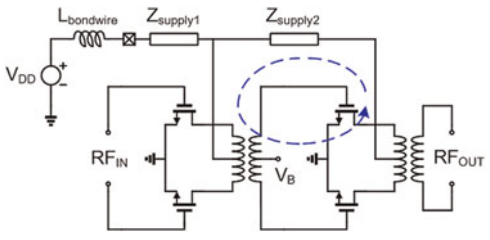

Fig. 5. Two-stage differential PA showing the potential loop for the common-mode instability.

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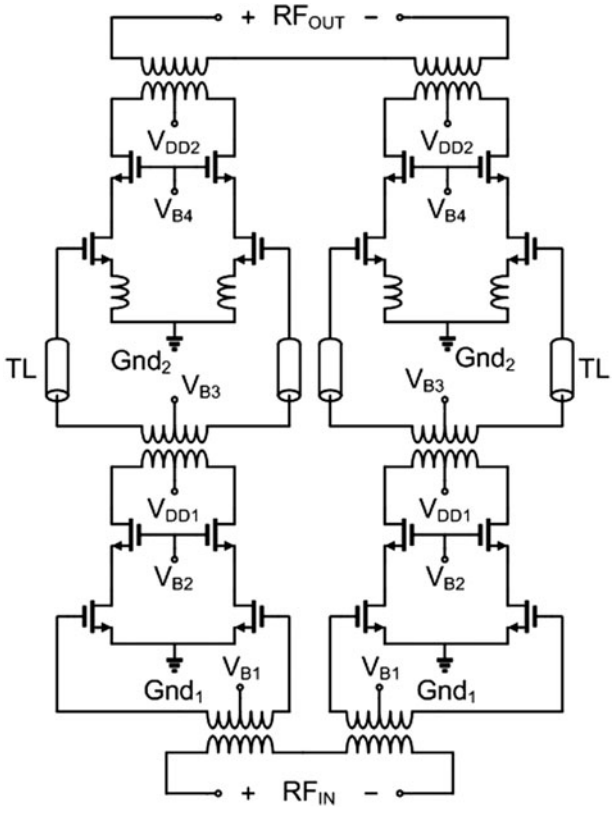

Fig. 6. Simplified schematic of 60 GHz PA.

Compared with the output stage, the driver stage is scaled by a factor of 2.5 in size, which is intended to provide sufficient signal power to drive the output stage.

For the passives, transformer-based structures are extensively employed in order to reduce the chip area. The transformers are implemented in the top two metals (metals 6 and 7). Both metals have the thickness of 0.9 μm and the coupling factor of the transformer is around 0.7, as mentioned in Section II. The input power divider matches the input impedance of the PA to 50 Ω input and provides two pairs of differential signals to the driver stage while the output power combiner sums the power from two unit PAs and transform the 50 Ω load to the optimum load impedance for each PA. A coupling transformer and a slow-wave differential TL [18] are employed for interstage matching network. The adoption of the differential TLs simplifies the transformer design. The

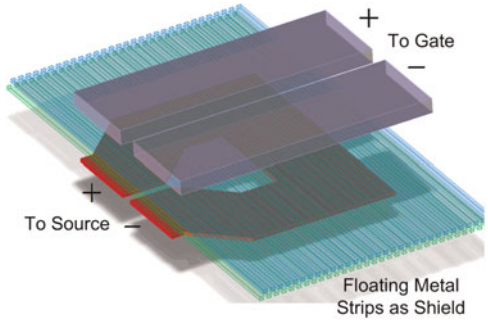

Fig. 7. Source degenerated inductor shielded from the signal path by floating metal strips.

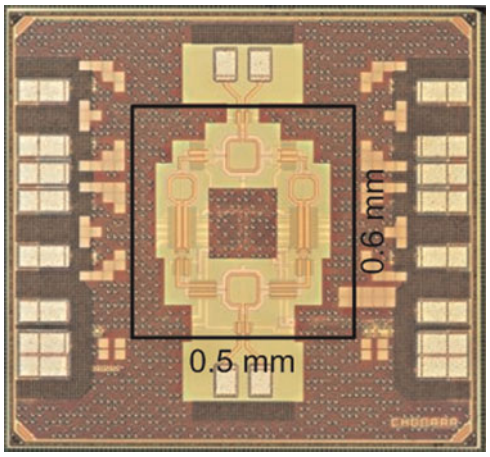

Fig. 8. Microphotograph of the PA testchip.

turn ratio of the transformer is 1:1 and high-power transfer efficiency can then be expected. The floating metal strips are placed beneath the TLs to shield the signal lines from the lossy substrate. The supply and bias lines can also be easily routed under the floating strips without affecting the RF performance. The supply and ground lines of the driver stage and output stage are separated from each other to ensure the stability. The low-Q decoupling capacitors are used for the supply lines to avoid any potential common-mode oscillations.

IV. EXPERIMENTAL RESULTS

The microphotograph of the PA testchip is shown in Fig. 8 with the PA core area of only 0.3 mm^2. The 60 GHz PA was measured via on-wafer probing. Two Model 67A Picoprobe GS/SG Probes were used for the input/output probing. Small signal S-parameter measurements were performed with a 67 GHz Agilent E8361C vector network analyzer. A short-open-load-through calibration method was applied using a separate calibration substrate. The large signal characterization was carried out with a 110 GHz Agilent power meter. The PA consumed 143 mA from a 1.6 V supply voltage at DC.

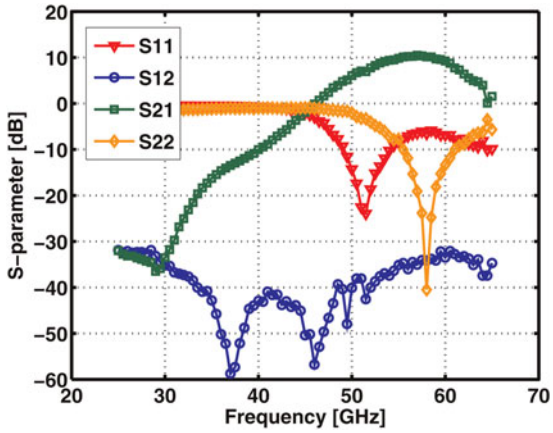

Fig. 9. Measured s-parameter of the PA versus frequency.

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Figure 9 shows small-signal *s*-parameter results of the PA. The PA has a peak small-signal gain S_{21} of 10.2 dB at 58 GHz. The 3-dB bandwidth is around 12 GHz (50–62 GHz). The reverse isolation is better than 33 dB within the measurement frequency range (25–65 GHz). The PA achieves broadband output matching ($S_{22} < -10$ dB) across the entire working frequencies. S_{11} is better than −6.5 dB. Note that the input matching of PA is not as important as the output matching since the PA will be connected to an on-chip up-converter in the transmitter.

Figure 10 illustrates the large signal behavior of the PA at 58 GHz. By increasing the input power, the PA shows an output saturation power (P_{SAT}) of 14 dBm and output 1-dB compression point (P_{O1dB}) of 10.8 dBm. The peak power-added efficiency (PAE) and drain efficiency (DE) are 7.2 and 14.8%, respectively, as shown in Fig. 11. Figure 12 shows the output power variations over the frequency band. A flat P_{O1dB} has been observed between 52 and 60 GHz and the variation is smaller than 1.5 dB. The P_{SAT} is between 12 and 14 dBm from 52 to 61 GHz.

The performance of the PA has also been studied by varying the supply voltage of the driver stage. As shown in Fig. 13, when the supply voltage of the driver stage is swept

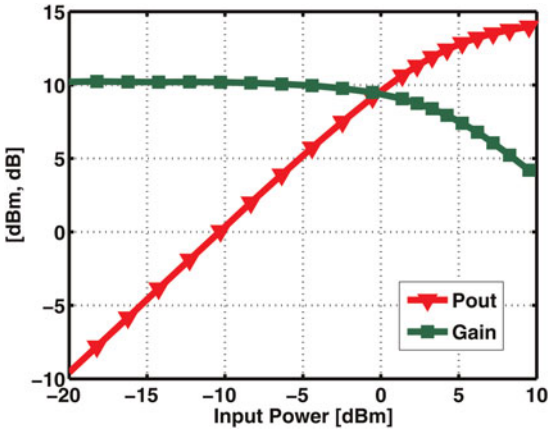

Fig. 10. Measured gain and output power of the PA versus input power at 58 GHz.

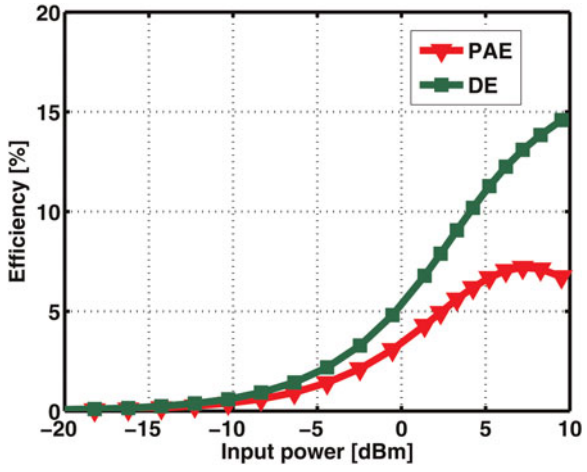

Fig. 11. Measured DE and PAE of the PA versus input power at 58 GHz.

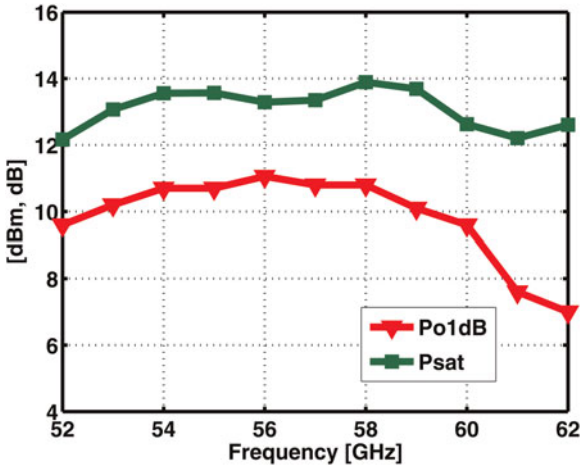

Fig. 12. Measured P_{O1dB} and P_{SAT} of the PA versus frequency.

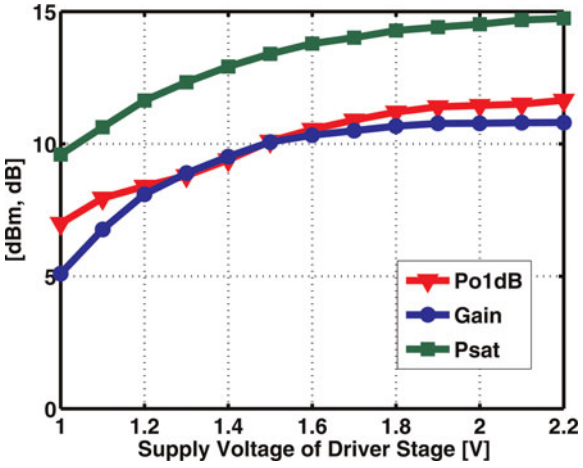

Fig. 13. Measured P_{O1dB}, P_{SAT} and gain of the PA versus the supply voltage of the drain stage at 58 GHz.

from 1 to 2.2 V, P_{O1dB} increases from 7 to 11.8 dBm and P_{SAT} from 9.7 to 14.8 dBm. Similar results were not observed when the supply voltage of the output stage was increased. This indicates that the driver stage is a bit under-designed and output power compression point is limited by the driver stage. It can probably be attributed to the process variations or the inaccurate modeling of the transistor. Better performance can be expected if the high-frequency transistor model is corrected or the size of the driver stage is increased so that enough power can be delivered to the output stage.

Table 1 compares the performance of this PA with recent published 60 GHz CMOS PAs. These amplifiers employ either CS or cascode topologies. Most designs use a differential (Diff.) configuration due to its advantages over the single-ended (Sing.) circuit at mm-wave frequencies. This work, [6, 7, 10], uses transformers for the matching networks to permit compact layouts. Power combining (PC) techniques are exploited in this work and [9] to achieve saturated output powers of 14.8 and 19.9 dBm, respectively. However, [9] uses four-way Wilkinson power combiners and thus consumes relatively large chip area. From this comparison, it can

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Table 1. 60 GHz CMOS power amplifiers' performance comparison.

Reference (Tech.)	Gain (dB)	P_{O1dB} (dBm)	P_{SAT} (dBm)	PAE_{MAX} (%)	Supply (V)	$Area_{Core}$ (mm^2)	Topology
This work (65 nm)	10.2/10.8*	10.8/11.8*	14/14.8*	7.2	1.6	0.3	Two-stage Cascode, Diff., PC
[6] (90 nm)	5.5	9	12.3	8.8	1	0.25	Two-stage CS, Diff.
[7] (90 nm)	15.4	2.5	11.5	11	1	0.053	Three-stage CS, Diff.
[8] (65 nm SOI)	14	7.1	10.5	22.3	1.2	0.57	Two-stage Cascode, Sing.
[9] (90 nm)	20.6	18.2	19.9	14.2	1.2	1.1†	Four-stage CS, Sing., PC
[10] (65 nm)	30	6.8	10.6	18	1	0.053	Three-stage CS, Diff.

*2.2 V supply voltage is applied to the driver stage.
†Core area of the PA is calculated based on the dimensions of the chip.

also be noticed that the PA implemented in CMOS-SOI [8] stands out with the highest PAE as the losses of the passives are smaller.

V. CONCLUSION

A 60 GHz PA was designed using 65 nm bulk CMOS technology. To overcome the low breakdown voltage of the transistor in nanometer CMOS technology, the power combining technique and cascode amplifier were used to maximize the output power. Cascode topology can also improve the reserve isolation and ensure the stability. Differential signaling was employed to mitigate the parasitic inductance in the ground plane and allow the ground separation between the driver stage and output stage. Transformer-based passives were extensively employed in the design to realize high-efficiency matching networks and permitted a compact layout. The PA prototype achieves a small signal gain of 10.2 dB with a 3 dB bandwidth of 9 GHz. The maximum saturated output power is 14.8 dBm with a peak PAE of 7.2%. The reverse isolation is better than −33 dB across the working frequencies.

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REFERENCES

[1] IEEE 802.15 Working Group: Wireless PAN Task Group 3c. Millimeter wave alternative PHY [Online], 2009. Available: http://www.ieee802.org/15/pub/TG3c.html.

[2] IEEE 802.11 Working Group: Very high throughput in 60 GHz [Online]. Available: http://www.ieee802.org/11/Reports/tgad_update.htm.

[3] Wireless Gigabit Alliance: WiGig White Paper [Online]. Available: http://wirelessgigabitalliance.org/specifications/.

[4] Doan, C.H.; Emami, S.; Niknejad, A.M.; Brodersen, R.W.: Millimeter-wave CMOS design. IEEE J. Solid-State Circuits, **40** (2005), 144–155.

[5] Razavi, B.: A millimeter-wave CMOS heterodyne receiver with on-chip LO and divider. IEEE J. Solid-State Circuits, **43** (2008), 477–485.

[6] Chowdhury, D.; Reynaert, P.; Niknejad, A.M.: A 60 GHz 1 V + 12.3dBm transformer-coupled wideband PA in 90 nm CMOS, in ISSCC Dig. Tech. Papers, San Francisco, 2008.

[7] Chan, W.L.; Long, J.R.; Spirito, M.; Pekarik, J.J.: A 60 GHz-band 1 V 11.5dBm power amplifier with 11% PAE in 65 nm CMOS, in ISSCC Dig. Tech. Papers, San Francisco, 2009.

[8] Siligaris, A. et al.: A 60 GHz power amplifier with 14.5dBm saturation power and 25% peak PAE in CMOS 65 nm SOI, in Proc. of ESSCIRC, Athens, 2009.

[9] Law, C.; Pham, A.: A high-gain 60 GHz power amplifier with 20dBm output power in 90 nm CMOS, in ISSCC Dig. Tech. Papers, San Francisco, 2010.

[10] Boers, M.: A 60 GHz transformer coupled amplifier in 65 nm digital CMOS, in Proc. of RFIC, Anaheim, 2010.

[11] Reynaert, P.; Niknejad, A.M.: Power combining techniques for RF and mm-wave CMOS power amplifiers, in Proc. of ESSCIRC, Munich, 2007.

[12] Law, C.Y.; Pham, A.V.: A high-gain 60 GHz power amplifier with 20dBm output power in 90 nm CMOS, in ISSCC Dig. Tech. Papers, San Francisco, 2010.

[13] He, Y.; Li, L.; Reynaert, P.: 60 GHz power amplifier with distributed active transformer and local feedback, in Proc. of ESSCIRC, Sevilla, 2010.

[14] Aoki, I. et al.: A fully-integrated quad-band GSM/GPRS CMOS power amplifier. IEEE J. Solid-State Circuits, **43** (2008), 2747–2758.

[15] Stephens, D.; Vanhoucke, T.; Donkers, J.: RF reliability of short channel NMOS devices, in Proc. of RFIC, Boston, 2009.

[16] Aoki, I.; Kee, S.D.; Rutledge, D.B.; Hajimiri, A.: Fully integrated CMOS power amplifier design using the distributed active-transformer architecture. IEEE J. Solid-State Circuits, **37** (2002), 371–383.

[17] Cheung, T.S.D.; Long, J.R.: A 21–26-GHz SiGe bipolar power amplifier MMIC. IEEE J. Solid-State Circuits, **40** (2005), 2583–2597.

[18] Cheung, T.S.D.; Long, J.R.: Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits. IEEE J. Solid-State Circuits, **41** (2006), 1183–1200.

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