International Journal of Microwave and Wireless Technologies, 2011, 3(2), 179–188.
doi:10.1017/S1759078711000213

Millimeter-wave antenna designs for 60 GHz applications: SoC and SiP approaches

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Antenna on chip (AoC) and antenna in package (AiP) solutions for millimeter-wave (mmWave) applications and their characterization are presented in this paper. Antenna integration on low resistivity (LR) and high resistivity (HR) silicon substrate are expected. And, in a packaging approach, the combination of antenna on silicon with a material, which has the effect of a "lens", allowing increasing gain is presented. In a second part, to satisfy beamforming capabilities, a hybrid integration of the antenna on silicon and glass substrates is proposed.

Keywords: Antenna Design, Modelling and Measurements, Antennas and Propagation for Wireless Systems

Received 30 October 2010; Revised 1 February 2011; first published online 18 March 2011

I. INTRODUCTION

At millimeter-wave (mmWave) frequencies, high data rate applications such as kiosk downloading or Wireless-High Definition Multimedia Interface (W-HDMI) require low-cost and low-power systems on chip (SoC) to address mass-market products and consumer expectations. Thanks to the recent progress of integrated circuits (ICs) on Complementary Metal Oxyde Semi-conductor (CMOS) or Bipolar-Complementary Metal Oxyde Semi-conductor (BiCMOS) silicon technologies, the complete integration of the radio-frequency (RF) front-end (FE) on a single chip is now achievable [1–3], except for the antenna that remains usually off-chip. Therefore, the last challenge is the antenna integration. The antenna specifications depend on the targeted applications. For kiosk-file downloading applications (usage model 5 for IEEE-802.15.3c [4]), line-of-sight configuration is considered on a limited distance (<3 m). So, a 5 dBi gain is typically required. For wireless HDMI application (usage model 1 for IEEE-802.15.3c), a non-line-of-sight configuration is recommended over a 10 m maximum distance. In that case, a 14 dBi gain is expected, with beamforming capabilities for enhancing the link budget and preventing multipath effects generated by human presence and environment.

MmWave antennas suffer from their integration on lossy silicon substrate. Due to the low resistivity (LR) silicon substrate characteristics (dielectric constant, loss tangent, and thickness), integrated antennas exhibit quite low gain and reduced radiation efficiency [5, 6]. Using a high resistivity (HR) silicon technology contributes to improve performances, thanks to a reduced part of the energy previously dissipated in the lossy substrate (when LR silicon substrate is considered). Thus, an HR silicon-on-insulator (SOI) CMOS integrated RF FE, including a silicon integrated antenna, has been demonstrated [7]. So, in order to propose a high-performance low-cost SoC, a co-integration of the antenna and ICs can be proposed on HR SOI CMOS.

Nevertheless, for mmWave applications requiring beamforming, the design of a passive antenna array on Si suffers from high insertion losses into the planar feeding network. Therefore, the hybrid integration of the antenna on an additional substrate appears as a disruptive issue, exploiting packaging and coupling possibilities within such confined environment.

So, we propose two research axes to develop antenna solutions for mmWave applications under low-cost considerations: antenna design on silicon substrate (antenna on chip) and hybrid antenna design (antenna in package).

In the first section, we first describe two different test benches that we have developed in order to perform return loss and radiation pattern measurements of such mmWave integrated antennas. Indeed, accurate and reliable antenna characterization procedures are preliminary and fundamental steps in order to properly evaluate such antennas, and to accurately identify performances enhancement. In the second part, the design of integrated antennas on both LR and HR SOI substrates are investigated and associated performances are shown. In the third part, the hybrid integration of the antenna is described.

II. MMWAVE TEST BENCHES

A) STMicroelectronics test bench

In [8], we have described a measurement setup dedicated to the full characterization of silicon integrated antennas. The anechoic chamber is able to address radiation pattern and gain measurements as well as return loss extraction as far as an appropriate calibration technique is applied. Antennas

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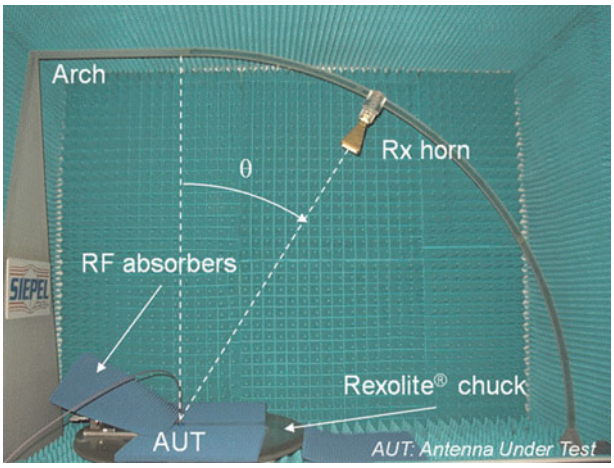

Fig. 1. STMicroelectronics measurement setup for gain characterization.

integrated on LR and HR silicon substrates have been characterized and their radiation patterns determined in both *E*- and *H*-planes. The gain extraction procedure has been completed. A picture of the measurement setup is presented in Fig. 1.

B) Lab-STICC test bench

At Lab-STICC laboratory (www.lab-sticc.fr), direct on-wafer measurement procedures are considered for accessing to return loss, gain, and radiation pattern measurements, using a probe station. For the radiation measurements, an open waveguide is used to respect far field conditions with quite a low distance in order to increase measurement dynamic range and to reduce the impact of the environment (parasitic reflection on probe and metallic parts) (Fig. 2). The distance between the reference antenna and the antenna under test is 5 cm. For the radiation pattern measurements, an arch has been realized in an electrically transparent foam material ($\varepsilon_r = 1.07$, tg $\delta = 0.003$ at 60 GHz). The reference antenna is inserted in a holding device made of foam and moved along the arch to acquire the complete radiation pattern (Fig. 3).

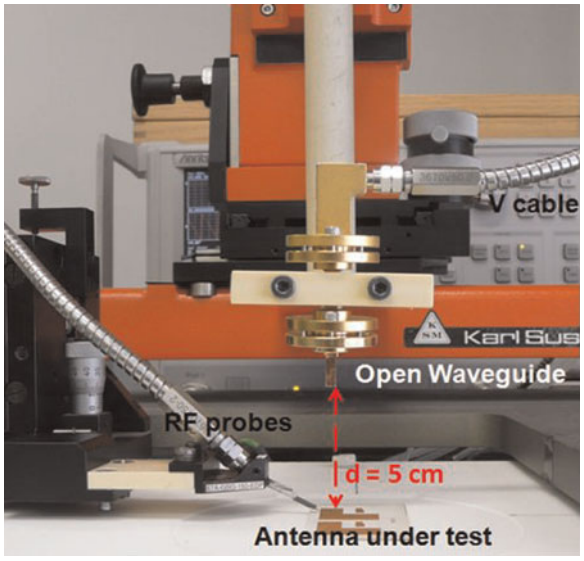

Fig. 2. Lab-STICC measurement setup for gain characterization.

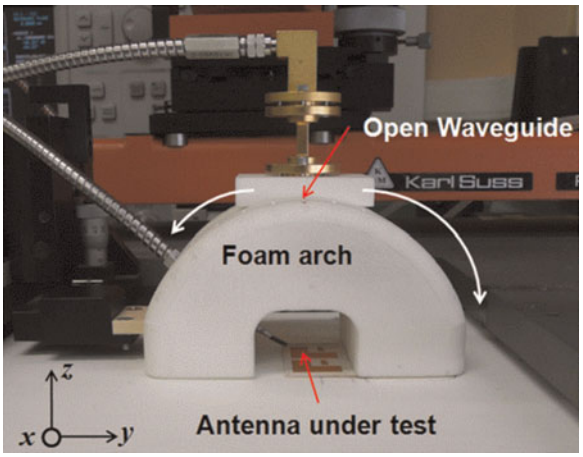

Fig. 3. Lab-STICC measurement setup for radiation pattern characterization.

These two test benches are complementary due to their different measurement environment. All measurements present in this paper are obtained from these test benches.

III. ANTENNA ON CHIP

Transition frequencies of transistors in silicon-based technologies have reached performances that enable those technologies to address mmWave applications such as 60 GHz W-HDMI, 77 GHz automotive radar, 94 GHz passive imaging, etc. With the increase of the frequency, and especially at mmWave frequencies, losses are limiting factors in the design of high-performance circuits and especially in RF FEs. These losses mostly come from passive devices (transmission lines, inductors), but are also due to packaging or assembly techniques (wire-bonds, flip-chip bumps).

With the previous concerns about losses, one can understand the benefit of the integration of the antenna along with the RF FE on the same substrate, in a standard silicon technology. Indeed, losses in the assembly of an external antenna can therefore be suppressed, or at least significantly reduced (as well as additional assembly costs). Furthermore, if the antenna is directly matched to the input – respectively output – impedance of a low noise amplifier (LNA) – respectively a power amplifier (PA), these losses can be minimized. Figure 4 illustrates the concept of such a co-integration technique for a receiving mode configuration in a SoC approach.

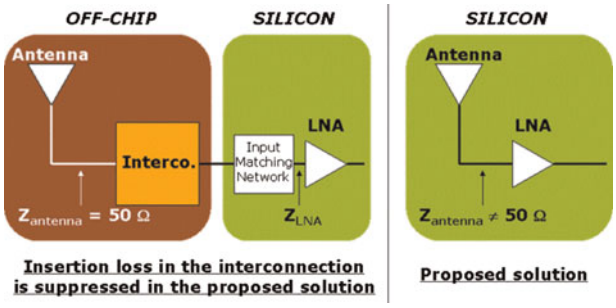

Fig. 4. Co-integration technique in an SoC approach.

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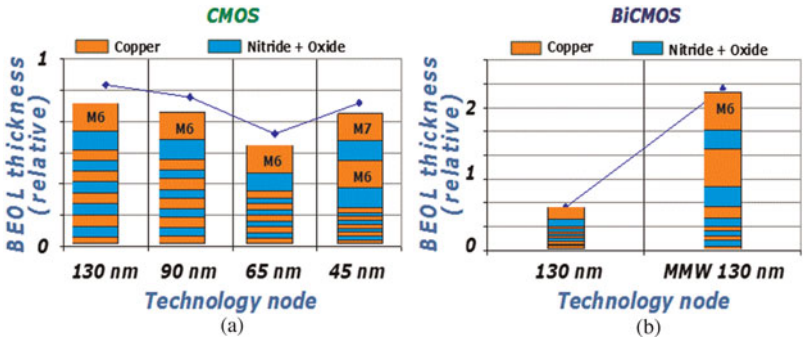

Fig. 5. BEOL in (a) CMOS and (b) BiCMOS processes.

The other benefit of integrating the antenna lies in the reduction of the size of the whole system, provided that the application targets short-range application with reduced gain expectation for both the LNA (or the PA) and the antenna.

In standard silicon technologies, the antenna can be designed using the metal layers of the back-end-of-line (BEOL), already used for the integration of passive devices such as metal–insulator–metal and metal–oxide–metal capacitors, inductances, or transmission lines. The BEOL is composed of dielectric and metal layers. In Fig. 5 are presented the BEOL of few technologies on standard CMOS and BiCMOS processes from STMicroelectronics. BEOL thickness is presented in a relative scale. A minimum of six metal layers, and more in the latest advanced technology nodes, are achieved on the top of the silicon substrate. A mmWave dedicated BiCMOS BEOL has been developed (Fig. 5(b)) with a total height reaching twice the value typically considered in standard CMOS process, enabling the design of high-performance passive devices (and especially mmWave ones) [9]. The BEOL is stacked on the substrate which can be either a LR bulk or HR silicon substrate (Fig. 6). HR substrate is compatible with SOI technology and passive filters in coplanar waveguide (CPW) topology have already been reported in such SOI technology with very good performances up to 325 GHz [10].

A) Elementary antenna

Due to the LR, integrated antennas on bulk (LR) silicon substrates exhibit low radiation efficiency. Several manufacturing techniques can be used to increase the efficiency such as silicon removal with micromachining [11], local resistivity increase with proton-implant [12], or thick benzo-cyclobuthen coating (above-IC process) [5]. But for industrial reasons, we focus our studies on the integration of antennas on standard silicon processes. Furthermore, our designs meet fabrication constraints in terms of metal density across the chip (20% < density < 80%). To do so, metal dummies are placed inside the structures and specific zones are dummies excluded.

Another parameter that can influence the antenna performance on LR silicon substrate is the substrate height. Indeed, the silicon die is usually thinned when inserted inside a package. Then, we have investigated the impact of the substrate height (h_sub) on the performance of a simple

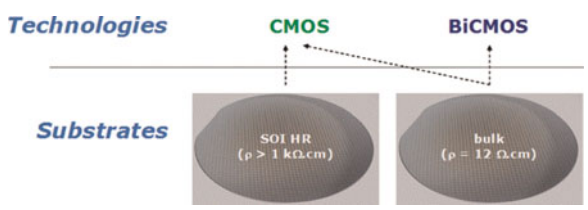

Fig. 6. HR and LR substrates available in silicon technologies.

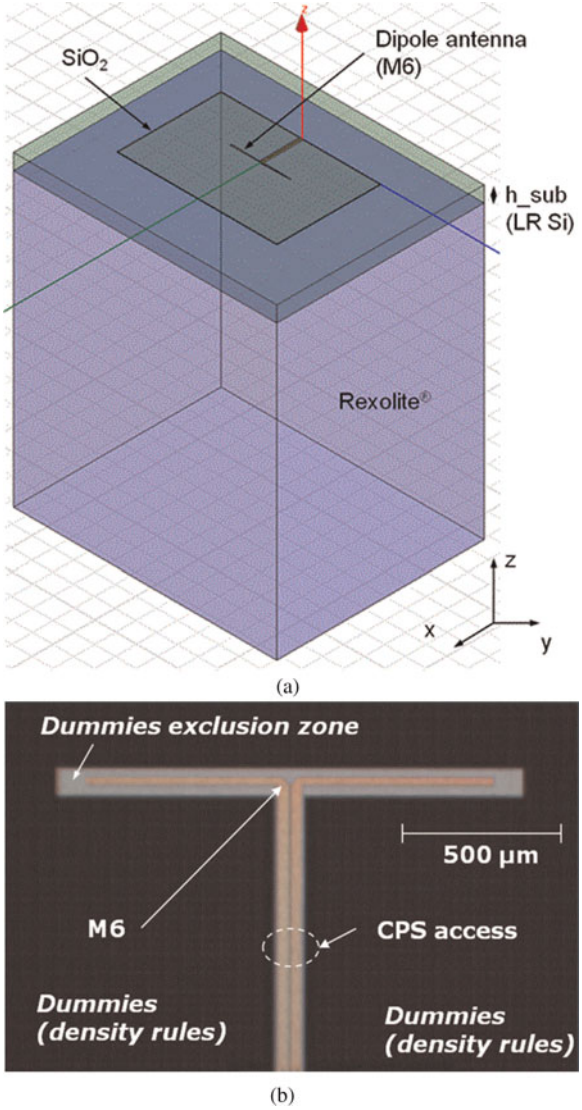

Fig. 7. Dipole antenna integrated on a LR substrate (a) model, and (b) microphotograph of the integrated antenna.

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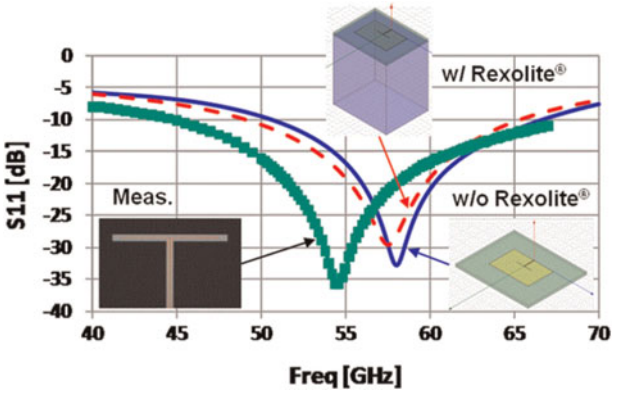

Fig. 8. Comparison of $S11$ for two configurations (w/ and w/o Rexolite®) and measurement.

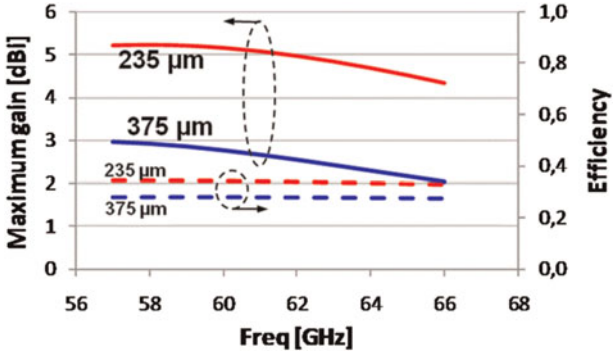

Fig. 10. Maximum gain and efficiency versus frequency.

dipole antenna integrated on a LR silicon substrate (Fig. 7). The antenna is built using the sixth metal layer (M6) of the BiCMOS MMW 130 nm technology from STMicroelectronics. The same antenna has been simulated and measured on different substrates with respective heights of 375 and 235 µm. The simulation has been performed using Ansoft HFSS™. In our model, we take into account the material on top of which is placed the antenna for the radiation pattern measurement (Rexolite® with a relative permittivity of 2.53). The effect of Rexolite® is a reasonable 5% shift of the resonant frequency to a lower value as shown in Fig. 8.

Because of the high permittivity substrate ($\varepsilon_{Si} = 11.7$), most of the energy is radiated through the silicon (along the negative direction $z < 0$). In Fig. 9, the gain values (E-plane) in $\theta = 0^\circ$ (azimuth position) and $\theta = 180^\circ$ are, respectively, -3.2 and -2.4 dBi. On the other hand, our current measurement setup allows for measurement in the upper hemisphere of the antenna ($z > 0$). So, we have simulated the maximum realized gain versus the frequency in the band of interest [57–66 GHz]. This maximum gain is achieved in the $\theta = 175$ and 173° directions, for the antenna on a substrate with a height of 375 and 235 µm, respectively. Figure 10 presents the simulation results of the maximum gain and the efficiency of both antennas. The radiation efficiency is increased from 28% (h_sub = 375 µm) to 34% (h_sub = 235 µm) on the whole frequency band. The maximum gain in their respective direction is also increased from 2.7 dBi (h_sub = 375 µm) to 5.2 dBi (h_sub = 235 µm) at 60 GHz.

The classical toroidal-shape radiation pattern of a dipole is heavily modified by the presence of the Rexolite® underneath the antenna (Fig. 11). In addition, the discrepancies observed between measurement and simulation results are also explained by the surrounding environment of the antenna, i.e. the proximity effects of the elements near the antenna (mainly the probe and the cable) used by the measurement setup. The substrate delimitations have also incidence in the radiation pattern degradations for low-elevation angle directions (Fig. 12).

The gain is also increased in the upper ($z > 0$) hemisphere but to a lower extent. A comparison between measured and simulated maximum gain at 60 GHz is provided in Table 1. The measured maximum gain is in the order of magnitude of the simulated value but the increase of the gain remains in the measurement error admitted for the setup.

To provide deeper insights of the dipole topology integrated on silicon substrate, we have also simulated the antenna on a 235 µm-height HR silicon substrate. The maximum gain and radiation efficiency are increased to

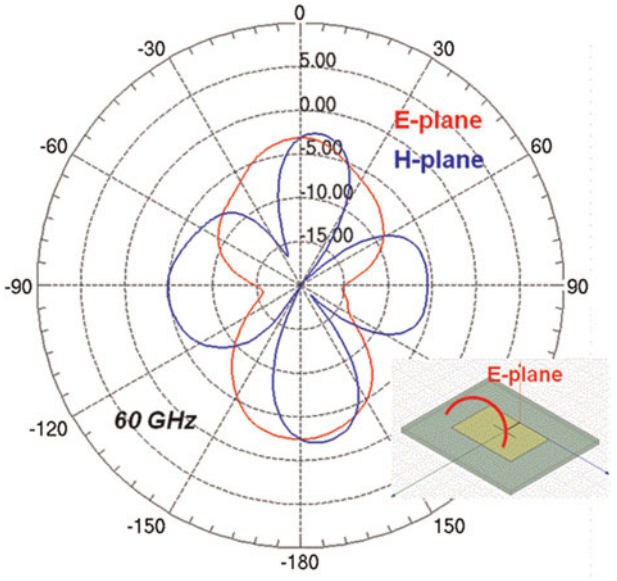

Fig. 9. Simulated radiation pattern of the standalone antenna at 60 GHz.

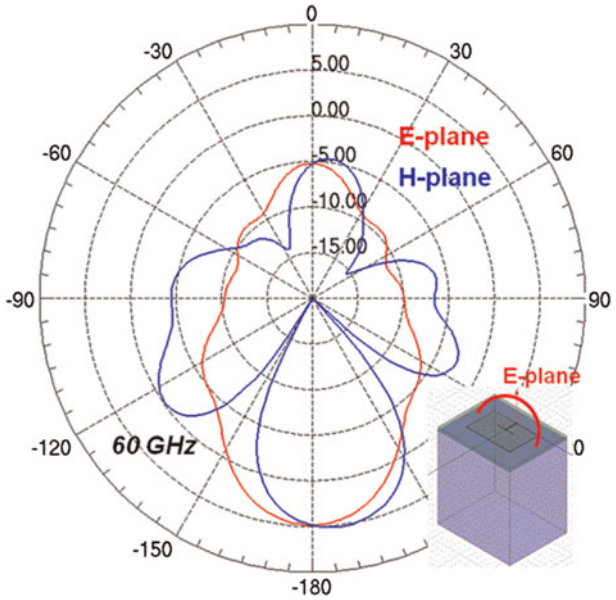

Fig. 11. Simulated radiation pattern of the antenna with Rexolite® at 60 GHz.

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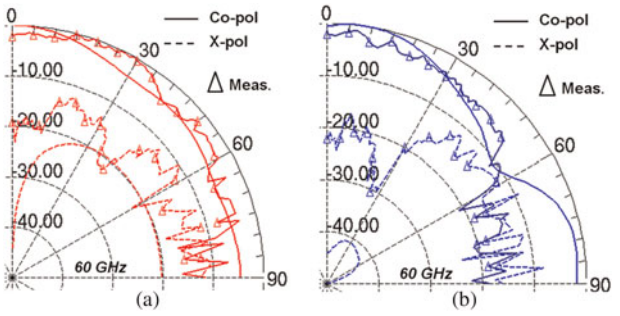

Fig. 12. Measured and simulated radiation pattern of the dipole antenna on 235 μm-height substrate: (a) *E*-plane and (b) *H*-plane.

7.7 dBi ($\theta = 172°$) and 90% at 60 GHz, respectively. The maximum gain in the $z > 0$ hemisphere is −0.5 dBi ($\theta = 12°$) at 60 GHz.

Finally, another antenna topology has been implemented on a 375 μm-height HR silicon: a folded-slot antenna with a 50 Ω CPW transmission line feeding the resonant structure (Fig. 13) [8]. A comparison between simulation and measurement is shown in Fig. 14 for the $|S11|$ dB parameter. A wide impedance matching is achieved from 55 GHz to more than 70 GHz, considering VSWR < 2. For this antenna, the maximum measured gain is −0.4 dBi at 60 GHz in the $z > 0$ hemisphere.

Considering these measurement results in the $z > 0$ hemisphere, we can expect comparable results on the substrate side ($z < 0$) concerning maximum gain value measurements. At simulation level, we can compare the radiation pattern of the antenna with different substrate size and we can also take into account the material placed below the substrate.

B) Fully integrated mmWave FE module and technological opportunities

Up to now, the antenna is considered as a standalone component. To go further toward a fully integrated approach, the antenna will be integrated in a whole die (co-integrated to the mmWave FE). The integration under industrial conditions is a big concern and the antenna cannot be designed without considering the whole circuit to prevent from parasitic coupling and metallization parts delimitations. The die will be packaged and the assembly strategy must take into account all the advantages we have seen so far:

— more energy radiated through the silicon ($\varepsilon_r = 11.7$),
— lower loss on HR silicon (HR SOI technology),
— low permittivity material used as a lens below the silicon substrate (low permittivity material).

Therefore, in terms of integration scheme, we can foresee the dipole antenna on LR silicon substrate with the use of a material that has the effect of a "lens" (Fig. 15).

Table 1. Maximum realized gain comparison in $z > 0$ hemisphere: measurement and simulation results.

Substrate height (μm)	Simulated maximum gain (dBi)	Measured maximum gain (dBi)
375	−7.5 at $\theta = 30°$ (*H*-plane)	−9.6 at $\theta = 28°$ (*E*-plane)
235	−6.6 at $\theta = 12°$ (*H*-plane)	−9.1 at $\theta = 15°$ (*E*-plane)

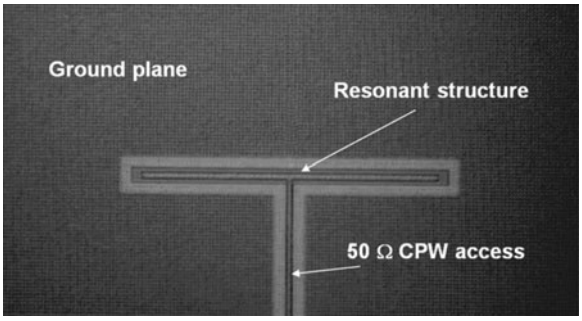

Fig. 13. Folded-slot antenna on a HR silicon substrate.

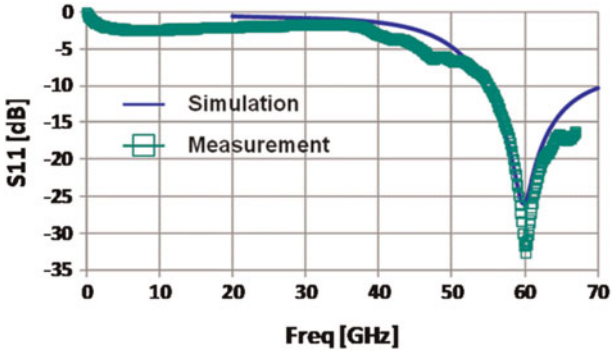

Fig. 14. Folded-slot antenna matching.

A simplified antenna model has been simulated and we have varied the lens material height placed under the Si substrate from 3 to 7 mm. A maximum 6 dBi gain can be reached using a 7 mm-height material with a permittivity of 2.53) (Table 2).

For integration purpose, one can understand that a low profile material is preferred. As a matter of fact, we have varied the permittivity for a 3 mm-height material. The results are presented in Fig. 16. The highest maximum realized gain is achieved using an intermediary permittivity $\varepsilon_r = 5.5$ typically corresponding to glass material.

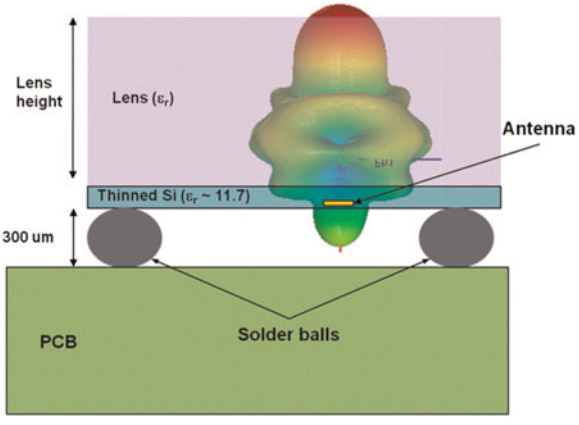

Fig. 15. Integration with a lens.

Table 2. Maximum realized gain of the antenna with a lens.

Lens height	3 mm	5 mm	7 mm
Maximum realized gain (dBi)	0.9	2.3	6.0

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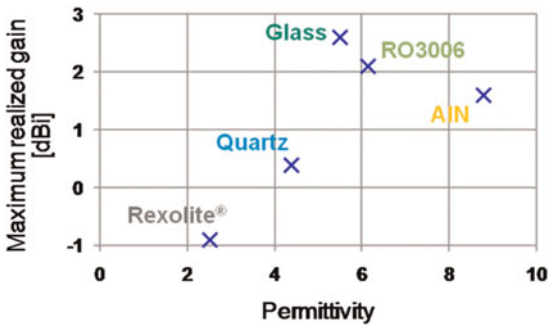

Fig. 16. Maximum realized gain versus "lens" material permittivity with 3 mm height.

At industrial scale, molding materials have a permittivity around 4. In a more complex but industrial process, a glass wafer can be sealed directly to the silicon substrate side by layer transfer technology [13], after having thinned the silicon substrate.

These results emphasize the fact that the antenna has to be designed in close relation with its environment: the antenna will be co-designed and co-integrated with the circuit and the environment.

IV. HYBRID ANTENNA

The targeted W-HDMI applications induce drastic specifications on the link budget, and therefore quite high-gain values for the antenna, with potentially beamforming capabilities depending on the considered usage model. As a consequence, an antenna array is necessary. The implementation of antenna array on Si is not appropriate because of the high insertion losses of planar distributing network on Si. Thus, in complement to the previous proposed Si + lens configuration for a standalone antenna on Si, a hybrid integration technique appears as a good trade-off to associate radiation elements and reduced loss feeding structures on an

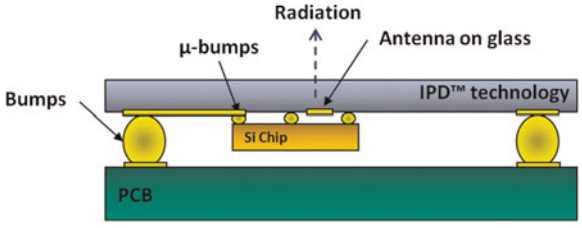

Fig. 17. Side view of the mmWave package with the Si-IPD™ packed antenna.

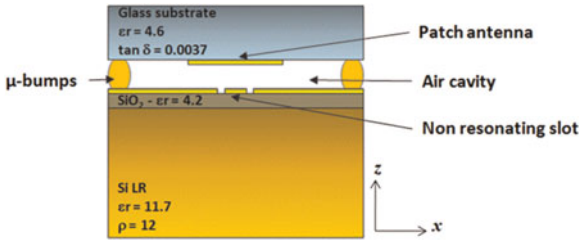

Fig. 18. Side view of the Si-IPD™ packed antenna.

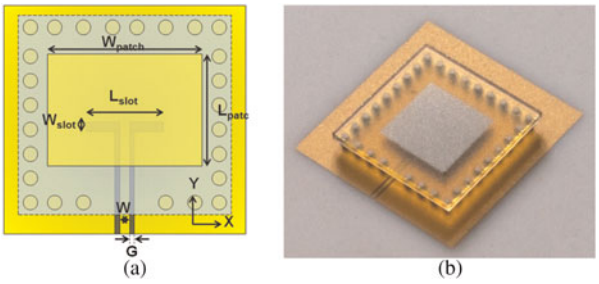

Fig. 19. Top view of the Si-IPD™ packaged antenna (a) and photo of a patch antenna on IPD™ mounting (b).

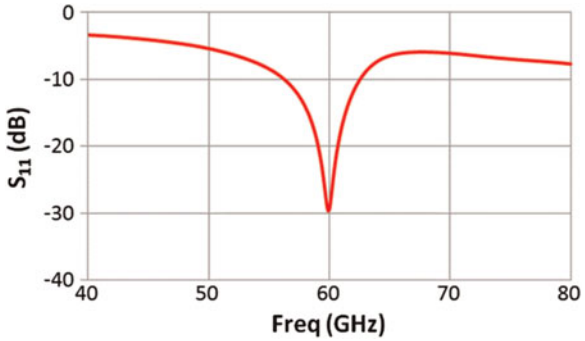

Fig. 20. Simulated return loss of the Si-IPD antenna.

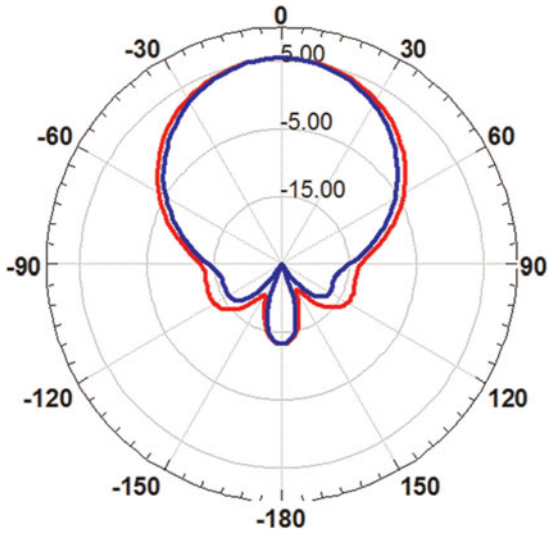

Fig. 21. Simulated radiations patterns at 60 GHz: *E* (blue) and *H* (red) planes.

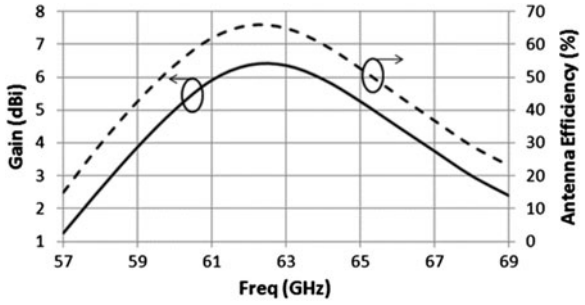

Fig. 22. Simulated gain and antenna efficiency versus frequency in $z>0$ (LR Si).

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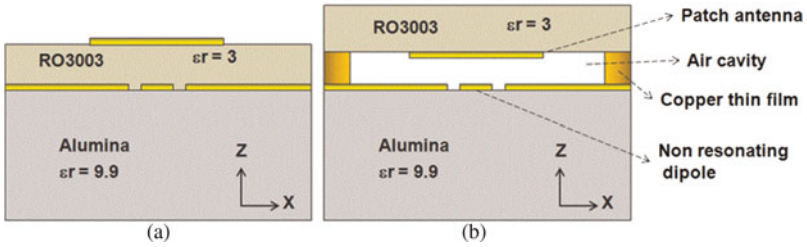

Fig. 23. Side view of the different packaged Alumina-RO3003 antenna configurations: without (a) and with intermediate air cavity (b).

Table 3. Bandwidth result summary.

Antenna	Air cavity height (μm)	Bandwidth (GHz)	
		Simulation	Measure
a	–	2,5	2,45
b	75	3,7	4
c	125	5	5,3
d	250	10	8,7

appropriate passive circuit supporting material, like glass substrate or fused silica [14–16]. A low-cost solution is to use the IPD^{TM} technology (glass substrate) like an Interposer [17] to make the interface between PCB and RF FE on silicon substrate and report the antenna part (Fig. 17).

A) Elementary antenna

The challenge of the hybrid integration is the interconnection between the IC chip and the antenna part. The different proposed interconnection solutions generate insertion losses or impedance mismatches. So, we propose an alternative approach where the antenna is electromagnetically excited by a primary source directly implemented on the Si-chip. The radiating patch is implemented on the bottom face of the IPD^{TM} material and the non-resonating coupling slot is located on the M6 metallization layer of the standard BEOL of the technology (Fig. 18). For characterization purpose, the glass substrate ($\varepsilon_r = 4.6$, $h = 300$ μm) is mounted by flip chip technique on the silicon chip. The air gap located between the coupling slot and the patch is related to the bumps height (height = 100 μm after assembly), which are properly well-controlled (height ± 5 μm).

The ground of the CPW transmission lines and the coupling slot is assumed as the ground plane of the patch. Besides, the input slot impedance can be modified according to the PA output or LNA input impedance. Therefore, the antenna is perfectly inserted in this equivalent package, and ready to be optimally interface with actives elements.

A first design of the coupling slot integrated on a BiCMOS process (LR Si – 12 Ω cm) from STMicroelectronics is proposed hereafter. The non-resonating slot is excited with a 50 Ω CPW line ($W = 30$ μm, $G = 9$ μm) and its dimensions are as follow: length $L_{slot} = 980$ μm, width $W_{slot} = 20$ μm. The slot is centered under the upper patch and is optimized in order to have the optimal magnetic coupling with the upper rectangular patch (length $L_{patch} = 1.71$ mm, width $W_{patch} = 2.05$ mm). The proposed antenna is presented in Fig. 19.

A first simulation on HFSS^{TM} leads to a 30 dB return loss at 60 GHz, and a 10.8% relative bandwidth ar VSWR = 2 (56–62.5 GHz) (Fig. 20). This antenna presents a gain of 5 dBi

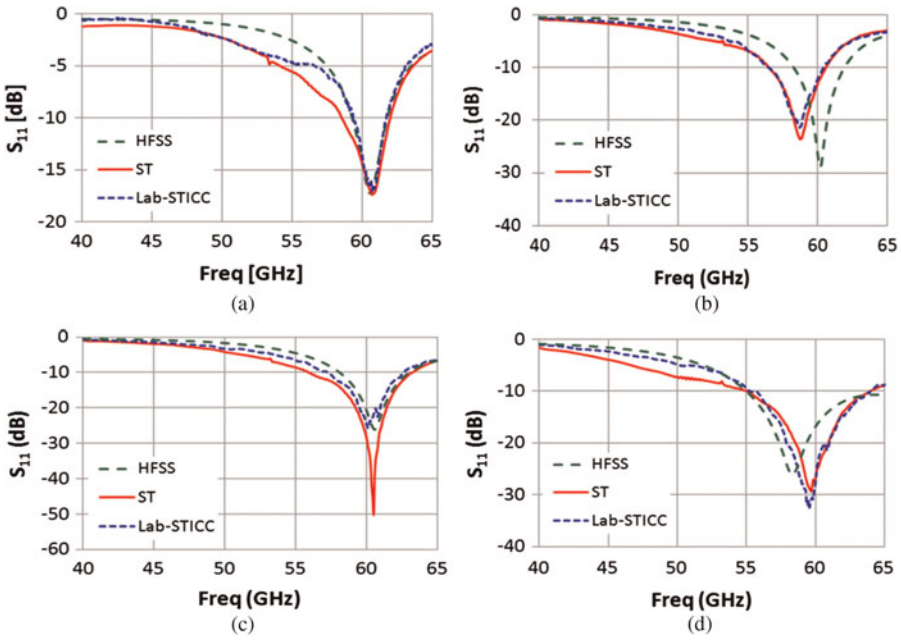

Fig. 24. Simulated and measured return losses of the different packaged Alumina-RO3003 antenna configurations.

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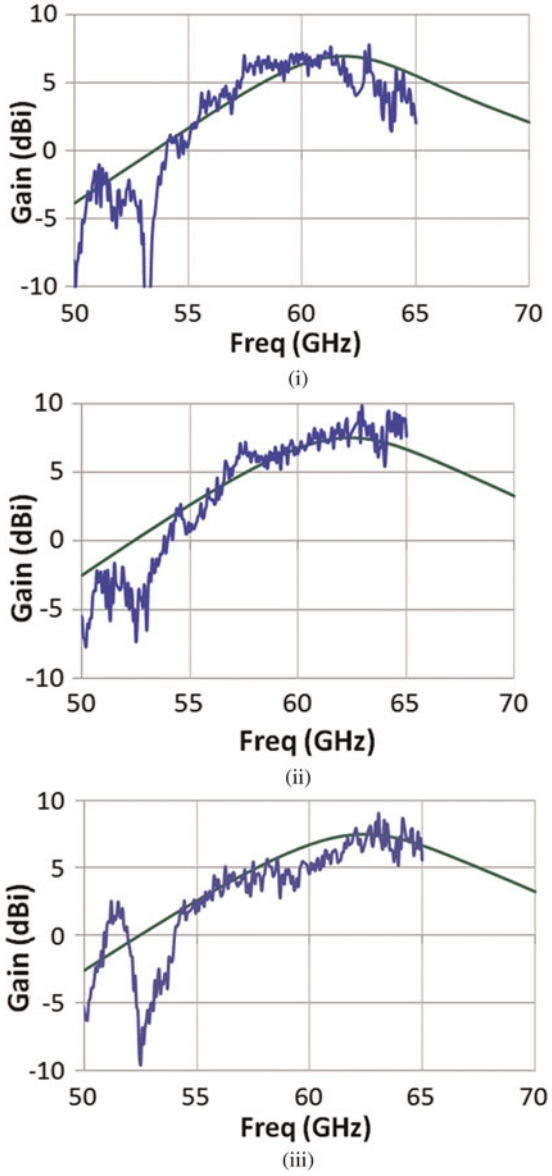

Fig. 25. Measured and simulated gain versus frequency for three cavity heights: $h = 75$ μm (i); $h = 125$ μm (ii); and $h = 250$ μm (iii).

and an *F*/*B* ratio of 17.5 dB at 60 GHz (Fig. 21). We obtain 55 and 66° half-power beamwidths for the *E*- and *H*-planes, respectively.

In Fig. 22, the simulated gain versus frequency is presented. The antenna achieves a gain greater than 5 dBi over a 5 GHz bandwidth [60–65 GHz] with a radiation efficiency of 53.7%

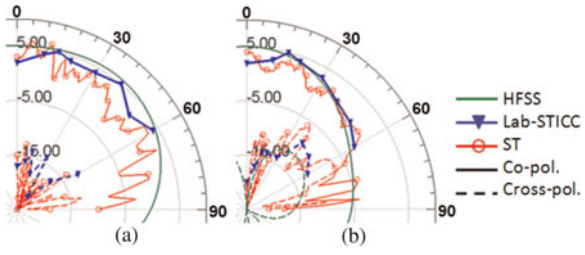

Fig. 26. Simulated and measured radiation pattern for the antenna without air cavity: *E*-plane (a) and *H*-plane (b).

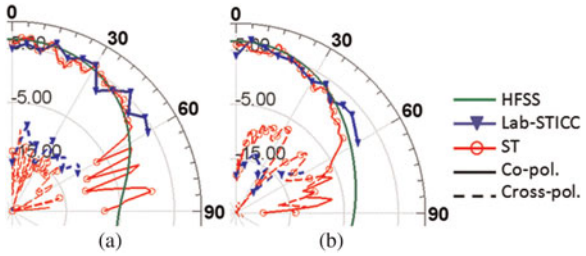

Fig. 27. Simulated and measured radiation pattern for the antenna with an air cavity of 125 μm: *E*plane (a) and *H*-plane (b).

at 60 GHz. This limited efficiency is due to the LR of the silicon substrate. Indeed, the electromagnetic coupling between the slot dipole and the rectangular patch is not optimal because of the absorbed energy by this lossy substrate. Antenna on HR Si (SOI CMOS technology) leads to a 90% radiation efficiency, with a 7 dBi simulated gain at 60 GHz.

B) Validation concept – measurements

Accessing to the optimal coupling between a primary source and a radiation patch structure integrated on high ε_r and low ε_r high Q substrates, respectively, appears as the main challenge for the proposed hybrid packaged antenna. Thus, experimental procedures have been conducted to validate this concept. The slot dipole is implemented on an alumina substrate ($\varepsilon_r = 9.9$, $\tan\delta = 0.004$, thickness $h = 381$ μm) reproducing quite accurately the Si support, while the rectangular patch is processed on a Duroïd RO3003™ substrate ($\varepsilon_r = 3$, thickness $h = 127$ μm). Different configurations are studied and proposed in this paper (Fig. 23) in order to compare bandwidth, gain, and efficiency performances.

A preliminary antenna is designed without intermediary air cavity between overlaid alumina and Duroïd substrates. The patch is printed on the upper face of the RO3003 material (Fig. 23(a)). Three other configurations are studied (Fig. 23(b)), where the patch is printed on the lower face of the Duroïd with different air cavity heights (75, 125, and 250 μm).

All antennas are excited with a 50 Ωcoplanar (CPW) line ($W = 70$ μm, $G = 40$ μm) and characterized with the two test benches in the [50–65 GHz] frequency range. Simulated and measured return losses are reported in Table 3 and presented in Fig. 24.

A quite good agreement is observed for all configurations in the two different measurement setups. We note that the bandwidth increases with the height of the air cavity. The antenna with a 250 μm-height air cavity exhibits a 14.5% relative bandwidth (atVSWR = 2) and covers the entire frequency band of the standard [3].

The antenna gain in the main axis of radiation (azimuth position $\theta = 0°$) is presented in Fig. 25 for the three cavity heights. A good agreement between measurement (realized at Lab-STICC) and simulation is observed for all configurations. A gain greater than 5 dBi is reached over 15% relative bandwidth for an air cavity equal to 125 and 250 μm. And the peak observed around 53 GHz can be explained by reflections on metallic surface of the probes station.

Figures 26 and 27 present the measured and simulated radiation patterns for two different configurations: without air cavity (Fig. 26) and with an air cavity equal to 125 μm (Fig. 27). The radiation patterns measured with the two test

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benches show a good agreement with simulation. The discrepancies can be explained by the proximity of the probes and the measurement environment.

The performances of these configurations allow expecting hybrid integration between silicon and Duroïd substrates to increase gain.

V. CONCLUSION

In order to target mmWave applications in the 60 GHz frequency band, two research axes are conducted to propose antenna solutions with low-cost constraints to address mass market. In this context, the co-integration of the antenna with circuits on silicon substrates is investigated considering an SoC approach. The packaging is also studied and, by taking into account the antenna environment, a material is assembled with silicon chip and acts as a "lens", and thus focusing system. Such assembly can increase gain value and is compatible with an industrial process. For mmWave applications requiring beamforming, hybrid integration techniques appear as a good tradeoff to report antenna and lossless feeding structures on an appropriate passive circuit supporting material. In this study, a hybrid antenna combining silicon and IPD^{TM} technologies is proposed. The advantage of this antenna is mainly related to its coupling element directly inserted on silicon, thus allowing immediate interfacing with on-chip ICs for beamforming operations.

From an industrial point of view, the antenna integration solution depends on the targeted application and associated production volume. For a short-range application (kiosk downloading), the antenna specifications (gain = 5 dBi) make possible antenna integration on silicon substrates due to an acceptable needed silicon area. However, for beamforming functions (W-HDMI application), an SiP approach is considered due to the antenna array area.

ACKNOWLEDGEMENTS

This work is supported by the collaborative MEDEA+ European project "Qstream".

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https://doi.org/10.1017/S1759078711000213 Published online by Cambridge University Press

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